

## AUIRFR5410-VB Datasheet

### P-Channel 100 V (D-S) MOSFET

#### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)	$Q_g$ (Typ.)
- 100	0.250 at $V_{GS} = - 10$ V	- 8.8	11.7
	0.280 at $V_{GS} = - 4.5$ V	- 8.0	

#### FEATURES

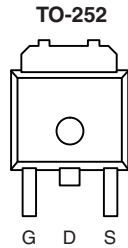
- Halogen-free According to IEC 61249-2-21 Definition
- Trench Power MOSFET
- 100 %  $R_g$  and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

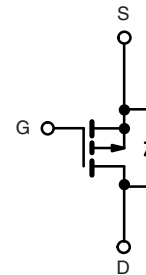
#### APPLICATIONS

- Power Switch
- DC/DC Converters



Top View

Drain Connected to Tab



P-Channel MOSFET

#### ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	- 100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150$ °C)	$I_D$	$T_C = 25$ °C	A
		$T_C = 70$ °C	
Pulsed Drain Current	$I_{DM}$	- 25	
Avalanche Current	$I_{AS}$	- 18	
Single Avalanche Energy <sup>a</sup>	$E_{AS}$	16.2	mJ
Maximum Power Dissipation <sup>a</sup>	$P_D$	$T_C = 25$ °C	W
		$T_A = 25$ °C <sup>c</sup>	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150	°C

#### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient (PCB Mount) <sup>c</sup>	$R_{thJA}$	50	°C/W
Junction-to-Case (Drain)	$R_{thJC}$	3.9	

Notes:

a. Duty cycle  $\leq 1$  %.

b. See SOA curve for voltage derating.

c. When Mounted on 1" square PCB (FR-4 material).

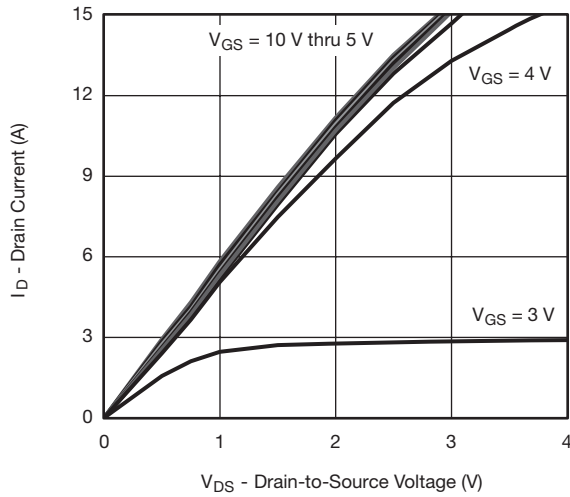
SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{DS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	- 100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	- 1		- 2.5	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 250$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -100\text{ V}, V_{GS} = 0\text{ V}$			- 1	$\mu\text{A}$
		$V_{DS} = -100\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^{\circ}\text{C}$			- 50	
		$V_{DS} = -100\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^{\circ}\text{C}$			- 250	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \leq -10\text{ V}, V_{GS} = -10\text{ V}$	- 15			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -3.6\text{ A}$		0.250		$\Omega$
		$V_{GS} = -4.5\text{ V}, I_D = -3.4\text{ A}$		0.280		
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -15\text{ V}, I_D = -3.6\text{ A}$		12		S
Dynamic <sup>b</sup>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = -50\text{ V}, f = 1\text{ MHz}$		1055		pF
Output Capacitance	$C_{oss}$			65		
Reverse Transfer Capacitance	$C_{rss}$			41		
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{DS} = -50\text{ V}, V_{GS} = -10\text{ V}, I_D = -3.6\text{ A}$		23.2	34.8	nC
		$V_{DS} = -50\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -3.6\text{ A}$		11.7	17.6	
					3.5	
Gate-Source Charge <sup>c</sup>	$Q_{gs}$			4.8		
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$					
Gate Resistance	$R_g$	$f = 1\text{ MHz}$	1.2	5.7	11.5	$\Omega$
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = -50\text{ V}, R_L = 17.2\text{ }\Omega$ $I_D \cong -2.9\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$		7	14	ns
Rise Time <sup>c</sup>	$t_r$			12	18	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$			33	50	
Fall Time <sup>c</sup>	$t_f$			9	18	
Drain-Source Body Diode Ratings and Characteristics $T_C = 25\text{ }^{\circ}\text{C}$ <sup>b</sup>						
Continuous Current	$I_S$				- 8.8	A
Pulsed Current	$I_{SM}$				- 15	
Forward Voltage <sup>a</sup>	$V_{SD}$	$I_F = -2.9\text{ A}, V_{GS} = 0\text{ V}$		- 0.8	- 1.5	V
Reverse Recovery Time	$t_{rr}$	$I_F = -2.9\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}$		50	75	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			- 4	- 6	A
Reverse Recovery Charge	$Q_{rr}$			98	147	nC

Notes:

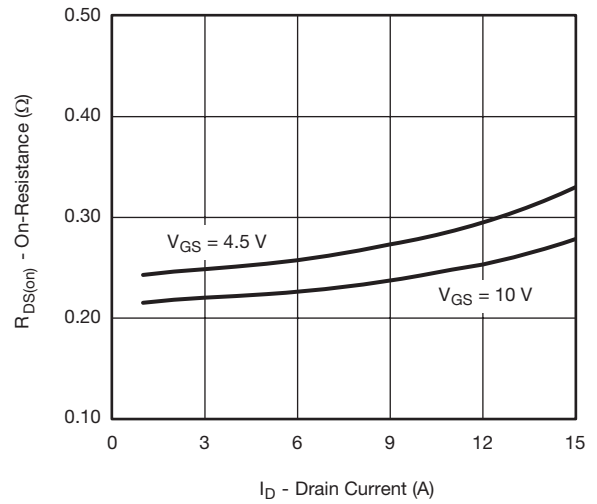
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
 b. Guaranteed by design, not subject to production testing.  
 c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

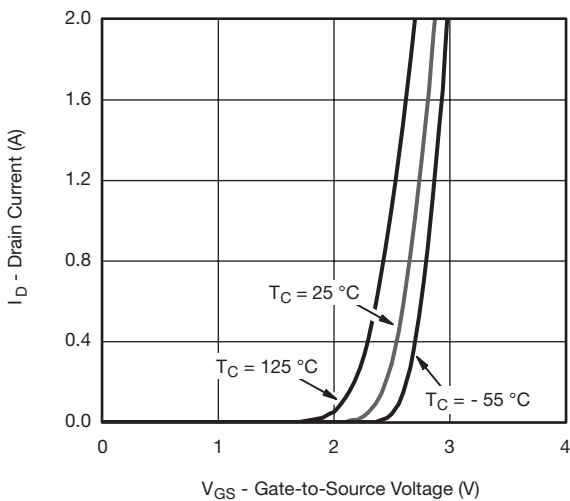
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



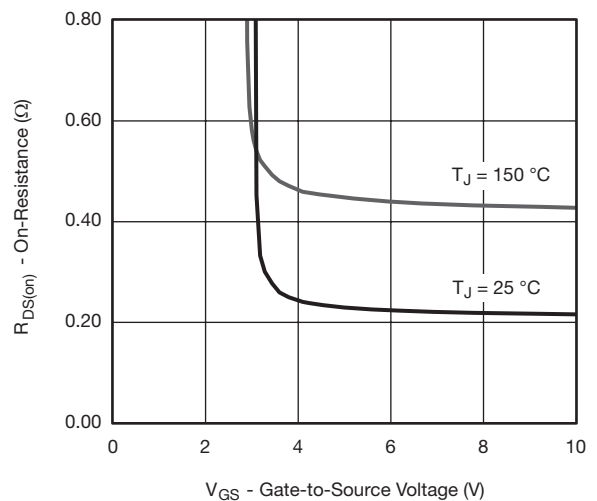
**Output Characteristics**



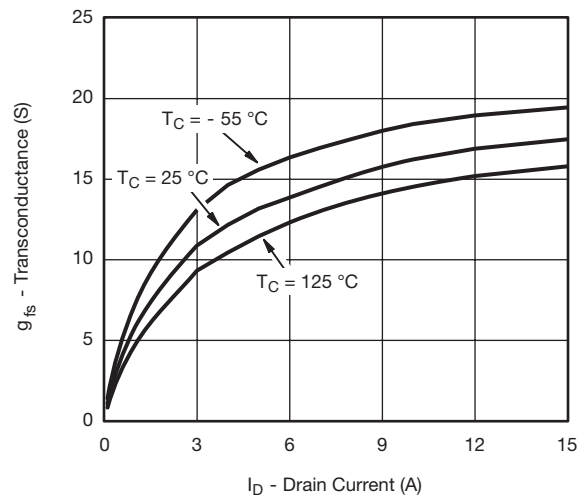
**On-Resistance vs. Drain Current**



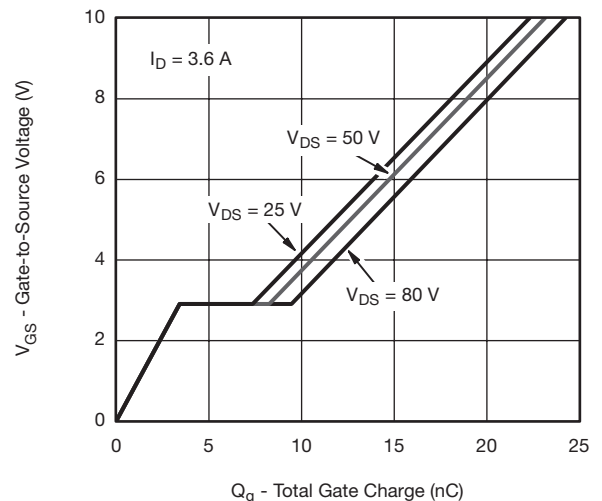
**Transfer Characteristics**



**On-Resistance vs. Gate-to-Source Voltage**

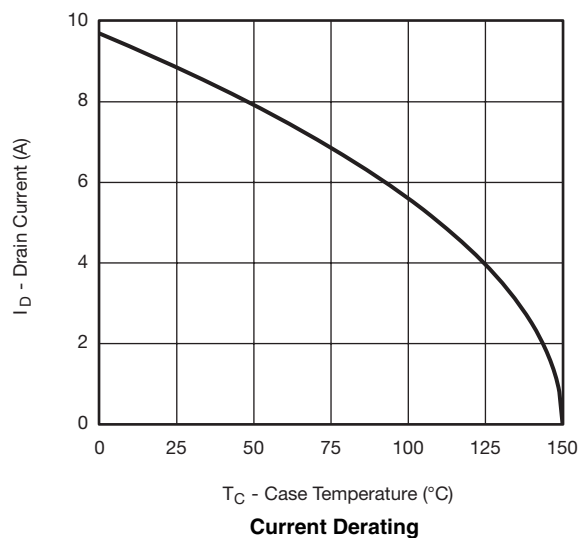
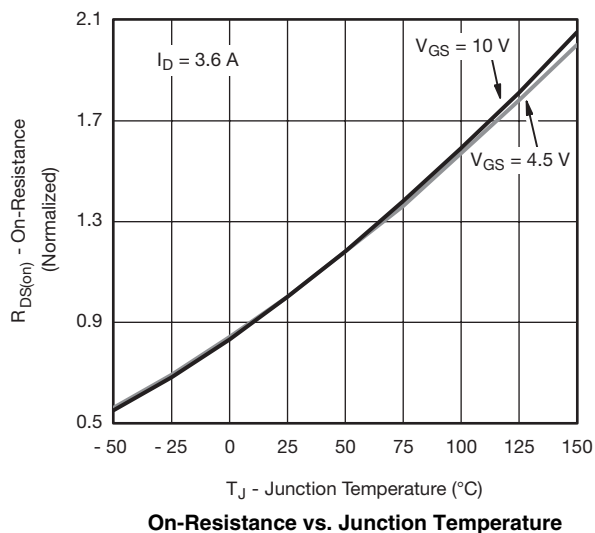
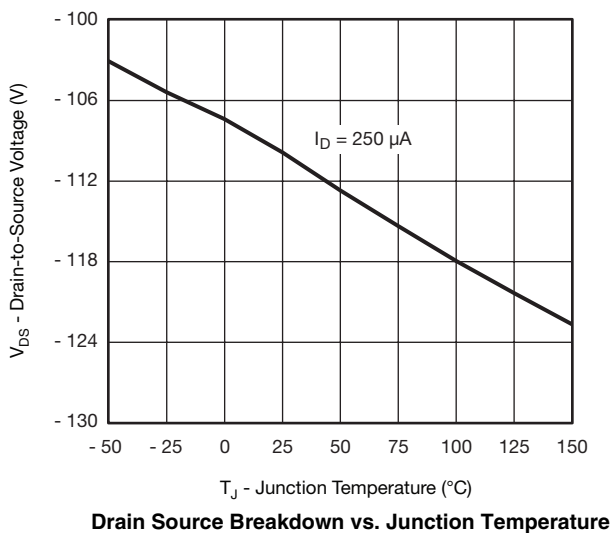
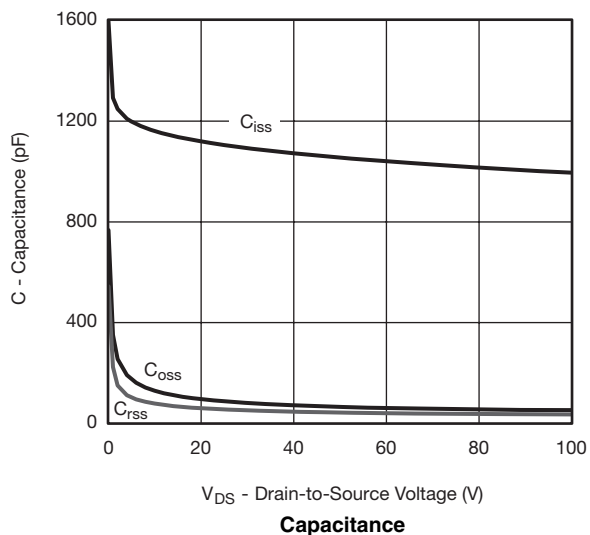
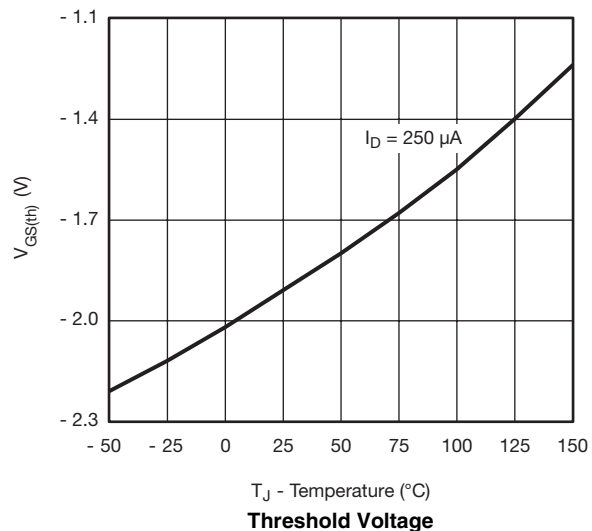
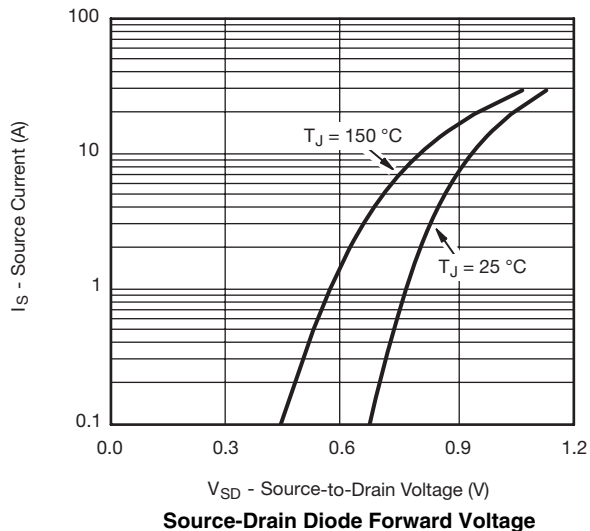


**Transconductance**

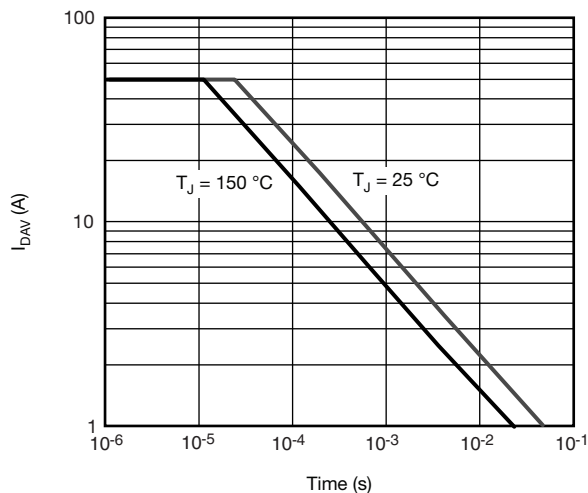


**Gate Charge**

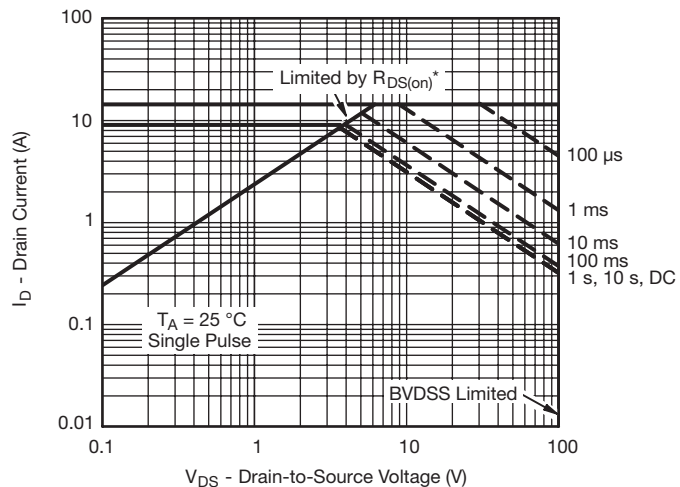
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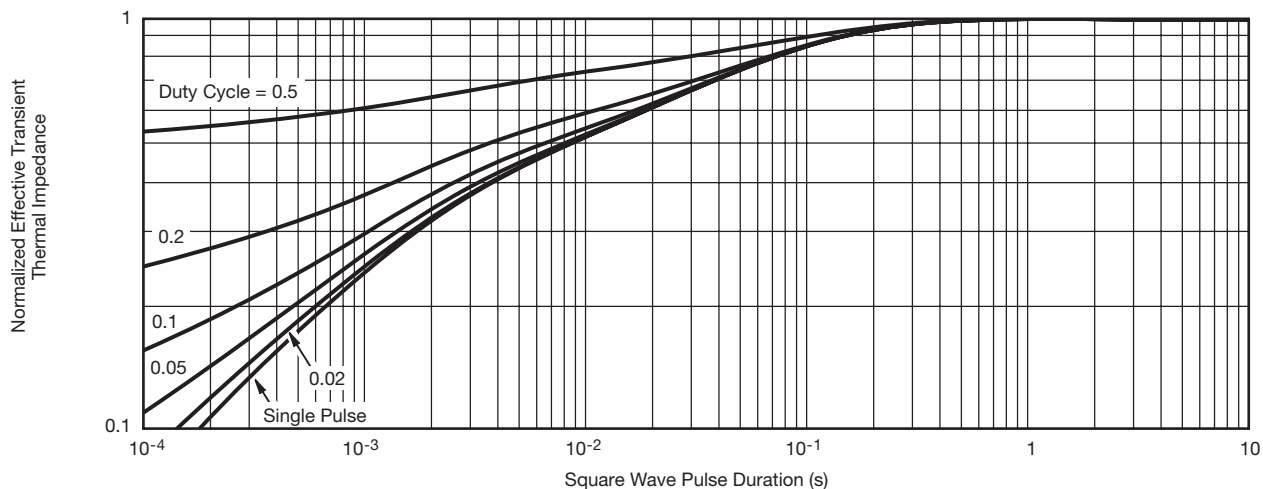


Single Pulse Avalanche Current Capability vs. Time



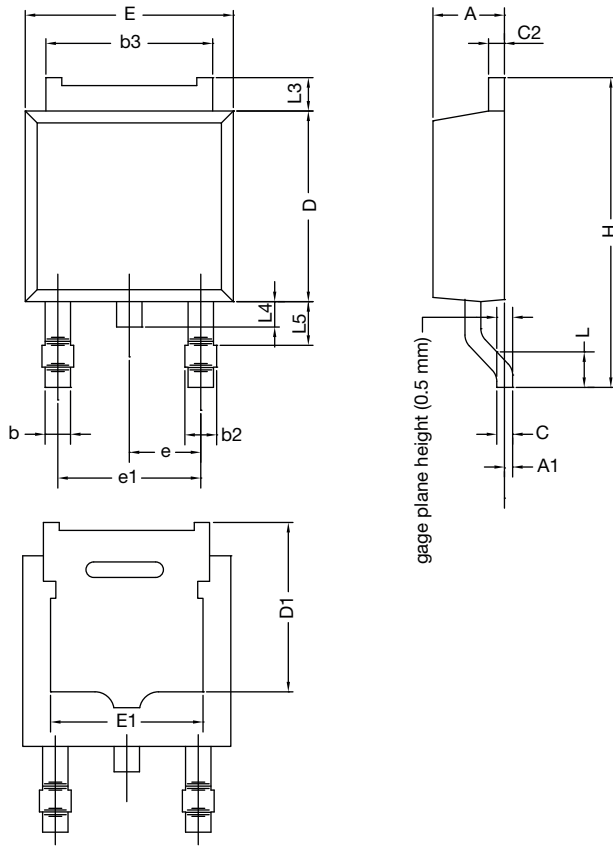
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

## TO-252AA Case Outline

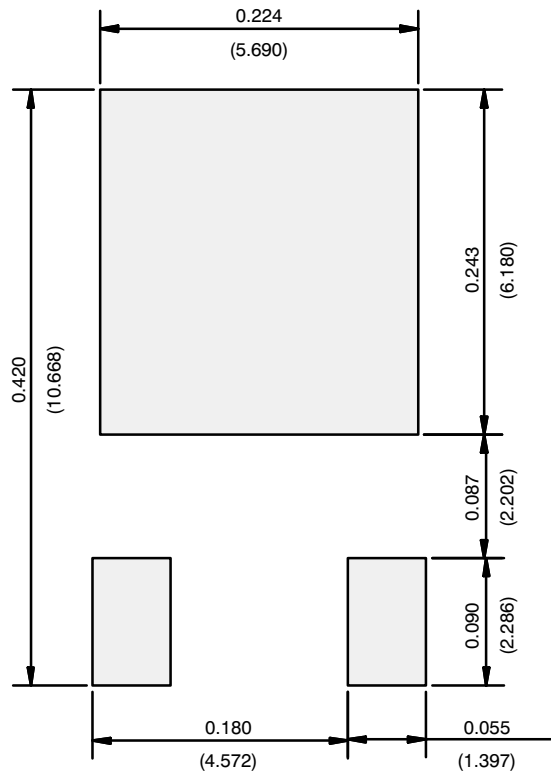


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T16-0236-Rev. P, 16-May-16 DWG: 5347				

### Notes

- Dimension L3 is for reference only.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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