

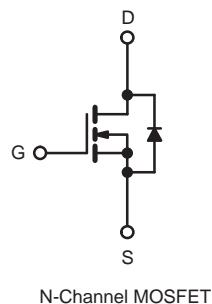
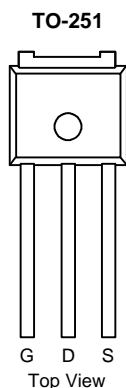
NCE65T2K4I-VB Datasheet

N-Channel 650V (D-S) Super Junction Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	650	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	2.3
Q_g (Max.) (nC)	31	
Q_{gs} (nC)	4.6	
Q_{gd} (nC)	17	
Configuration	Single	

FEATURES

- Isolated Package
- High Voltage Isolation = 2.5 kV_{RMS} (t = 60 s; f = 60 Hz)
- Sink to Lead Creepage Distance = 4.8 mm
- Dynamic dV/dt Rating
- Low Thermal Resistance
- Lead (Pb)-free Available


RoHS*
 COMPLIANT


ABSOLUTE MAXIMUM RATINGS T _C = 25 °C, unless otherwise noted					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V _{DS}	650	V
Gate-Source Voltage			V _{GS}	± 20	
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	I _D	2.0	A
		T _C = 100 °C		1.6	
Pulsed Drain Current ^a			I _{DM}	10	
Linear Derating Factor				0.28	W/°C
Single Pulse Avalanche Energy ^b			E _{AS}	250	mJ
Repetitive Avalanche Current ^a			I _{AR}	1.5	A
Repetitive Avalanche Energy ^a			E _{AR}	3.5	mJ
Maximum Power Dissipation	T _C = 25 °C		P _D	35	W
Peak Diode Recovery dV/dt ^c			dV/dt	3.0	V/ns
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300 ^d	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 73\text{ mH}$, $R_G = 25\text{ }\Omega$, $I_{AS} = 1.5\text{ A}$ (see fig. 12).
- $I_{SD} \leq 1.6\text{ A}$, $dI/dt \leq 60\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	65	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	3.6	

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		650	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.62	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 650 V, V _{GS} = 0 V		-	-	100	μA
		V _{DS} = 480 V, V _{GS} = 0 V, T _J = 125 °C		-	-	500	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 1.5 A ^b	-	2.3	-	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 1.5 A ^b		2.2	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	660	-	pF
Output Capacitance	C _{oss}			-	86	-	
Reverse Transfer Capacitance	C _{rss}			-	19	-	
Drain to Sink Capacitance	C	f = 1.0 MHz		-	12	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 1.6 A, V _{DS} = 360 V, see fig. 6 and 13 ^b	-	-	31	nC
Gate-Source Charge	Q _{gs}			-	-	4.6	
Gate-Drain Charge	Q _{gd}			-	-	17	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 300 V, I _D = 1.6 A, R _G = 12 Ω, R _D = 82 Ω, see fig. 10 ^b		-	11	-	ns
Rise Time	t _r			-	13	-	
Turn-Off Delay Time	t _{d(off)}			-	35	-	
Fall Time	t _f			-	14	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	2.0	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	10	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 1.5 A, V _{GS} = 0 V ^b		-	-	1.6	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 1.6 A, dI/dt = 100 A/μs ^b		-	400	810	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	2.1	4.2	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
 b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

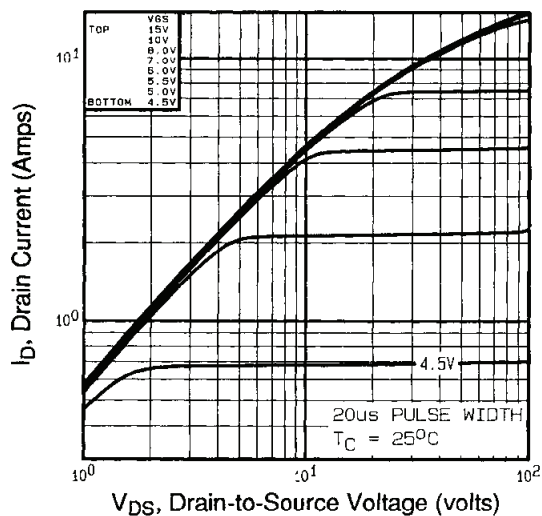
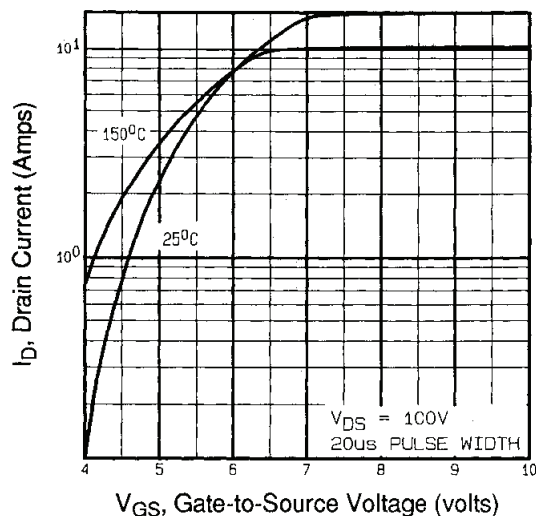
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted
Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$ 

Fig. 3 - Typical Transfer Characteristics

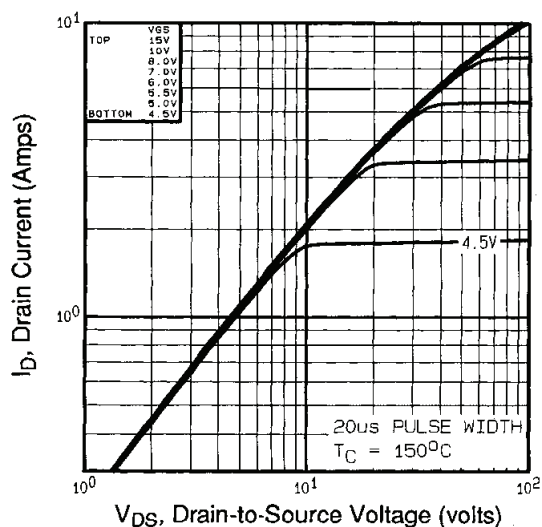
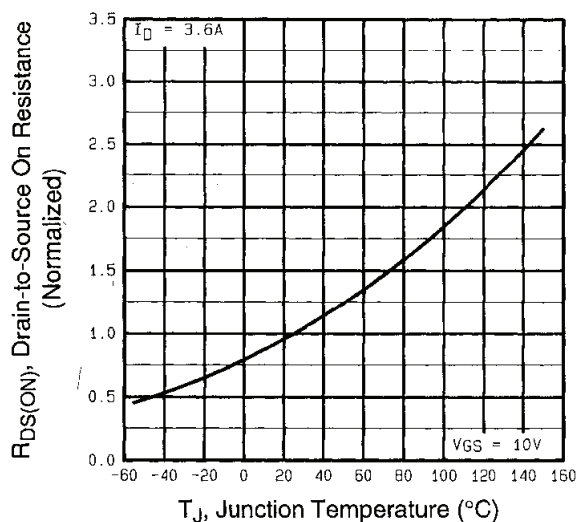
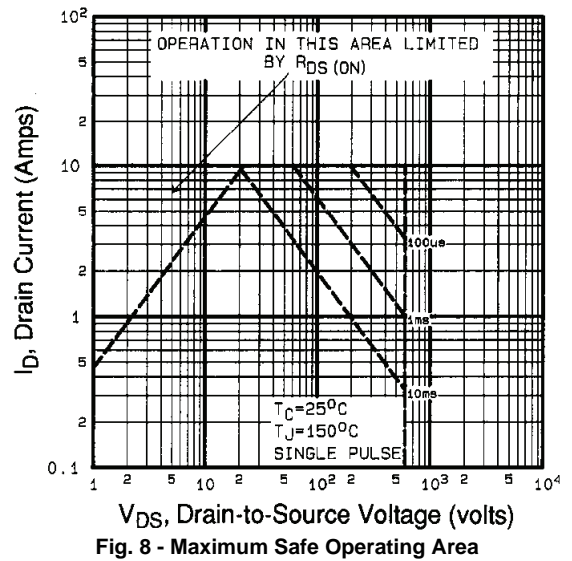
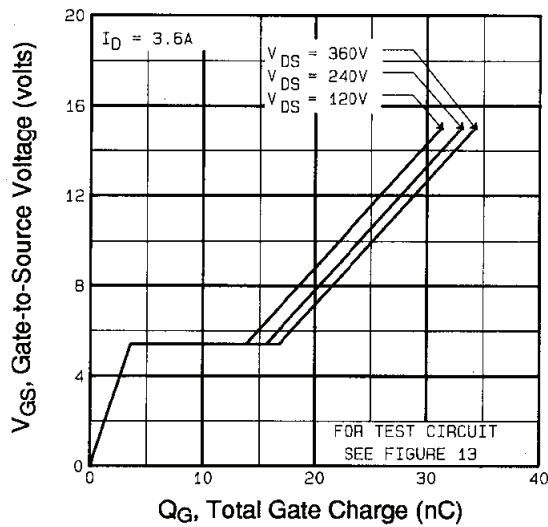
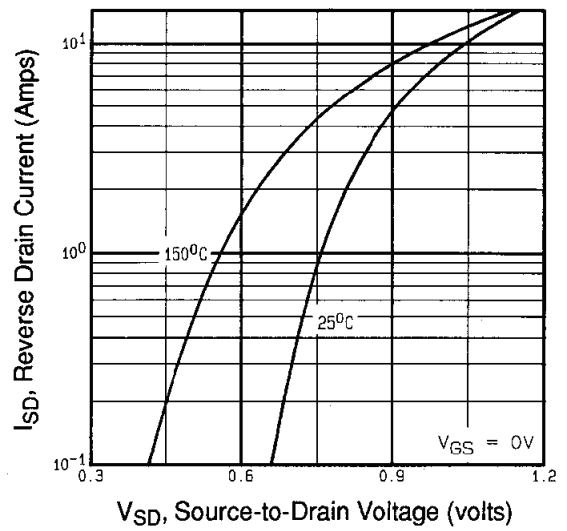
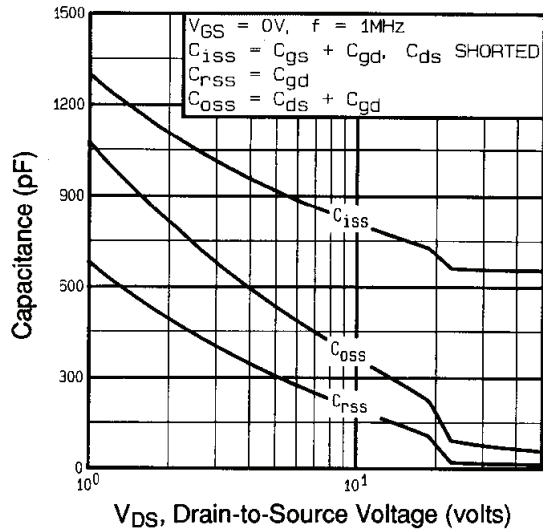
Fig. 2 - Typical Output Characteristics, $T_C = 150^\circ\text{C}$ 

Fig. 4 - Normalized On-Resistance vs. Temperature



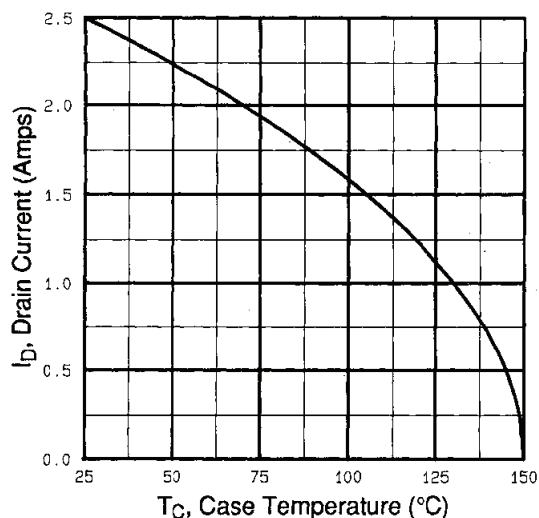


Fig. 9 - Maximum Drain Current vs. Case Temperature

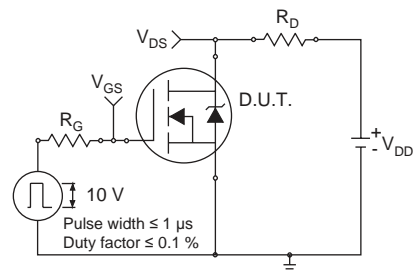


Fig. 10a - Switching Time Test Circuit

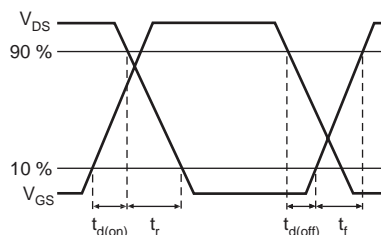


Fig. 10b - Switching Time Waveforms

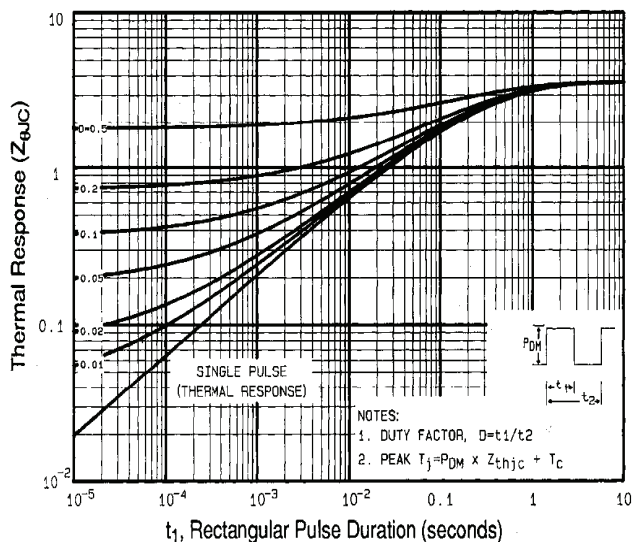


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

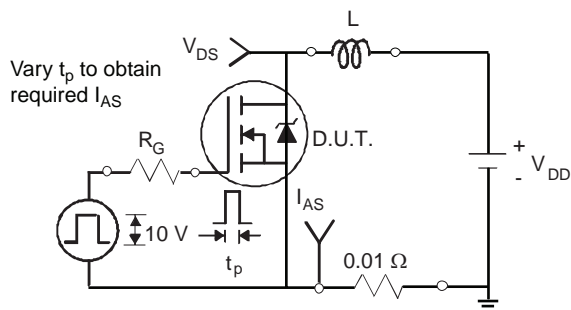


Fig. 12a - Unclamped Inductive Test Circuit

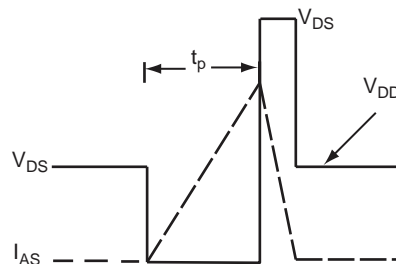


Fig. 12b - Unclamped Inductive Waveforms

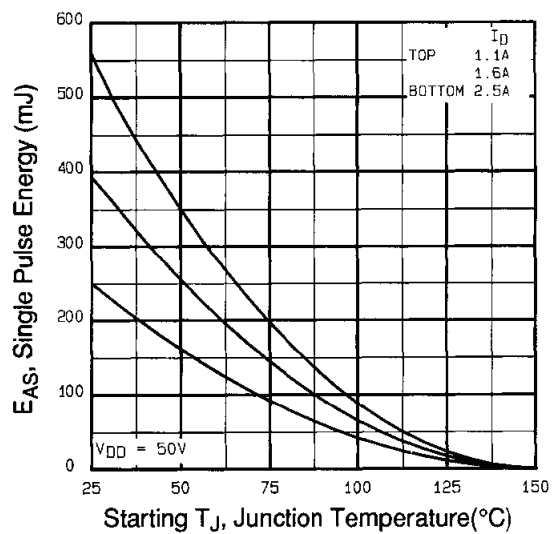


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

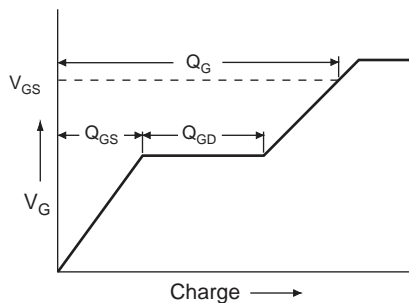


Fig. 13a - Basic Gate Charge Waveform

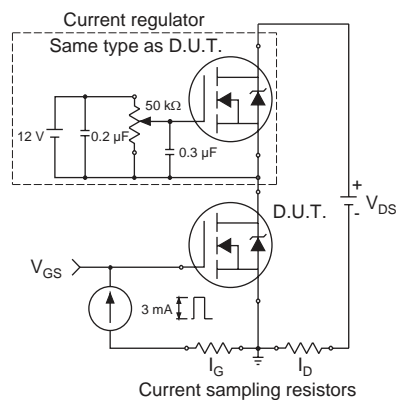
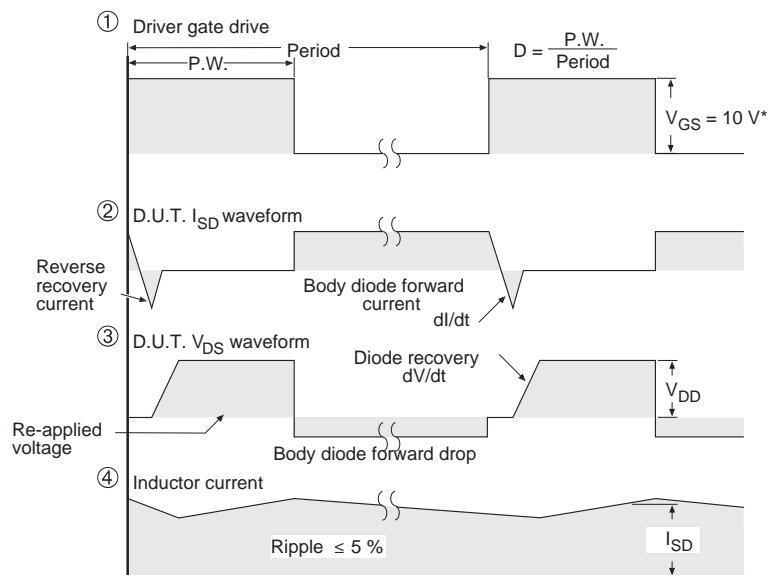
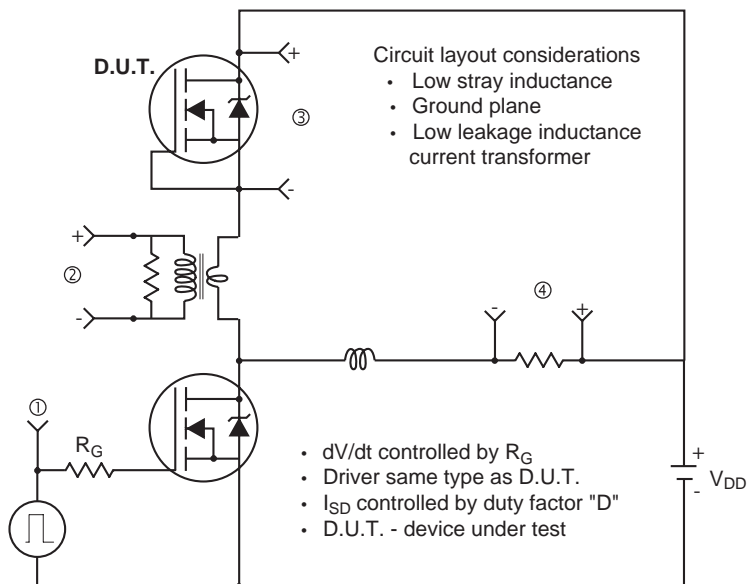


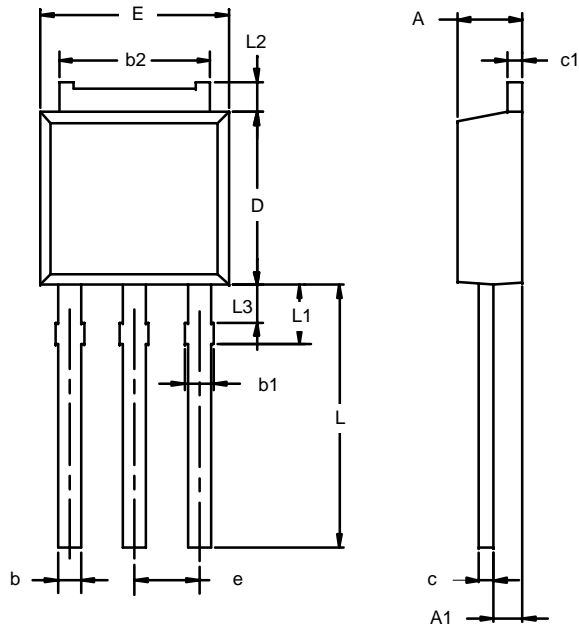
Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5 V$ for logic level devices and $3 V$ drive devices

Fig. 14 - For N-Channel

TO-251AA (DPAK)

Note: Dimension L3 is for reference only.

Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	2.21	2.38	0.087	0.094
A1	0.89	1.14	0.035	0.045
b	0.71	0.89	0.028	0.035
b1	0.76	1.14	0.030	0.045
b2	5.23	5.43	0.206	0.214
c	0.46	0.58	0.018	0.023
c1	0.46	0.58	0.018	0.023
D	5.97	6.22	0.235	0.245
E	6.48	6.73	0.255	0.265
e	2.28 BSC		0.090 BSC	
L	8.89	9.53	0.350	0.375
L1	1.91	2.28	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.15	1.52	0.045	0.060
ECN: S-03946—Rev. E, 09-Jul-01 DWG: 5346				

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