

## NCE65R1K2I-VB Datasheet

## N-Channel 650V (D-S) Super Junction Power MOSFET

## PRODUCT SUMMARY

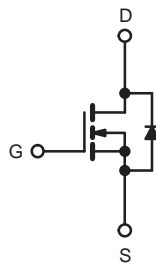
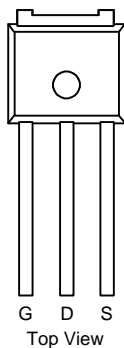
$V_{DS}$ (V)	650	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	0.95
$Q_g$ (Max.) (nC)	15	
$Q_{gs}$ (nC)	3	
$Q_{gd}$ (nC)	6	
Configuration	Single	

## FEATURES

- Low Gate Charge  $Q_g$  Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic  $dV/dt$  Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Compliant to RoHS directive 2002/95/EC


 Available  
**RoHS\***  
 COMPLIANT

TO-251



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS  $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			$V_{DS}$	650	V
Gate-Source Voltage			$V_{GS}$	$\pm 30$	
Continuous Drain Current <sup>a</sup>	$V_{GS}$ at 10 V	$T_C = 25\text{ }^\circ\text{C}$	$I_D$	5	A
Continuous Drain Current		$T_C = 100\text{ }^\circ\text{C}$		4	
Pulsed Drain Current <sup>a</sup>			$I_{DM}$	16	
Linear Derating Factor				1.67/0.8/0.3	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy <sup>b</sup>			$E_{AS}$	120	mJ
Repetitive Avalanche Current <sup>a</sup>			$I_{AR}$	34	A
Repetitive Avalanche Energy <sup>a</sup>			$E_{AR}$	17	mJ
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$		$P_D$	205/35/30	W
Peak Diode Recovery $dV/dt$ <sup>c</sup>			$dV/dt$	4.5	V/ns
Operating Junction and Storage Temperature Range			$T_J, T_{stg}$	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) <sup>d</sup>	for 10 s			300	
Mounting Torque	6-32 or M3 screw			10	
				1.1	N · m


## Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
 b. Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 24\text{ mH}$ ,  $R_G = 25\text{ }\Omega$ ,  $I_{AS} = 3.2\text{ A}$  (see fig. 12).  
 c.  $I_{SD} \leq 3.2\text{ A}$ ,  $dI/dt \leq 90\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .  
 d. 1.6 mm from case.  
 e. Drain current limited by maximum junction temperature.

**THERMAL RESISTANCE RATINGS**

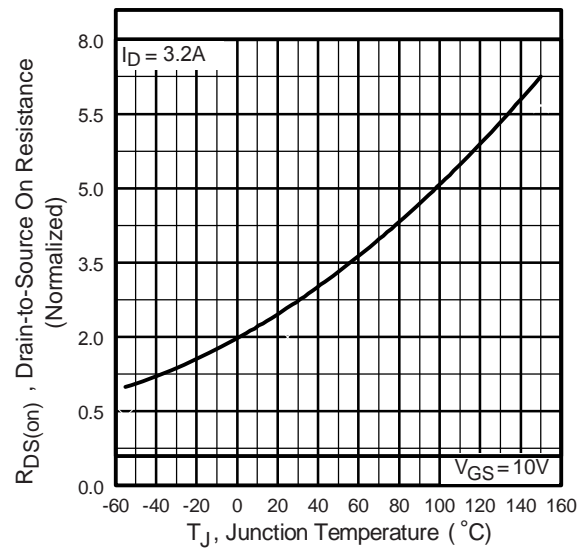
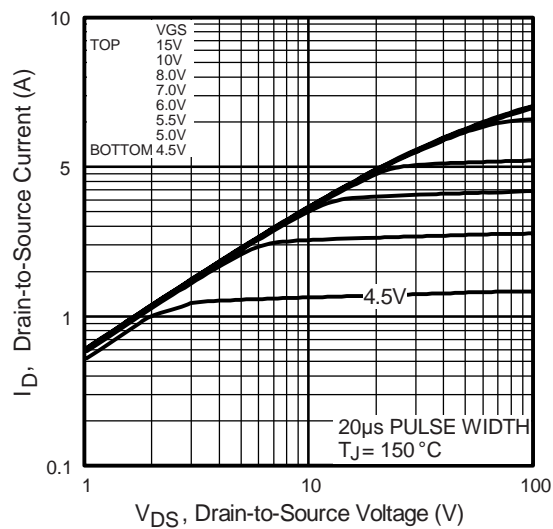
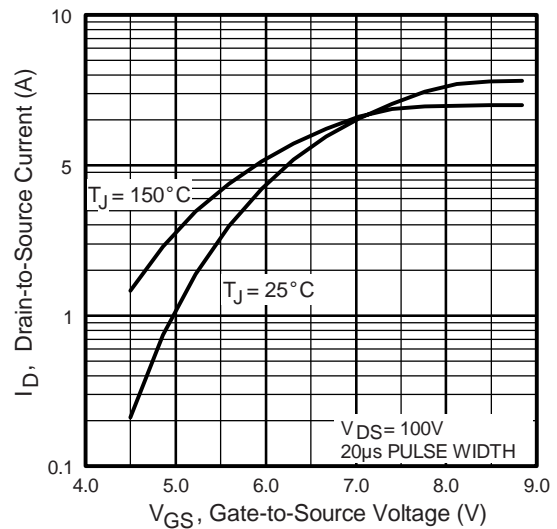
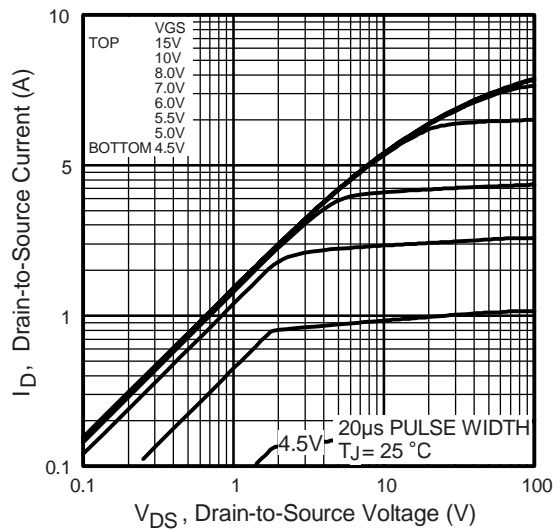
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	3.6/1.2/0.6	

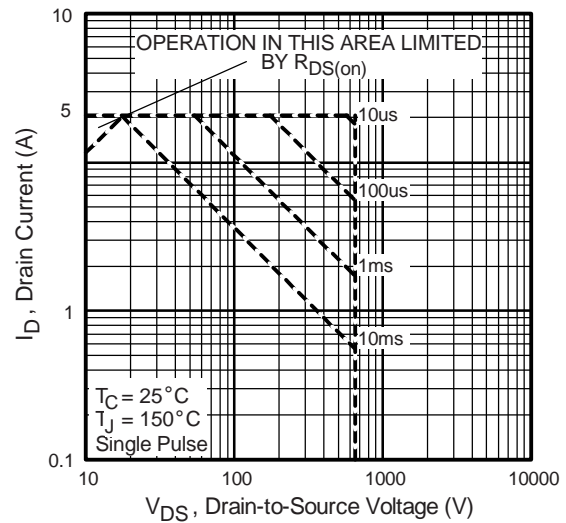
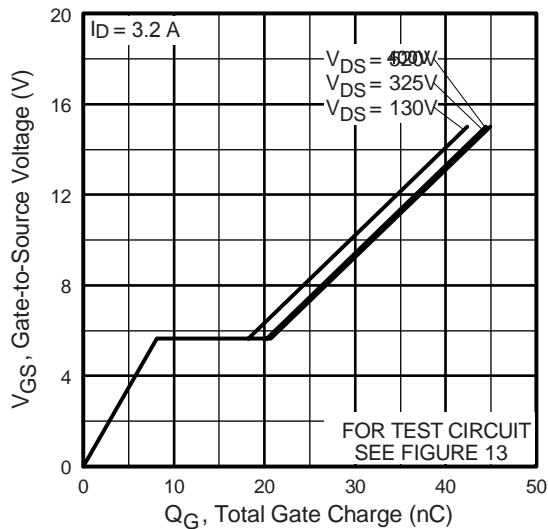
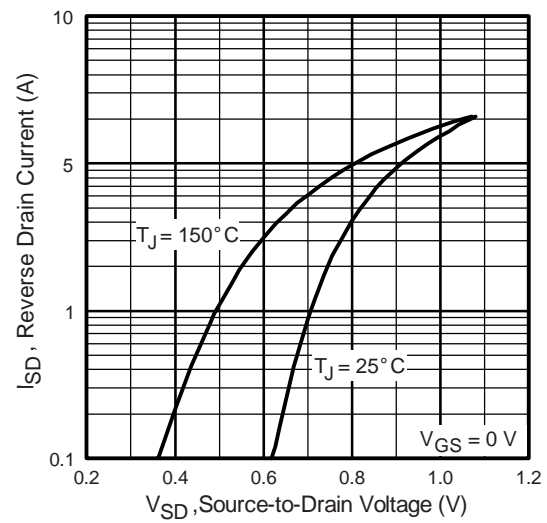
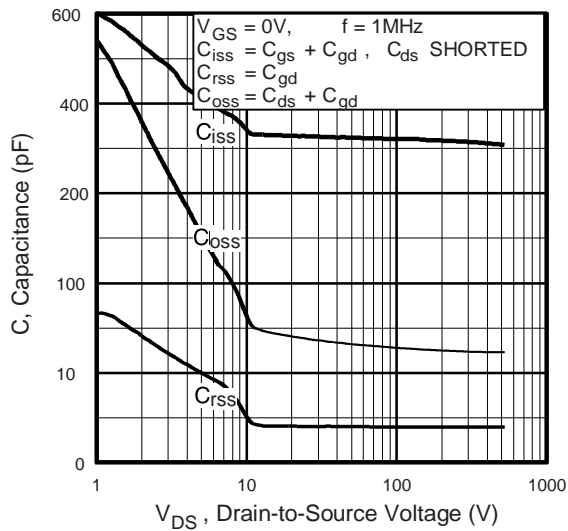
**SPECIFICATIONS**  $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		650	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA <sup>d</sup>		-	0.6	-	mV/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 30 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 650 V, V <sub>GS</sub> = 0 V		-	-	10	μA
		V <sub>DS</sub> = 520 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	100	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 2.5 A <sup>b</sup>	-	0.95	-	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 2.5 A		8	-	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz, see fig. 5		-	320	-	pF
Output Capacitance	C <sub>oss</sub>			-	75	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	4	-	
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 1.0 V, f = 1.0 MHz	-	500	-	pF
			V <sub>DS</sub> = 520 V, f = 1.0 MHz	-	83	-	
Effective Output Capacitance	C <sub>oss eff.</sub>		V <sub>DS</sub> = 0 V to 520 V <sup>c</sup>	-	14	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 2.5 A, V <sub>DS</sub> = 400 V see fig. 6 and 13 <sup>b</sup>	-	-	15	nC
Gate-Source Charge	Q <sub>gs</sub>			-	-	3	
Gate-Drain Charge	Q <sub>gd</sub>			-	-	6	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 325 V, I <sub>D</sub> = 3.2 A R <sub>G</sub> = 9.1 Ω, R <sub>D</sub> = 62 Ω, see fig. 10 <sup>b</sup>		-	18	-	ns
Rise Time	t <sub>r</sub>			-	40	-	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	50	-	
Fall Time	t <sub>f</sub>			-	30	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	5	A
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	16	
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 3.2 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	1.5	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 3.2 A, dI/dt = 100 A/μs <sup>b</sup>		-	180	-	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			-	2.1	3.2	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
 b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .  
 c.  $C_{oss\text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$ .  
 d.  $t = 60\text{ s}$ ,  $f = 60\text{ Hz}$ .

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted




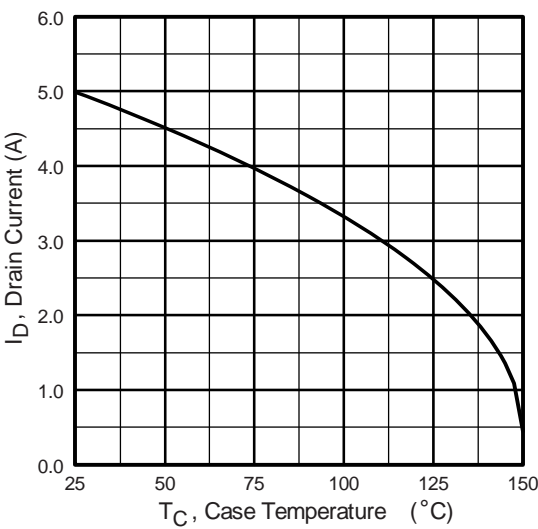


Fig. 9 - Maximum Drain Current vs. Case Temperature

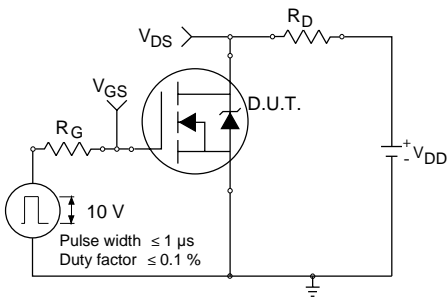


Fig. 10a - Switching Time Test Circuit

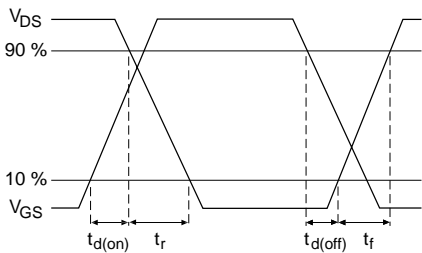


Fig. 10b - Switching Time Waveforms

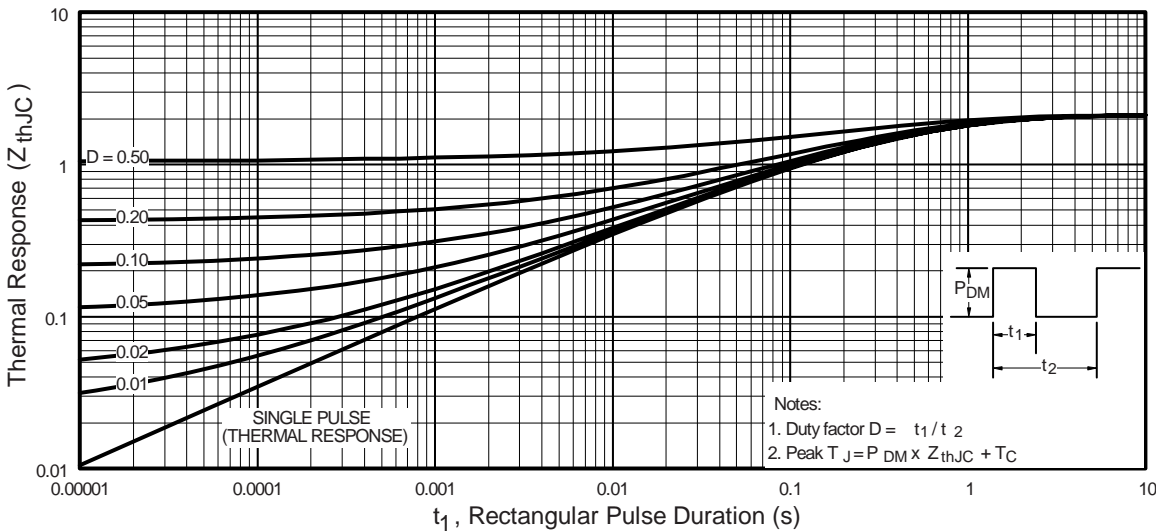


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

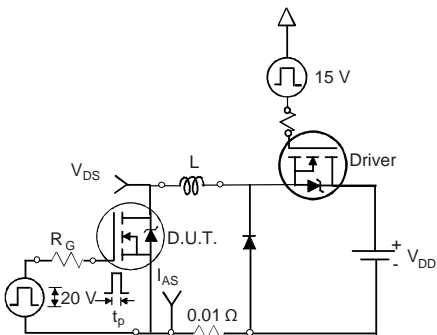


Fig. 12a - Unclamped Inductive Test Circuit

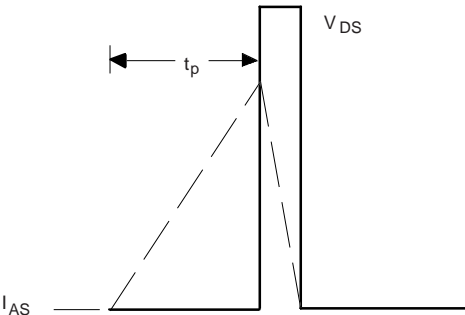


Fig. 12b - Unclamped Inductive Waveforms

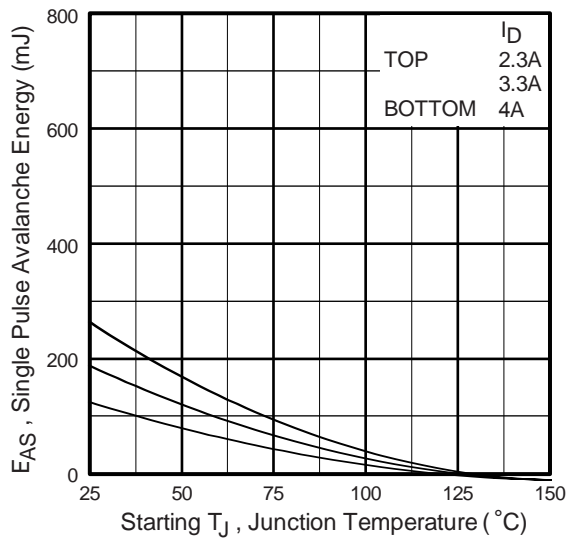


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

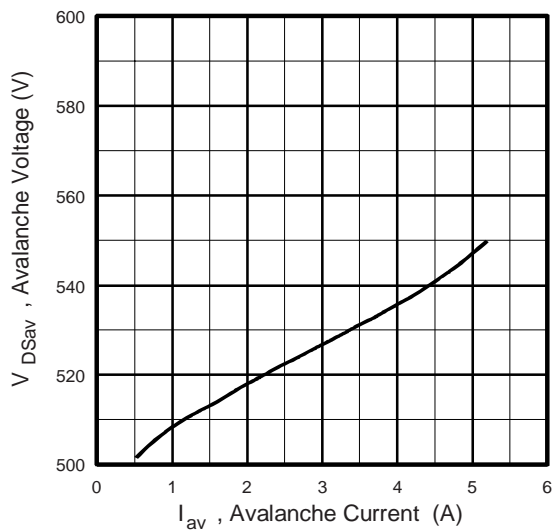


Fig. 12d - Typical Drain-to Source Voltage vs. Avalanche Current

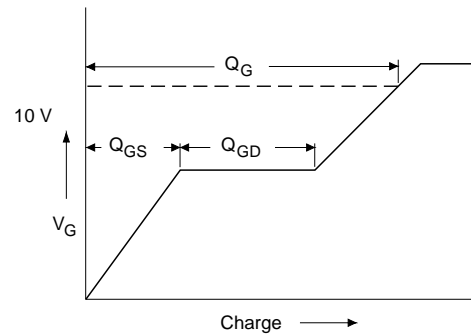


Fig. 13a - Basic Gate Charge Waveform

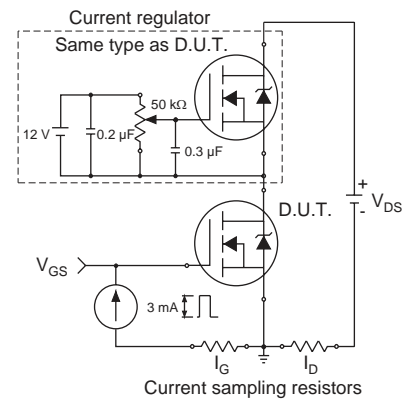
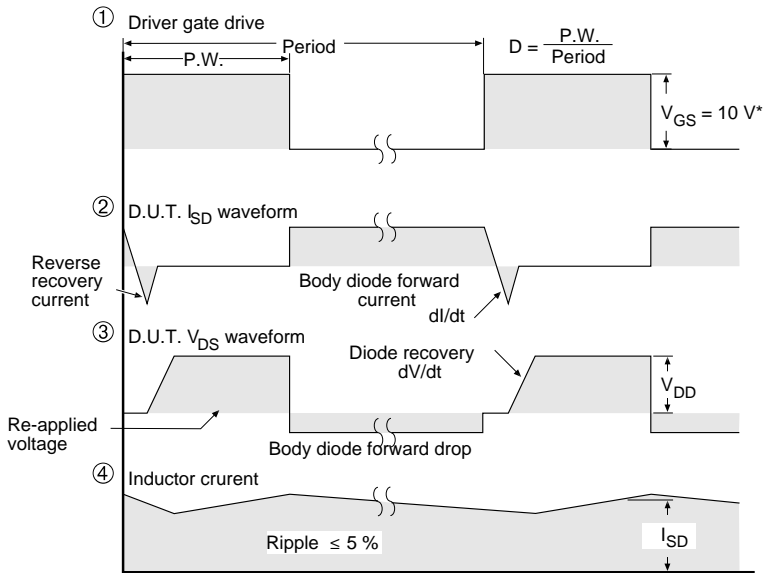
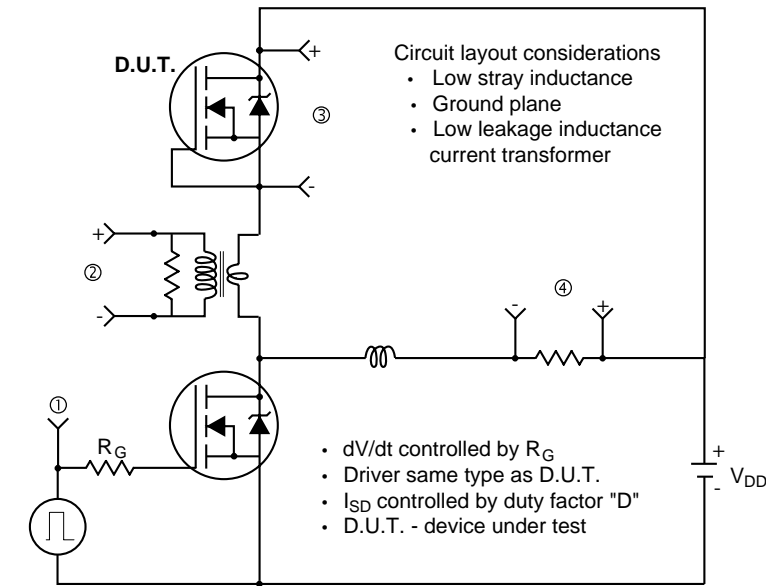


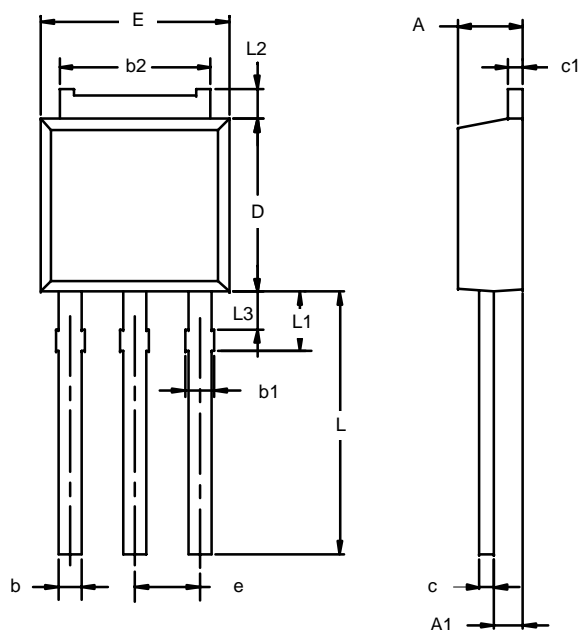
Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



\*  $V_{GS} = 5 V$  for logic level devices

Fig. 14 - For N-Channel

**TO-251AA (DPAK)**

Note: Dimension L3 is for reference only.

Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
<b>A</b>	2.21	2.38	0.087	0.094
<b>A1</b>	0.89	1.14	0.035	0.045
<b>b</b>	0.71	0.89	0.028	0.035
<b>b1</b>	0.76	1.14	0.030	0.045
<b>b2</b>	5.23	5.43	0.206	0.214
<b>c</b>	0.46	0.58	0.018	0.023
<b>c1</b>	0.46	0.58	0.018	0.023
<b>D</b>	5.97	6.22	0.235	0.245
<b>E</b>	6.48	6.73	0.255	0.265
<b>e</b>	2.28 BSC		0.090 BSC	
<b>L</b>	8.89	9.53	0.350	0.375
<b>L1</b>	1.91	2.28	0.075	0.090
<b>L2</b>	0.89	1.27	0.035	0.050
<b>L3</b>	1.15	1.52	0.045	0.060
ECN: S-03946—Rev. E, 09-Jul-01 DWG: 5346				



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