

## NCE60T2K4I-VB Datasheet

### Power MOSFET

#### PRODUCT SUMMARY

$V_{DS}$ (V)	600	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	2.2
$Q_g$ (Max.) (nC)	39	
$Q_{gs}$ (nC)	10	
$Q_{gd}$ (nC)	19	
Configuration	Single	

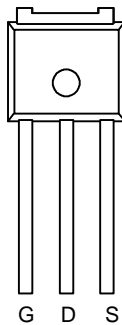
#### FEATURES

- Ultra Low Gate Charge
- Reduced Gate Drive Requirement
- Enhanced 30 V,  $V_{GS}$  Rating
- Reduced  $C_{iss}$ ,  $C_{oss}$ ,  $C_{rss}$
- Extremely High Frequency Operation
- Repetitive Avalanche Rated
- Compliant to RoHS Directive 2002/95/EC

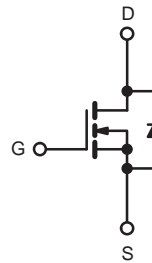


Available  
**RoHS\***  
 COMPLIANT

TO-251



Top View



N-Channel MOSFET

#### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			$V_{DS}$	600	V
Gate-Source Voltage			$V_{GS}$	$\pm 30$	
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25\text{ }^{\circ}\text{C}$	$I_D$	5.5	A
		$T_C = 100\text{ }^{\circ}\text{C}$		4.9	
Pulsed Drain Current <sup>a</sup>			$I_{DM}$	25	
Linear Derating Factor				1.0	W/ $^{\circ}\text{C}$
Single Pulse Avalanche Energy <sup>b</sup>			$E_{AS}$	530	mJ
Repetitive Avalanche Current <sup>a</sup>			$I_{AR}$	6.2	A
Repetitive Avalanche Energy <sup>a</sup>			$E_{AR}$	13	mJ
Maximum Power Dissipation	$T_C = 25\text{ }^{\circ}\text{C}$		$P_D$	125	W
Peak Diode Recovery $dV/dt^c$			$dV/dt$	3.0	V/ns
Operating Junction and Storage Temperature Range			$T_J, T_{stg}$	- 55 to + 150	$^{\circ}\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s			300 <sup>d</sup>	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

#### Notes

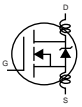

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 25\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 6.2\text{ A}$  (see fig. 12).
- $I_{SD} \leq 6.2\text{ A}$ ,  $dI/dt \leq 80\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.50	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.0	

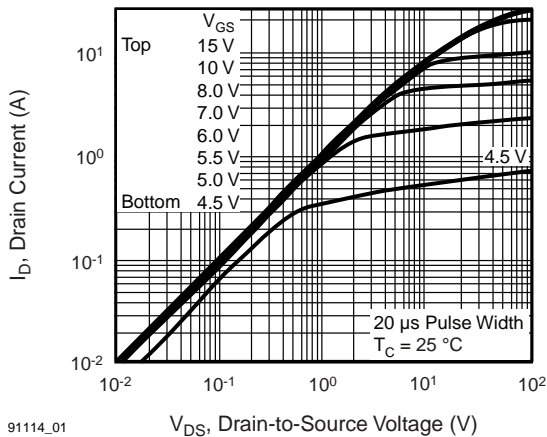
**SPECIFICATIONS** ( $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		600	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.70	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V		-	-	100	μA
		V <sub>DS</sub> = 480 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	500	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 3.7 A <sup>b</sup>	-	2.2	-	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 100 V, I <sub>D</sub> = 3.7 A <sup>b</sup>		3.7	-	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V V <sub>DS</sub> = 25 V f = 1.0 MHz, see fig. 5		-	1100	-	pF
Output Capacitance	C <sub>oss</sub>			-	140	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	15	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 4 A, V <sub>DS</sub> = 360 V, see fig. 6 and 13 <sup>b</sup>	-	-	39	nC
Gate-Source Charge	Q <sub>gs</sub>			-	-	10	
Gate-Drain Charge	Q <sub>gd</sub>			-	-	19	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 4 A R <sub>g</sub> = 9.1 Ω, R <sub>D</sub> = 47 Ω, see fig. 10 <sup>b</sup>		-	12	-	ns
Rise Time	t <sub>r</sub>			-	20	-	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	27	-	
Fall Time	t <sub>f</sub>			-	17	-	
Internal Drain Inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	L <sub>S</sub>			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	4.0	A
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	25	
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 4 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	1.5	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 4 A, dI/dt = 100 A/μs <sup>b</sup>		-	440	680	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			-	2.1	3.2	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					

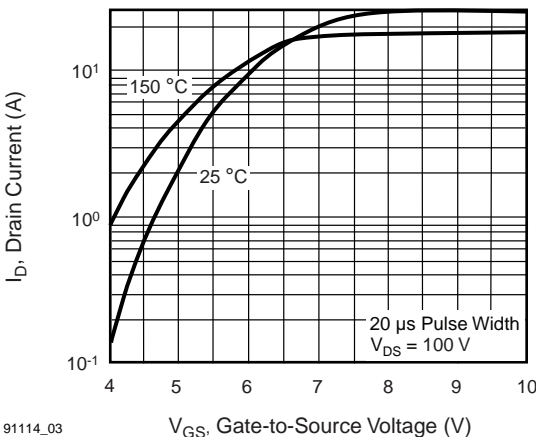
**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
 b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

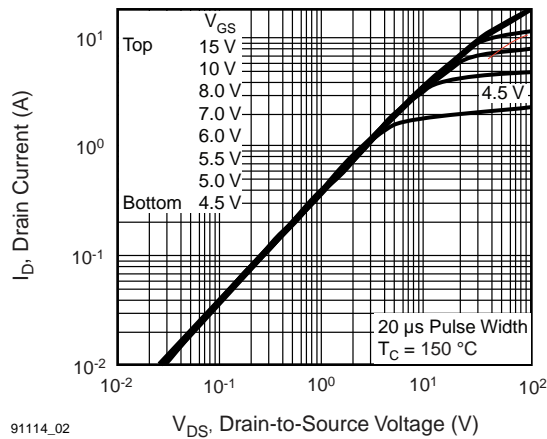
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



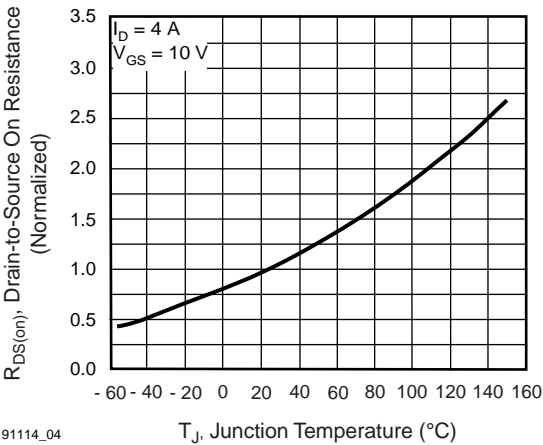
**Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^{\circ}\text{C}$**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^{\circ}\text{C}$**



**Fig. 4 - Normalized On-Resistance vs. Temperature**

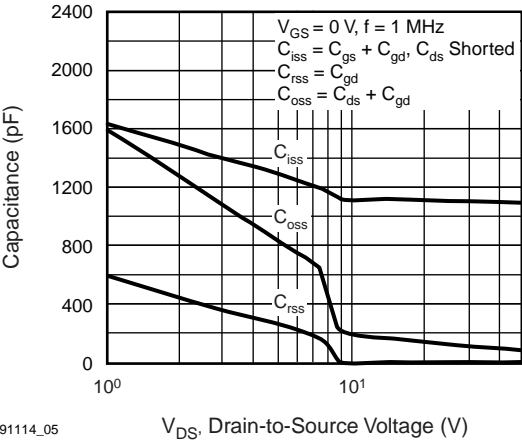


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

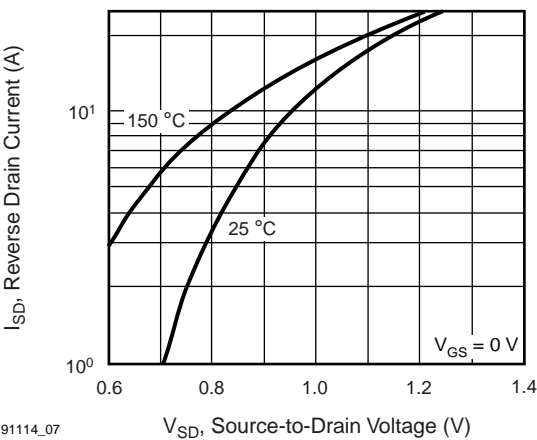


Fig. 7 - Typical Source-Drain Diode Forward Voltage

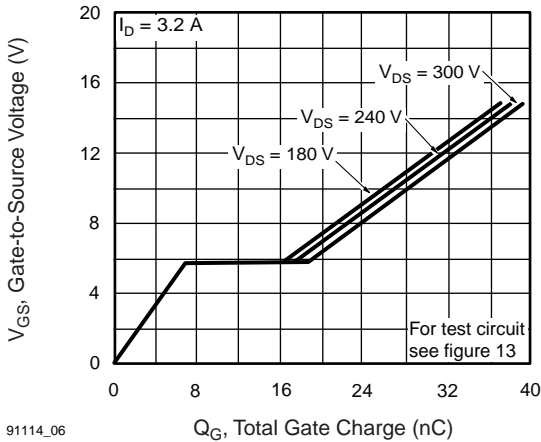


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

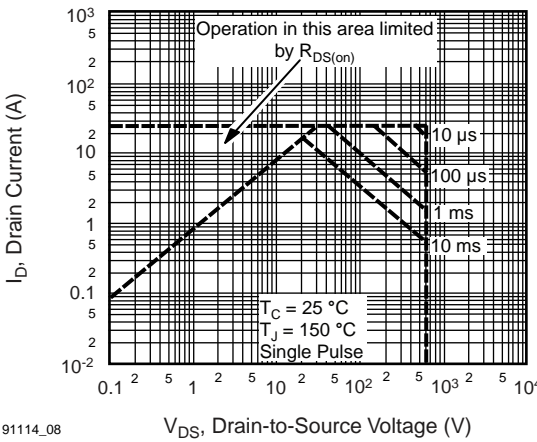
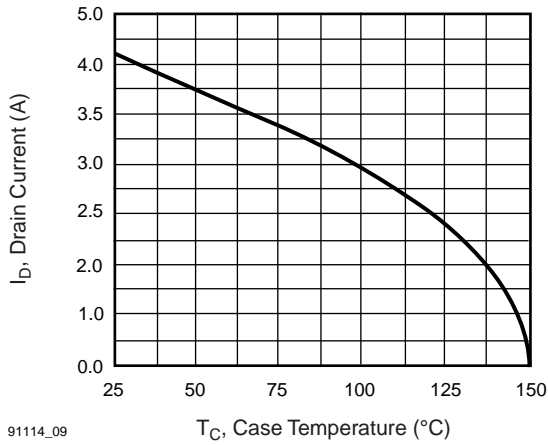
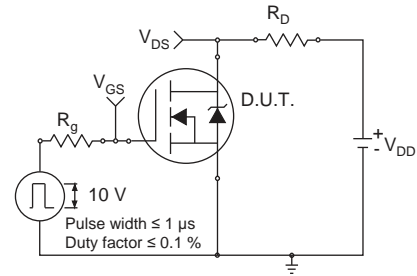


Fig. 8 - Maximum Safe Operating Area

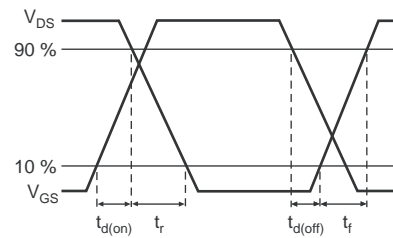


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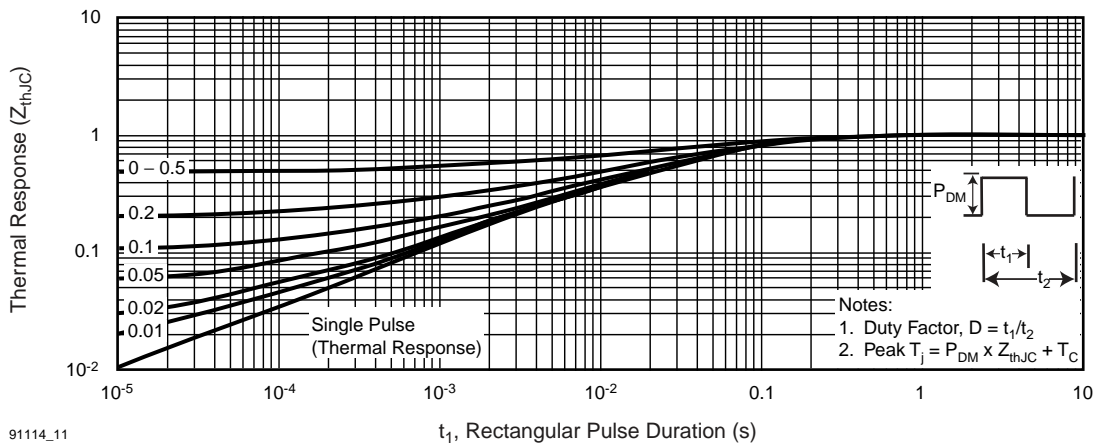
**Fig. 9 - Maximum Drain Current vs. Case Temperature**



**Fig. 10a - Switching Time Test Circuit**

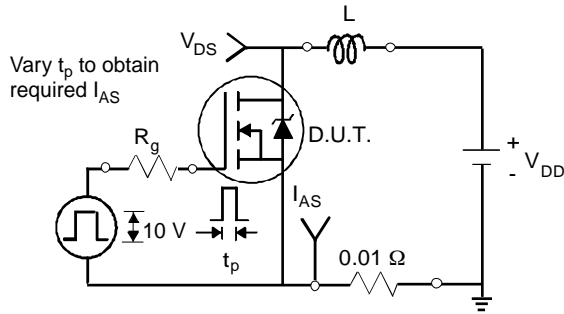


**Fig. 10b - Switching Time Waveforms**

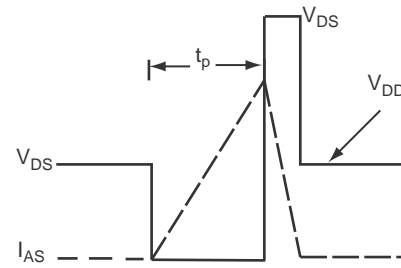


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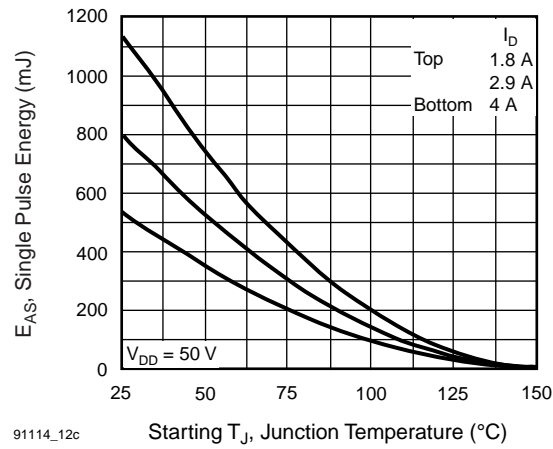
**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**



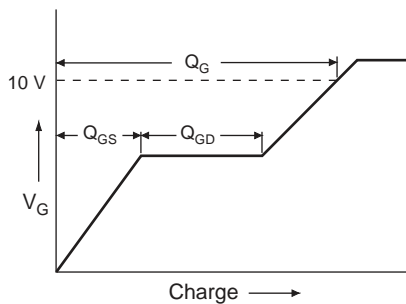
**Fig. 12a - Unclamped Inductive Test Circuit**



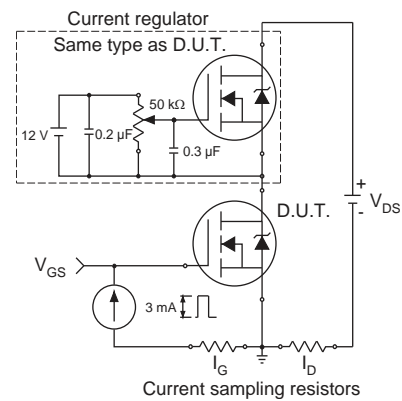
**Fig. 12b - Unclamped Inductive Waveforms**



**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**

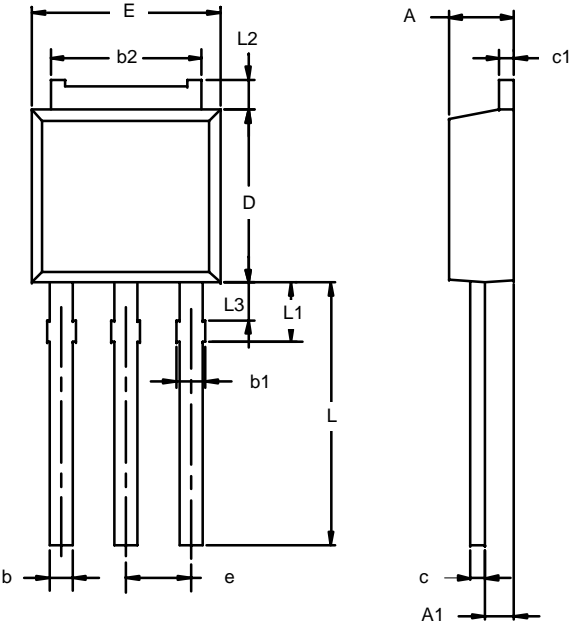


**Fig. 13a - Basic Gate Charge Waveform**



**Fig. 13b - Gate Charge Test Circuit**

TO-251AA (DPAK)



Note: Dimension L3 is for reference only.

Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
<b>A</b>	2.21	2.38	0.087	0.094
<b>A1</b>	0.89	1.14	0.035	0.045
<b>b</b>	0.71	0.89	0.028	0.035
<b>b1</b>	0.76	1.14	0.030	0.045
<b>b2</b>	5.23	5.43	0.206	0.214
<b>c</b>	0.46	0.58	0.018	0.023
<b>c1</b>	0.46	0.58	0.018	0.023
<b>D</b>	5.97	6.22	0.235	0.245
<b>E</b>	6.48	6.73	0.255	0.265
<b>e</b>	2.28 BSC		0.090 BSC	
<b>L</b>	8.89	9.53	0.350	0.375
<b>L1</b>	1.91	2.28	0.075	0.090
<b>L2</b>	0.89	1.27	0.035	0.050
<b>L3</b>	1.15	1.52	0.045	0.060
ECN: S-03946—Rev. E, 09-Jul-01 DWG: 5346				

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