

## NCE0140IA-VB Datasheet

### N-Channel 100-V (D-S), 175 °C MOSFET

**PRODUCT SUMMARY**

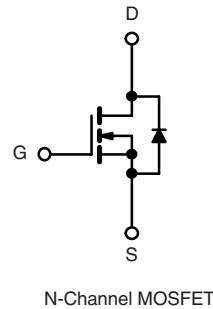
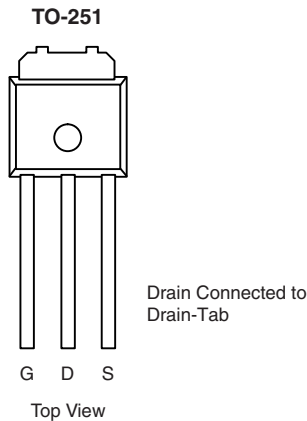
$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>a</sup>	$Q_g$ (Typ.)
100	0.0125 at $V_{GS} = 10$ V	65	48 nC

**FEATURES**

- Trench Power MOSFET
- 100 %  $R_g$  Tested
- 100 % UIS Tested

**APPLICATIONS**

- Primary Side Switch
- Isolated DC/DC Converter

**ABSOLUTE MAXIMUM RATINGS**  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150\text{ }^\circ\text{C}$ )	$I_D$	$T_C = 25\text{ }^\circ\text{C}$	65 <sup>a</sup>
		$T_C = 100\text{ }^\circ\text{C}$	52
		$T_A = 25\text{ }^\circ\text{C}$	8.2 <sup>b</sup>
		$T_A = 100\text{ }^\circ\text{C}$	5.8 <sup>b</sup>
Pulsed Drain Current	$I_{DM}$	200	A
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	65 <sup>a</sup>
		$T_A = 25\text{ }^\circ\text{C}$	2.0 <sup>b</sup>
Single Pulse Avalanche Current	$I_{AS}$	48	
Avalanche Energy	$E_{AS}$	121	mJ
Maximum Power Dissipation	$P_D$	$T_C = 25\text{ }^\circ\text{C}$	156.4
		$T_C = 100\text{ }^\circ\text{C}$	78.2
		$T_A = 25\text{ }^\circ\text{C}$	3.0 <sup>b</sup>
		$T_A = 100\text{ }^\circ\text{C}$	1.5 <sup>b</sup>
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 175	$^\circ\text{C}$

**THERMAL RESISTANCE RATINGS**

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b</sup>	$R_{thJA}$	40	50	$^\circ\text{C/W}$
Maximum Junction-to-Case	$R_{thJC}$	0.85	1.1	

Notes:

a. Package limited.

b. Surface mounted on 1" x 1" FR4 board.

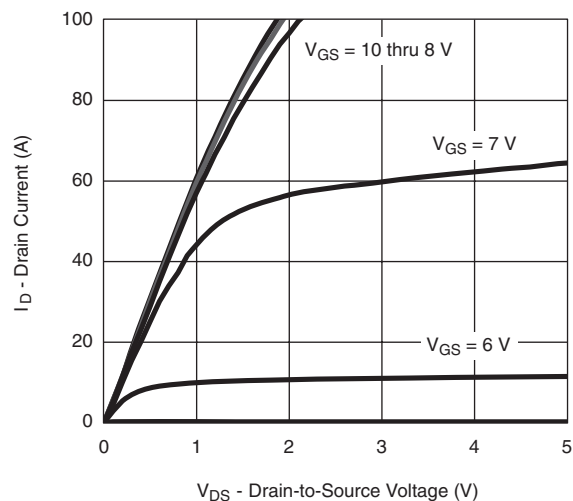
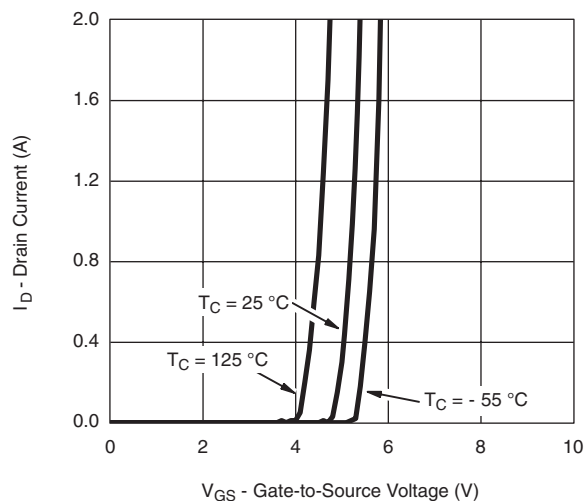
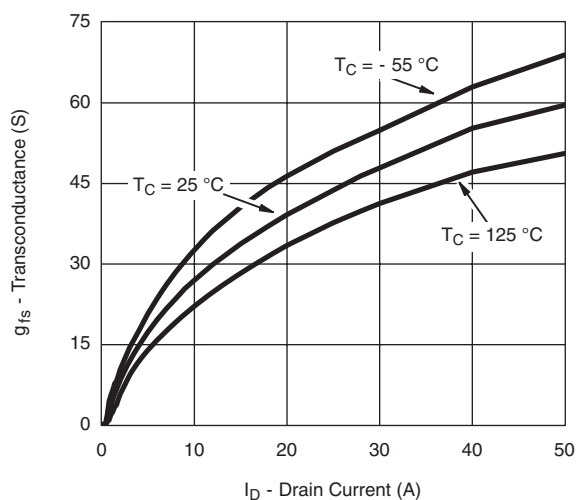
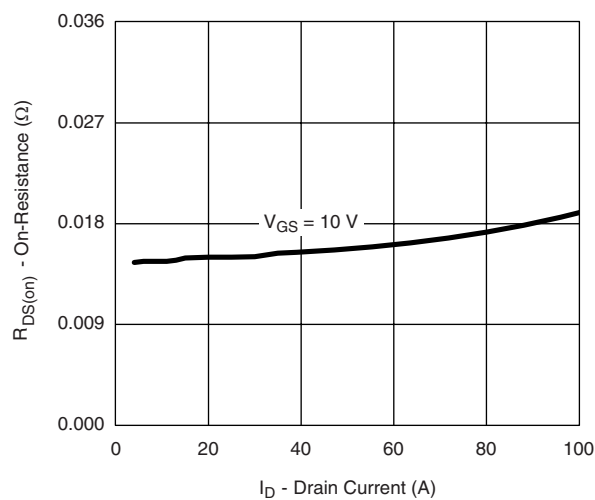
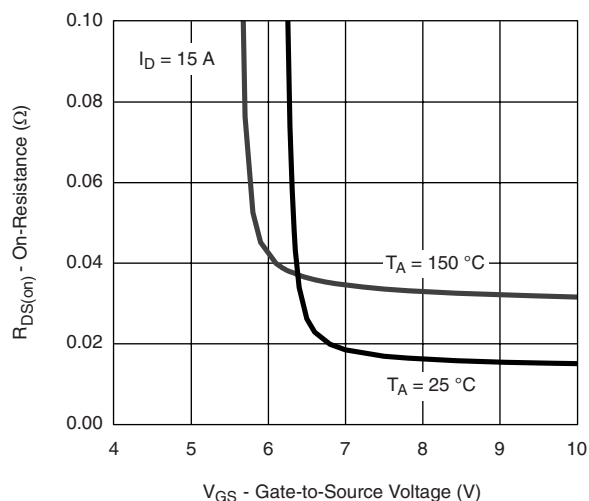
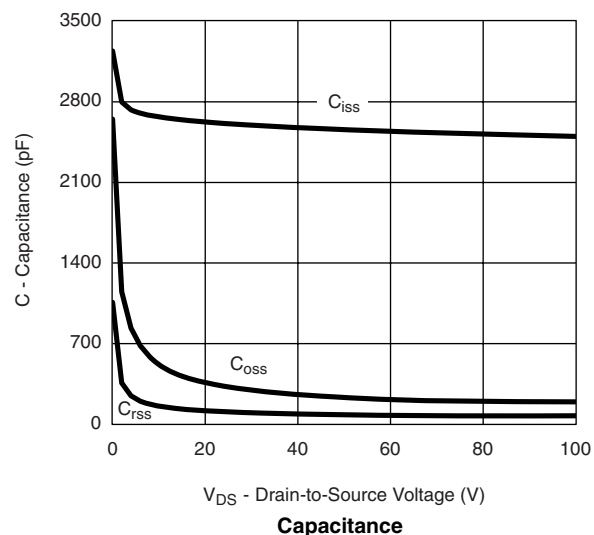
SPECIFICATIONS T <sub>J</sub> = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	100			V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA		110		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>			- 12.5		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.5		5	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C			50	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	50			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A		0.0125		Ω
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A		33		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V, f = 1 MHz		2800		pF
Output Capacitance	C <sub>oss</sub>			260		
Reverse Transfer Capacitance	C <sub>rss</sub>			100		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 50 A		48	75	nC
Gate-Source Charge	Q <sub>gs</sub>			16		
Gate-Drain Charge	Q <sub>gd</sub>			13		
Gate Resistance	R <sub>g</sub>	f = 1 MHz		1.6	2.5	Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 50 V, R <sub>L</sub> = 1.0 Ω I <sub>D</sub> ≅ 50 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		12	20	ns
Rise Time	t <sub>r</sub>			10	20	
Turn-Off Delay Time	t <sub>d(off)</sub>			18	35	
Fall Time	t <sub>f</sub>			8	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			50	A
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				100	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 15 A		0.85	1.5	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 50 A, dI/dt = 100 A/μs, T <sub>J</sub> = 25 °C		80	120	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			160	240	nC
Reverse Recovery Fall Time	t <sub>a</sub>			57		ns
Reverse Recovery Rise Time	t <sub>b</sub>			23		

Notes:

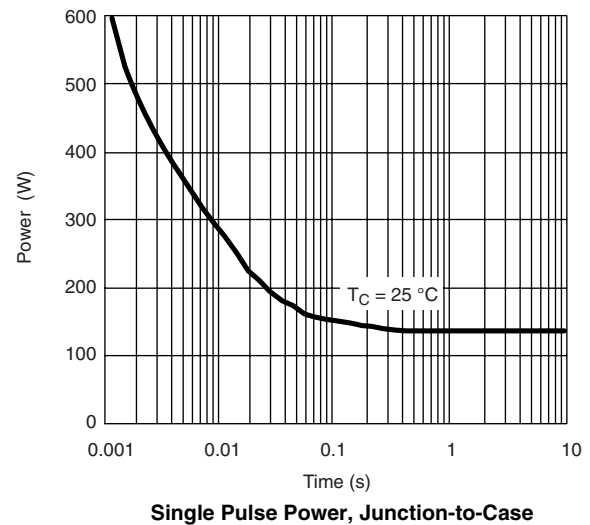
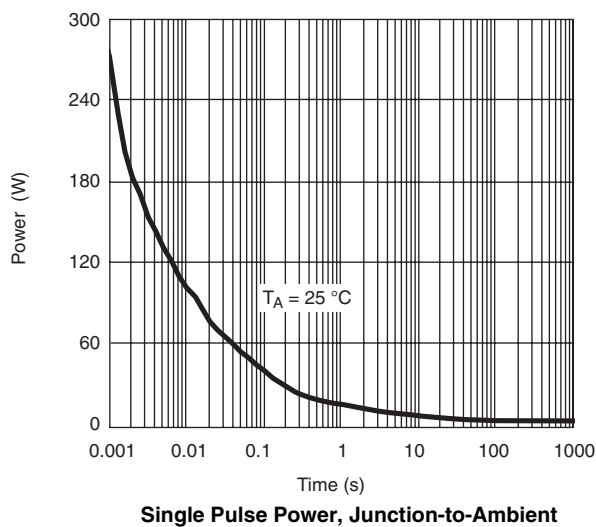
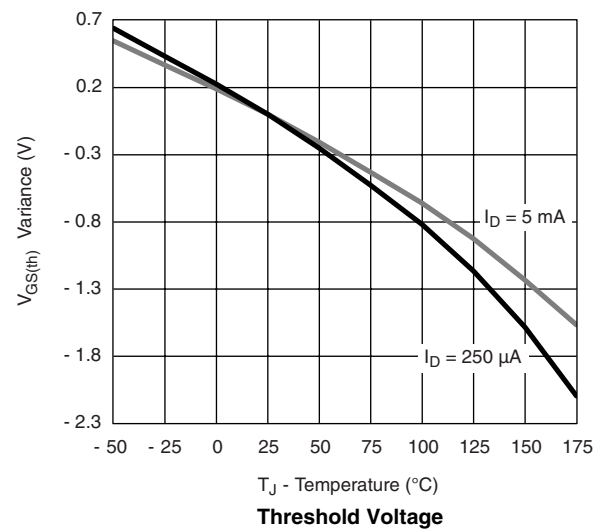
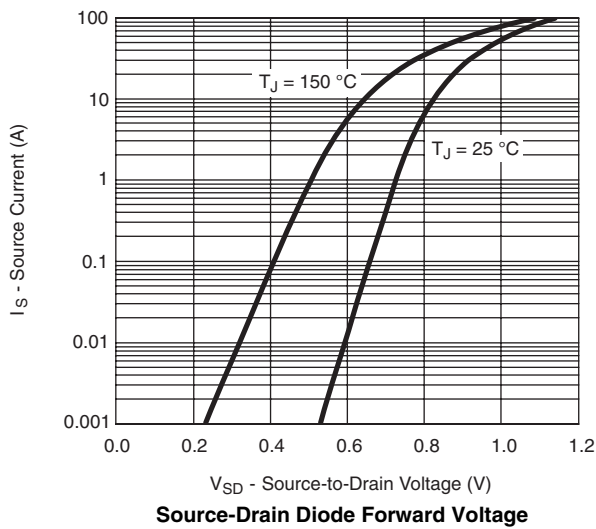
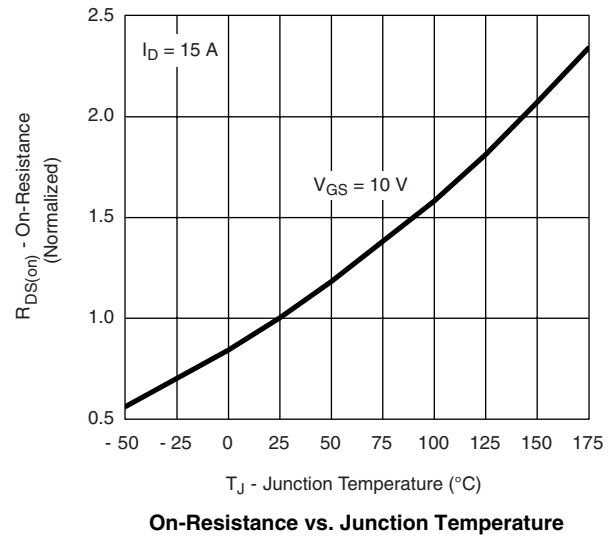
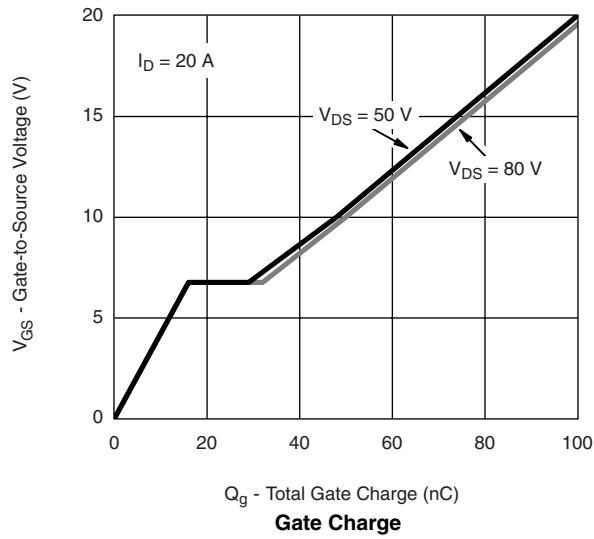
a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

b. Guaranteed by design, not subject to production testing.

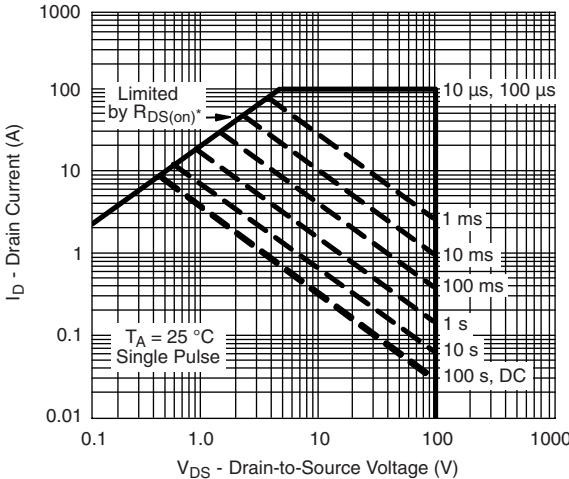
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

**Output Characteristics**

**Transfer Characteristics**

**Transconductance**

**On-Resistance vs. Drain Current**

**On-Resistance vs. Gate-to-Source Voltage**

**Capacitance**

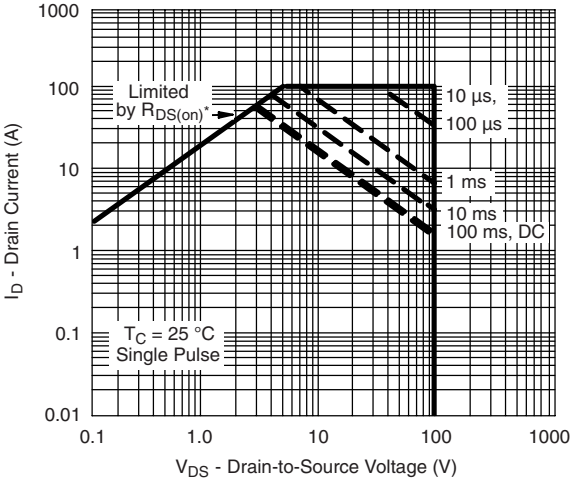
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



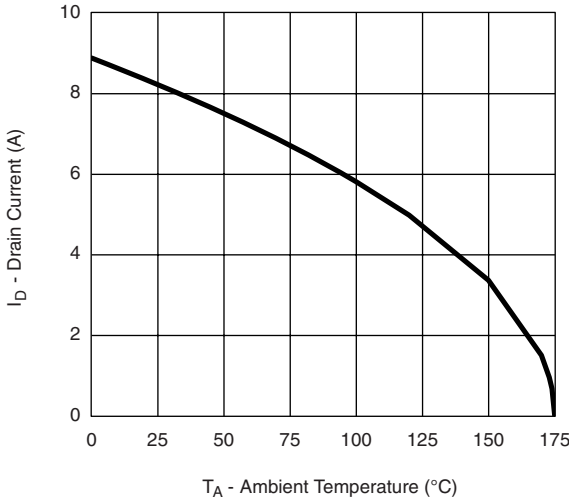
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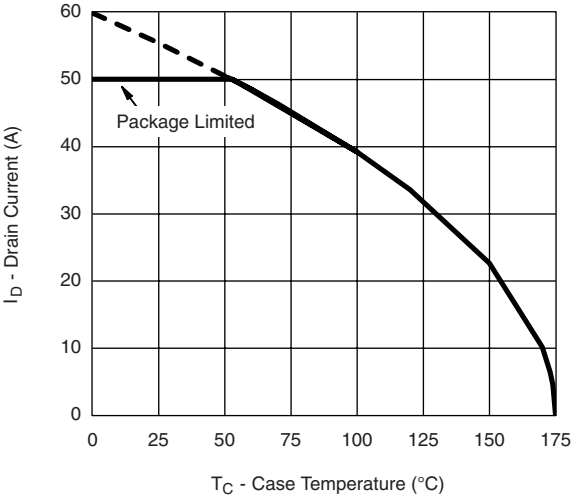
**Safe Operating Area, Junction-to-Ambient**



**Safe Operating Area, Junction-to-Case**

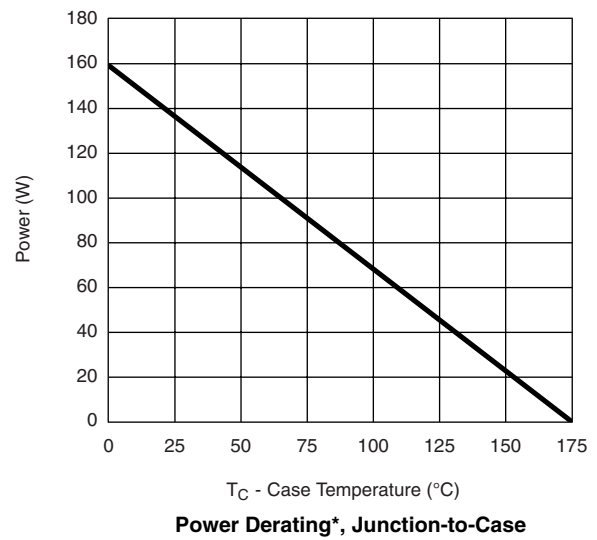
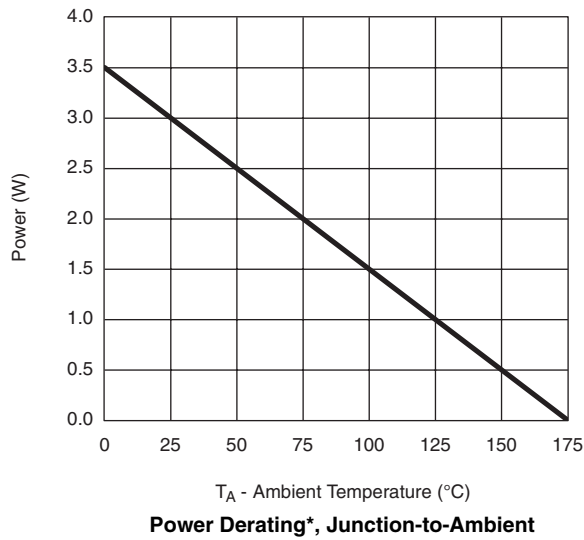


**Current Derating\*\*, Junction-to-Ambient**



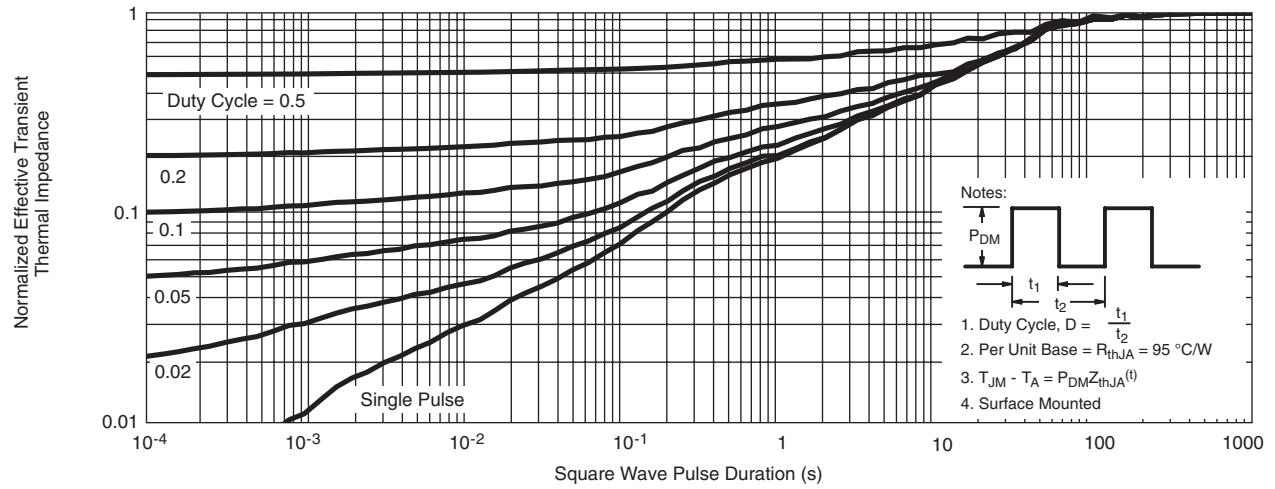
**Current Derating\*\*, Junction-to-Case**

\*\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 175\text{ }^{\circ}\text{C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

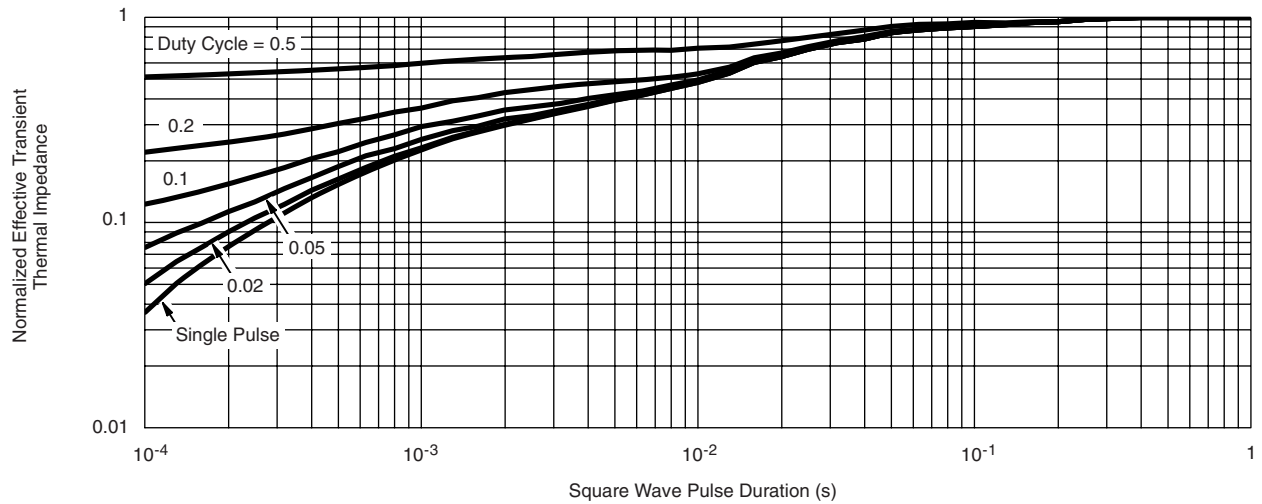
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\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 175$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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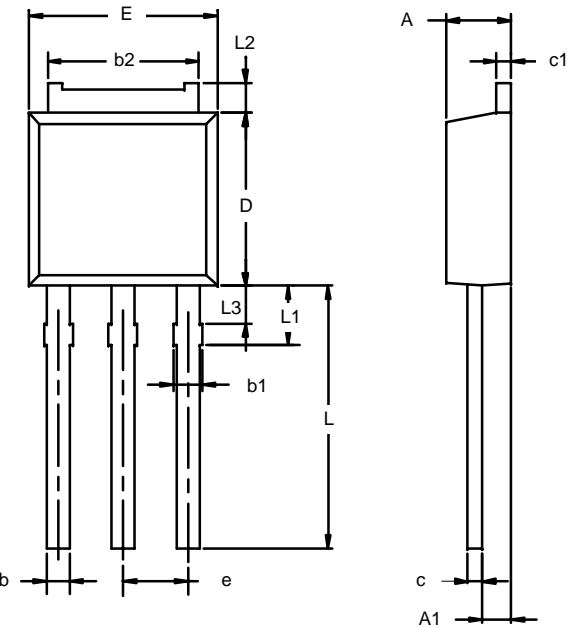


**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

TO-251AA (DPAK)



Note: Dimension L3 is for reference only.

Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	2.21	2.38	0.087	0.094
A1	0.89	1.14	0.035	0.045
b	0.71	0.89	0.028	0.035
b1	0.76	1.14	0.030	0.045
b2	5.23	5.43	0.206	0.214
c	0.46	0.58	0.018	0.023
c1	0.46	0.58	0.018	0.023
D	5.97	6.22	0.235	0.245
E	6.48	6.73	0.255	0.265
e	2.28 BSC		0.090 BSC	
L	3.89	9.53	0.153	0.375
L1	1.91	2.28	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.15	1.52	0.045	0.060



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