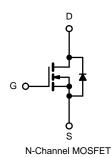


# IRFU2607ZPBF-VB Datasheet N-Channel 80 V (D-S) MOSFET

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$ Max.	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)		
	0.0064 at V <sub>GS</sub> = 10 V	75 <sup>a</sup>			
80	0.0070 at V <sub>GS</sub> = 6.0 V	65 <sup>a</sup>	17.1 nC		
	$0.0087$ at $V_{GS} = 4.5$ V	55 <sup>a</sup>			



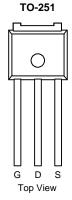
#### **FEATURES**

- Trench Power MOSFET
- 100 % R<sub>g</sub> and UIS Tested

#### **APPLICATIONS**

- · Primary Side Switching
- Synchronous Rectification
- DC/AC Inverters
- LED Backlighting





Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V <sub>DS</sub> 80	80	.,
Gate-Source Voltage		V <sub>GS</sub> ± 20		V
	T <sub>C</sub> = 25 °C		75 <sup>a</sup>	
Continuous Dunis Comment (T. 150 °C)	T <sub>C</sub> = 70 °C		62.7 <sup>a</sup>	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>A</sub> = 25 °C	I <sub>D</sub>	28.6 <sup>b, c</sup>	
	T <sub>A</sub> = 70 °C		24.9 <sup>b, c</sup>	_
Pulsed Drain Current (t = 100 μs)		I <sub>DM</sub>	350	A
Continuous Courses Drain Diada Current	T <sub>C</sub> = 25 °C		75ª	
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	l <sub>s</sub>	4.5 <sup>b, c</sup>	
Single Pulse Avalanche Current	. 0.4	I <sub>AS</sub>	30	
Single Pulse Avalanche Energy	L = 0.1 mH	E <sub>AS</sub>	45	mJ
	T <sub>C</sub> = 25 °C		62.5	
Maniana Dania Disainatian	T <sub>C</sub> = 70 °C		40	10/
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	5 <sup>b, c</sup>	W
	T <sub>A</sub> = 70 °C		3.2 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	00
Soldering Recommendations (Peak Temperatur	, and the second	260	°C	

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient <sup>b, f</sup>	t ≤ 10 s	$R_{thJA}$	20	25	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	$R_{thJC}$	1.5	2.0	- C/VV	

#### **Notes**

- a. Package limited.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. The TO-220 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- f. Maximum under steady state conditions is 70 °C/W.



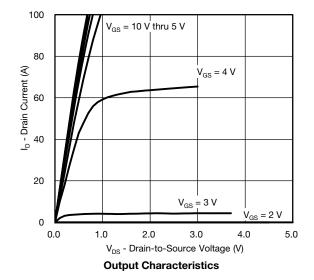
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	80			V	
V <sub>DS</sub> Temperature Coefficient	ΔVne/T <sub>1</sub>			37		1400	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA		- 6.1		mV/°C	
Gate-Source Threshold Voltage	V <sub>GS(th</sub> )	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	1.4		2.6	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
7 0	I <sub>DSS</sub>	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA	
Zero Gate Voltage Drain Current		V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			10		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	75			Α	
	, ,	$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$		0.0064			
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 6 \text{ V}, I_D = 15 \text{ A}$		0.0070		Ω	
	, ,	$V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$		0.0087		1	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	$V_{DS} = 10 \text{ V}, I_D = 20 \text{ A}$		60		S	
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>			1855			
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		950		рF	
Reverse Transfer Capacitance	C <sub>rss</sub>			76			
	Qg	$V_{DS} = 40 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$		35.5	54	nC	
Total Gate Charge		$V_{DS} = 40 \text{ V}, V_{GS} = 6 \text{ V}, I_D = 10 \text{ A}$		22	33		
				17.1	26		
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 40 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$		5.3			
Gate-Drain Charge	$Q_{gd}$			7.3			
Output Charge	Q <sub>oss</sub>	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$		57	86		
Gate Resistance	$R_g$	f = 1 MHz	0.5	1.3	2	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			12	24		
Rise Time	t <sub>r</sub>	$V_{DD} = 40 \text{ V}, R_L = 4 \Omega$		8	16		
Turn-Off DelayTime	t <sub>d(off)</sub>	$I_D \cong 10^{\circ} \text{A}, V_{GEN} = 10^{\circ} \text{V}, R_g = 1^{\circ} \Omega$		32	64		
Fall Time	t <sub>f</sub>			7	14		
Turn-On Delay Time	t <sub>d(on)</sub>			14	28	ns	
Rise Time	t <sub>r</sub>	$V_{DD} = 40 \text{ V}, R_{L} = 4 \Omega$		11	22	- - -	
Turn-Off DelayTime	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 6.0 \text{ V}, R_g = 1 \Omega$		30	60		
Fall Time	t <sub>f</sub>			8	16		
<b>Drain-Source Body Diode Characteristic</b>	s						
Continuous Source-Drain Diode Current	Is	T <sub>C</sub> = 25 °C			75	۸	
Pulse Diode Forward Current (t = 100 μs)	I <sub>SM</sub>				150	A	
Body Diode Voltage	$V_{SD}$	I <sub>S</sub> = 5 A		0.76	1.1	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			38	75	ns	
Body Diode Reverse Recovery Charge	$Q_{rr}$	1 10 A 11/14 100 A/ - T 05 20		36	70	nC	
Reverse Recovery Fall Time $t_a$ $I_F = 10 \text{ A, dI/dt} = 100 \text{ A/µs, T}$		$I_F = 10 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$		19			
Reverse Recovery Rise Time	t <sub>b</sub>			19		ns	

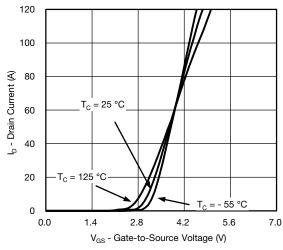
#### Notes

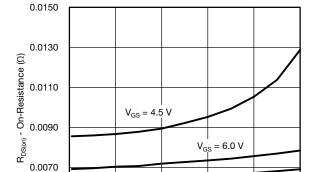
- a. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

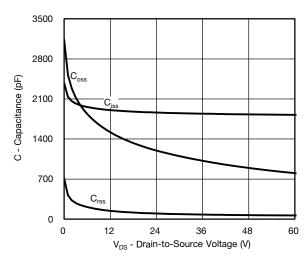


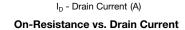






**Transfer Characteristics** 



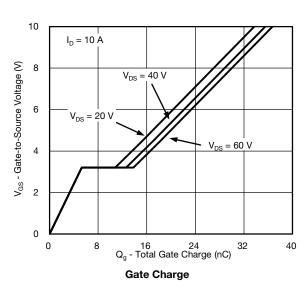


40

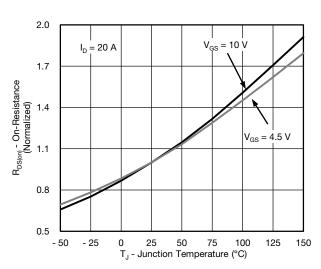
 $V_{GS} = 10 \text{ V}$ 

100

80



Capacitance



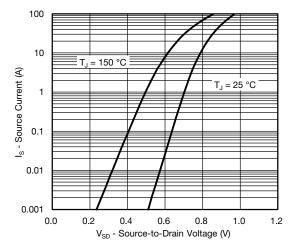
On-Resistance vs. Junction Temperature

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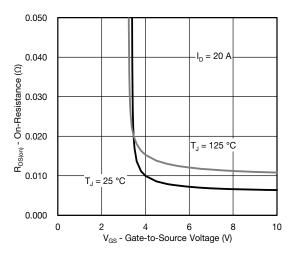
0.0050

0

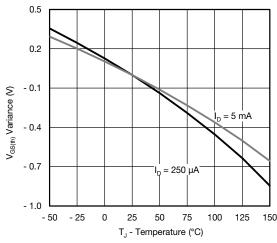




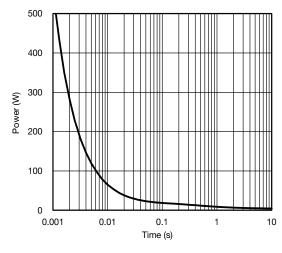
Source-Drain Diode Forward Voltage



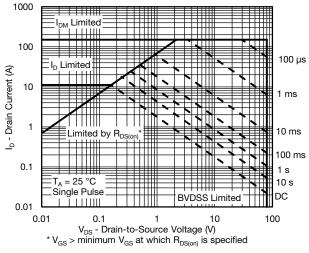
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

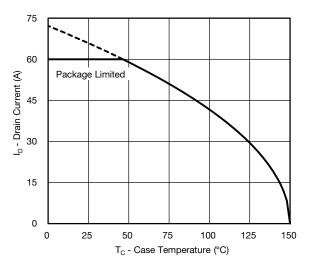


Single Pulse Power, Junction-to-Ambient

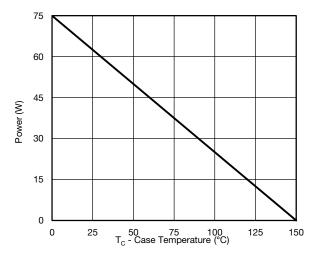


Safe Operating Area, Junction-to-Ambient

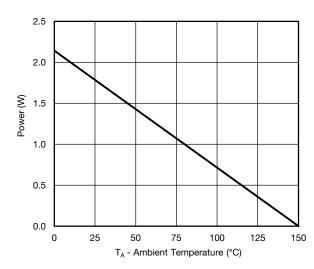




#### **Current Derating\***



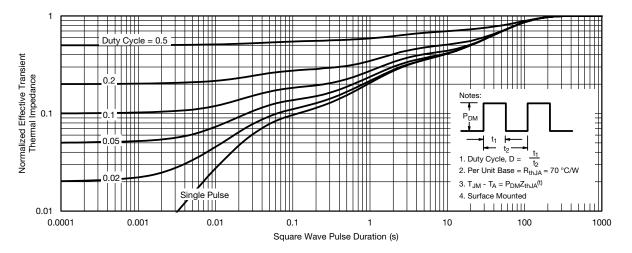




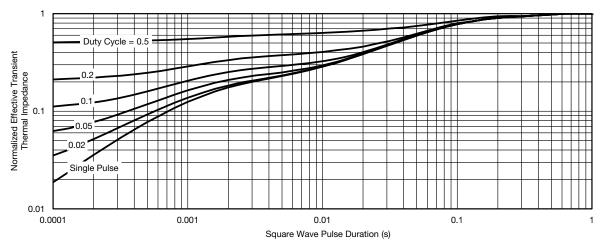
Power, Junction-to-Ambient

<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max.)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





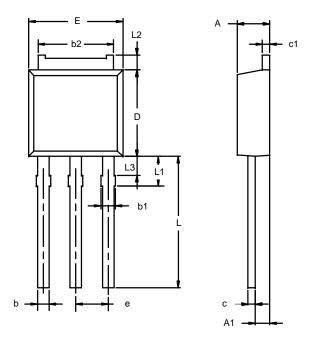
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case



# TO-251AA (DPAK)



Note: Dimension L3 is	s for reference only.
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	MILLIM	IETERS	INC	HES
Dim	Min	Max	Min	Max
Α	2.21	2.38	0.087	0.094
A1	0.89	1.14	0.035	0.045
b	0.71	0.89	0.028	0.035
b1	0.76	1.14	0.030	0.045
b2	5.23	5.43	0.206	0.214
С	0.46	0.58	0.018	0.023
с1	0.46	0.58	0.018	0.023
D	5.97	6.22	0.235	0.245
Е	6.48	6.73	0.255	0.265
е	2.28 BSC		0.090 BSC	
L	3.89	9.53	0.153	0.375
L1	1.91	2.28	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.15	1.52	0.045	0.060

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