STW45NM50FD-VB Datasheet

N-Channel 600V(D-S) Super Junction Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	600	
$R_{DS(on)}$ at 25 °C (Ω)	V_{GS} = 10 V	0.056
Q_g max. (nC)	228	
Q_{gs} (nC)	32	
Q_{gd} (nC)	62	
Configuration	Single	

FEATURES

- Fast body diode MOSFET using E series technology
- Reduced t_{rr}, Q_{rr}, and I_{RRM}
- Low figure-of-merit (FOM) R_{on} x Q_g
- Low input capacitance (C_{iss})
- Increased robustness due to low Q_{rr}
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)

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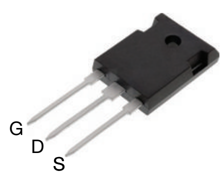
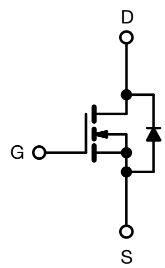




N-Channel MOSFET

APPLICATIONS

- Telecommunications
  - Server and telecom power supplies
- Lighting
  - High-intensity lighting (HID)
  - Light emitting diodes (LEDs)
- Consumer and computing
  - ATX power supplies
- Industrial
  - Welding
  - Battery chargers
- Renewable energy
  - Solar (PV inverters)
- Switching mode power supplies (SMPS)
- Applications using the following topologies
  - LLC
  - Phase shifted bridge (ZVS)
  - 3-level inverter
  - AC/DC bridge

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

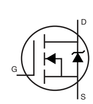
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	600	V
Gate-Source Voltage			V_{GS}	± 30	
Continuous Drain Current (T_J = 150 °C)	V_{GS} at 10 V	T_C = 25 °C	I_D	47	A
		T_C = 100 °C		29	
Pulsed Drain Current [a]			I_{DM}	138	
Linear Derating Factor				3	W/°C
Single Pulse Avalanche Energy [b]			E_{AS}	1500	mJ
Maximum Power Dissipation			P_D	379	W
Operating Junction and Storage Temperature Range			T_J, T_{stg}	-55 to +150	°C
Drain-Source Voltage Slope	T_J = 125 °C		dV/dt	70	V/ns
Reverse Diode dV/dt [d]				50	
Soldering Recommendations (Peak Temperature) [c]	for 10 s			300	°C

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature
b. V_{DD} = 50 V, starting T_J = 25 °C, L = 73.5 mH, R_g = 25 Ω, I_{AS} = 6.4 A
c. 1.6 mm from case
d. $I_{SD} \leq I_D$, dI/dt = 500 A/μs, starting T_J = 25 °C

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.33	°C/W

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	600	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-		-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
		V_{GS} = ± 30 V	-	-	± 1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 480 V, V_{GS} = 0 V	-	-	1	μA
		V_{DS} = 480 V, V_{GS} = 0 V, T_J = 125 °C	-	-	500	μA
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 24 A	-	0.056	-	Ω
Forward Transconductance	g_{fs}	V_{DS} = 30 V, I_D = 24 A	-	17	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	-	5000	-	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	-	220	-	pF
Reverse Transfer Capacitance	C_{rss}	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	-	7	-	pF
Effective Output Capacitance, Energy Related [a]	$C_{o(er)}$	V_{DS} = 0 V to 480 V, V_{GS} = 0 V	-	172	-	pF
Effective Output Capacitance, Time Related [b]	$C_{o(tr)}$	V_{DS} = 0 V to 480 V, V_{GS} = 0 V	-	634	-	pF
Total Gate Charge	Q_g	V_{GS} = 10 V, I_D = 24 A, V_{DS} = 480 V	-	152	228	nC
Gate-Source Charge	Q_{gs}	V_{GS} = 10 V, I_D = 24 A, V_{DS} = 480 V	-	32	-	nC
Gate-Drain Charge	Q_{gd}	V_{GS} = 10 V, I_D = 24 A, V_{DS} = 480 V	-	62	-	nC
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 480 V, I_D = 24 A, V_{GS} = 10 V, R_g = 4.4 Ω	-	30	60	ns
Rise Time	t_r	V_{DD} = 480 V, I_D = 24 A, V_{GS} = 10 V, R_g = 4.4 Ω	-	56	84	ns
Turn-Off Delay Time	$t_{d(off)}$	V_{DD} = 480 V, I_D = 24 A, V_{GS} = 10 V, R_g = 4.4 Ω	-	91	137	ns
Fall Time	t_f	V_{DD} = 480 V, I_D = 24 A, V_{GS} = 10 V, R_g = 4.4 Ω	-	56	84	ns
Gate Input Resistance	R_g	f = 1 MHz, open drain	0.2	0.46	1.0	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	47	A
Pulsed Diode Forward Current	I_{SM}		-	-	138	A
Diode Forward Voltage	V_{SD}	T_J = 25 °C, I_S = 24 A, V_{GS} = 0 V	-	0.9	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = I_S = 24 A, dI/dt = 100 A/μs, V_R = 400 V	-	199	398	ns
Body Diode Reverse Recovery Charge	Q_{rr}	T_J = 25 °C, I_F = I_S = 24 A, dI/dt = 100 A/μs, V_R = 400 V	-	1.4	2.8	μC
Reverse Recovery Current	I_{RRM}	T_J = 25 °C, I_F = I_S = 24 A, dI/dt = 100 A/μs, V_R = 400 V	-	13.2	-	A

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}

b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

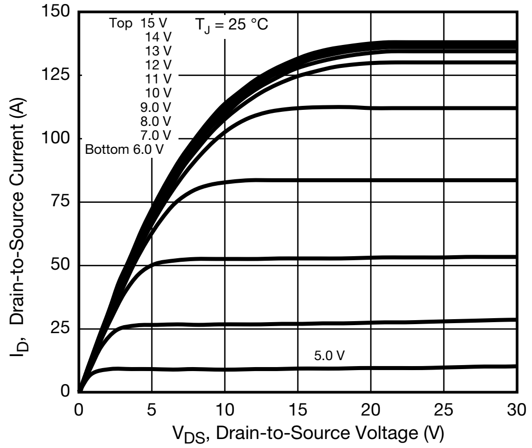


Fig. 1 - Typical Output Characteristics

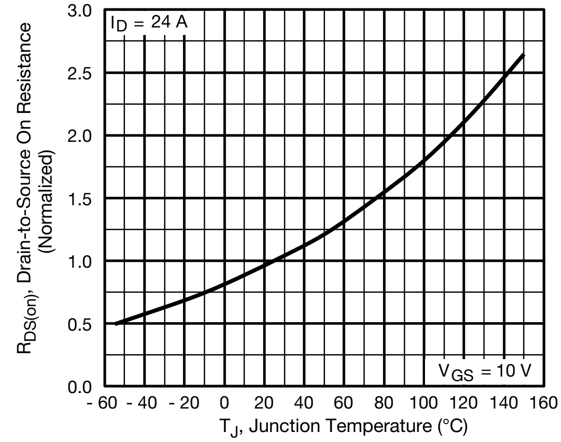


Fig. 4 - Normalized On-Resistance vs. Temperature

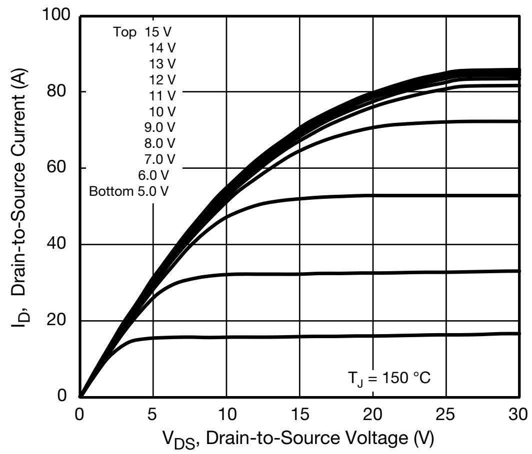


Fig. 2 - Typical Output Characteristics

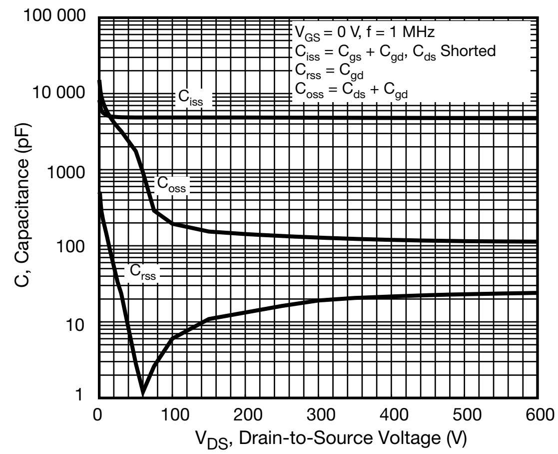


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

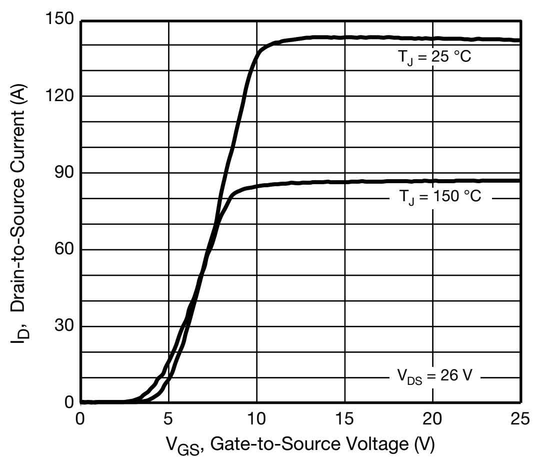


Fig. 3 - Typical Transfer Characteristics

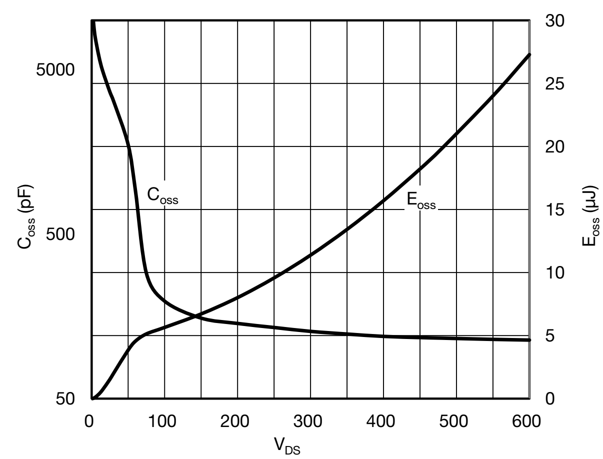


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

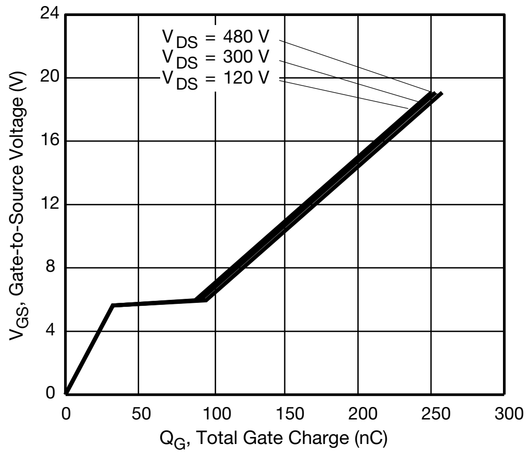


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

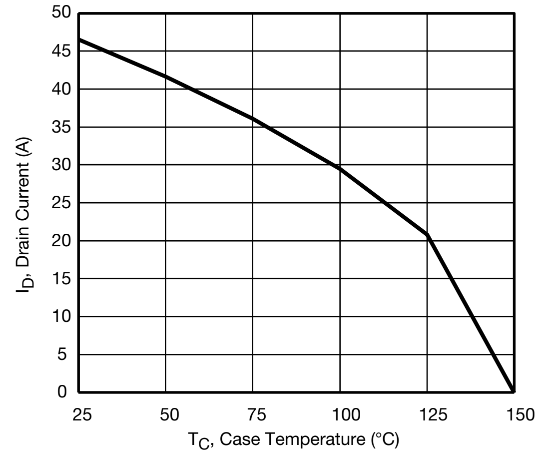


Fig. 10 - Maximum Drain Current vs. Case Temperature

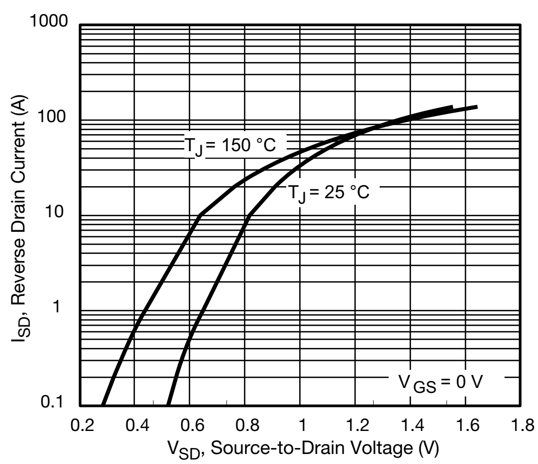


Fig. 8 - Typical Source-Drain Diode Forward Voltage

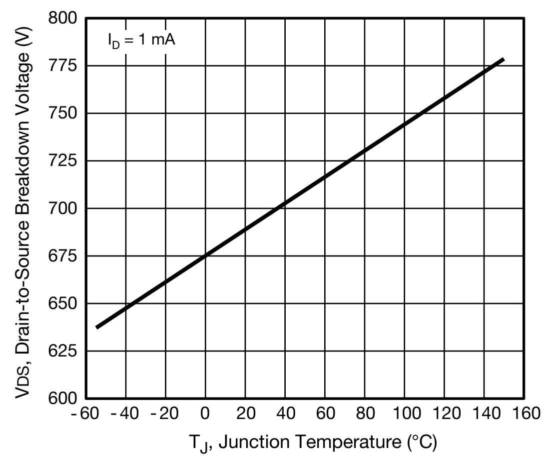
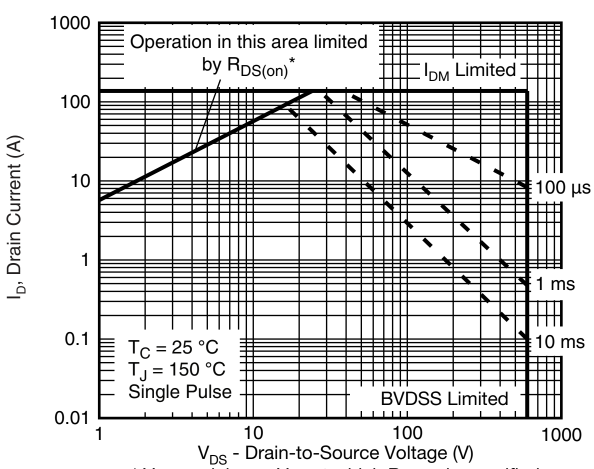


Fig. 11 - Temperature vs. Drain-to-Source Voltage



* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Fig. 9 - Maximum Safe Operating Area

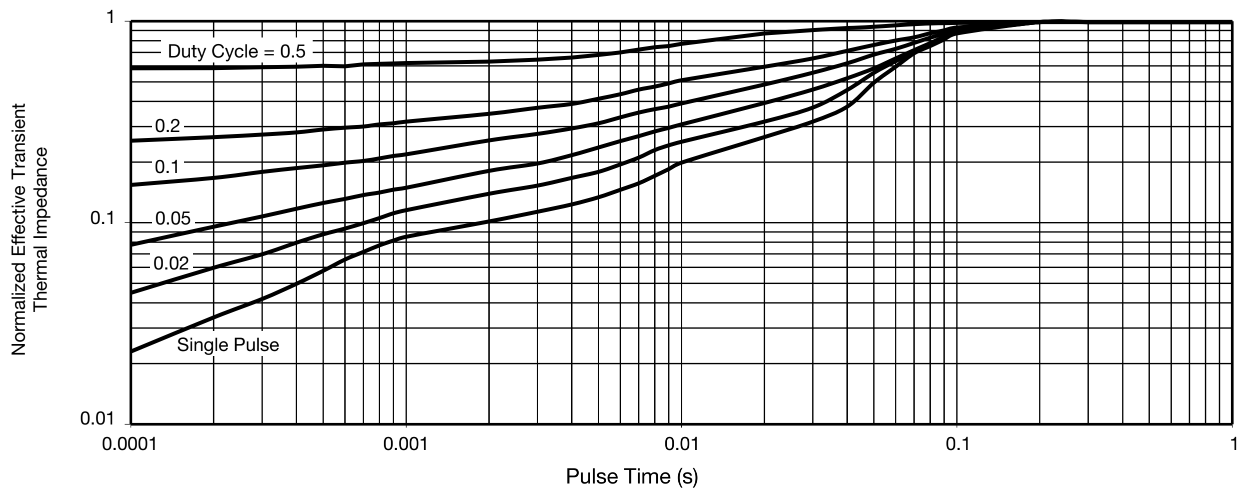


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

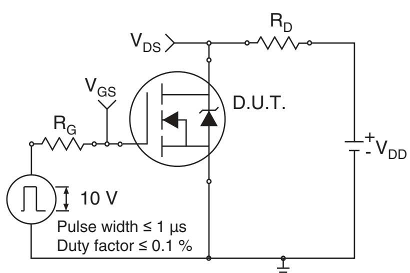


Fig. 13 - Switching Time Test Circuit

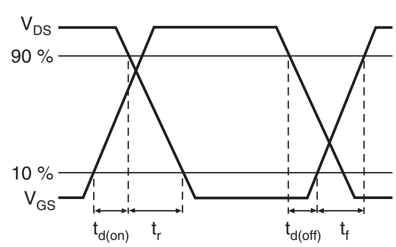


Fig. 14 - Switching Time Waveforms

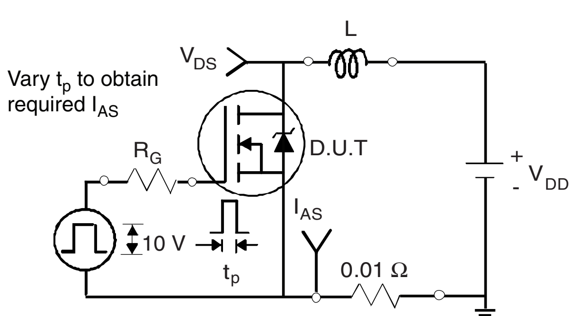


Fig. 15 - Unclamped Inductive Test Circuit

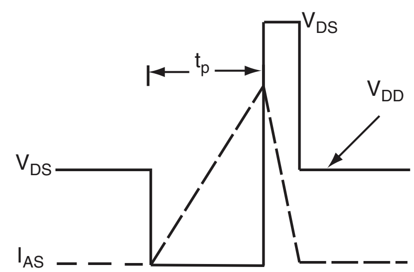


Fig. 16 - Unclamped Inductive Waveforms

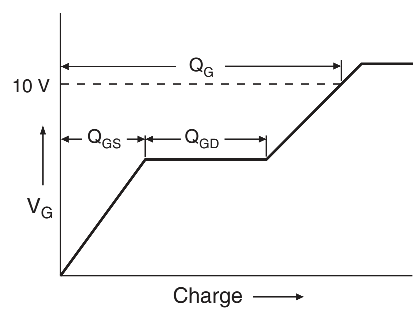


Fig. 17 - Basic Gate Charge Waveform

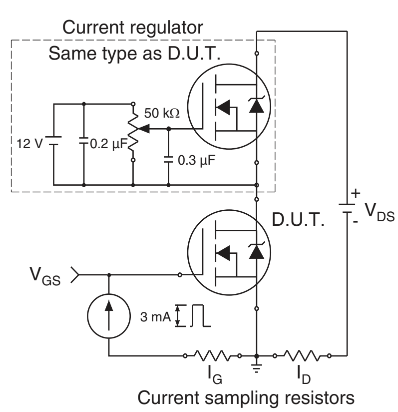
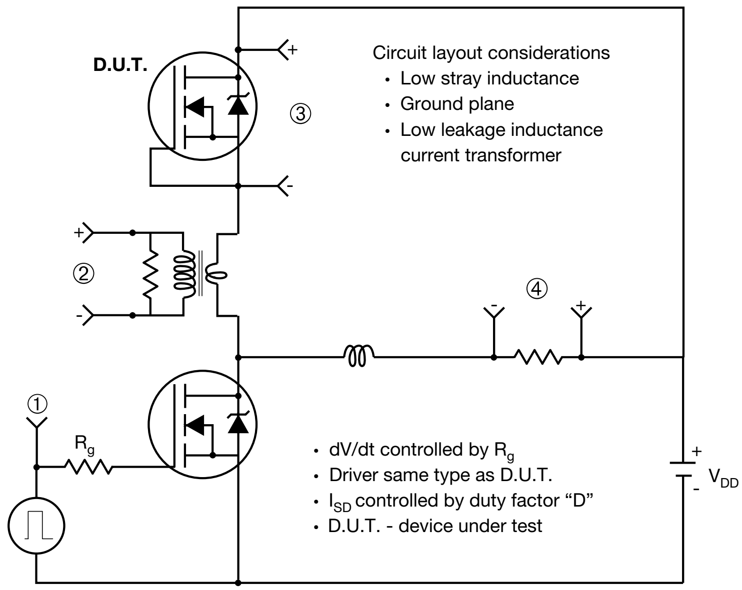
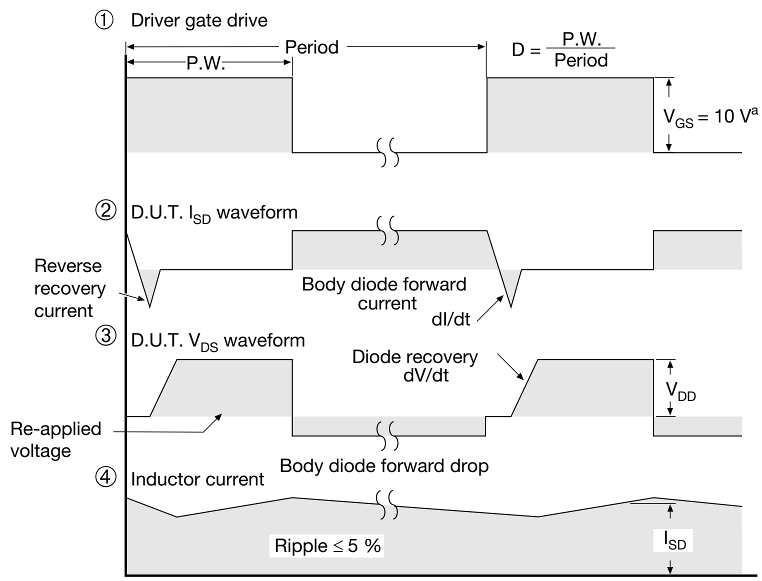


Fig. 18 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit





Note

a. V_{GS} = 5 V for logic level devices

Fig. 18 - For N-Channel

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