

NVHL040N120SC1-VB Datasheet

N-Channel 1200V (D-S) SiC Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	1200	
$R_{DS(on)}$ at 25 °C (Ω)	$V_{GS} = 18V$	0.040
Q_g (nC)	101	

FEATURES

- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)

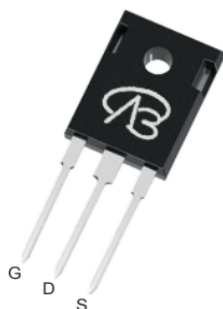


RoHS

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- DC/DC converter

TO-247



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)						
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			V _{DS}	1200	V	
Gate-Source Voltage			V _{GS}	-10 / +22		
Continuous Drain Current (T _J = 150 °C)	V _{GS} at 18V	T _C = 25 °C	I _D	60	A	
		T _C = 100 °C		42		
Pulsed Drain Current ^a			I _{DM}	160		
Linear Derating Factor				2.1	W/°C	
Single Pulse Avalanche Energy ^b			E _{AS}	1200	mJ	
Maximum Power Dissipation			P _D	320	W	
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +175	°C	
Drain-Source Voltage Slope		T _J = 125 °C		dV/dt	50	V/ns
Reverse Diode dV/dt ^d			15			
Soldering Recommendations (Peak Temperature) ^c		for 10 s			260	°C

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 100\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 30\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 9\text{ A}$.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, $dI/dt = 100\text{ A}/\mu\text{s}$, starting $T_J = 25\text{ }^\circ\text{C}$.

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.47	

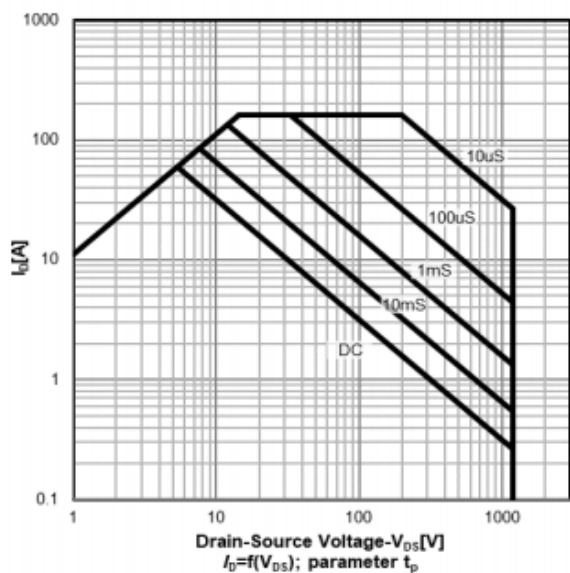
SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	1200	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C , $I_D = 1\text{ mA}$	-	0.70	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 10\text{ mA}$	2.5	-	4.5	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = +22\text{ V}$	-	-	100	nA
		$V_{GS} = -10\text{ V}$	-	-	100	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 1200\text{ V}$, $V_{GS} = 0\text{ V}$	-	10	-	μA
		$V_{DS} = 1200\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ °C}$	-	-	100	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 18\text{ V}$, $I_D = 30\text{ A}$	-	0.040	-	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 0\text{ V}$, $I_D = 30\text{ A}$	-	16	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 800\text{ V}$, $f = 1\text{ MHz}$	-	2200	-	pF
Output Capacitance	C_{oss}		-	123	-	
Reverse Transfer Capacitance	C_{rss}		-	10	-	
Effective Output Capacitance, Energy Related ^a	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 800\text{ V}$, $V_{GS} = 0\text{ V}$	-	156	-	
Effective Output Capacitance, Time Related ^b	$C_{o(tr)}$		-	268	-	
Total Gate Charge	Q_g	$V_{GS} = -5/18\text{ V}$, $I_D = 20\text{ A}$, $V_{DS} = 800\text{ V}$	-	101	-	nC
Gate-Source Charge	Q_{gs}		-	29	-	
Gate-Drain Charge	Q_{gd}		-	33	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 800\text{ V}$, $I_D = 20\text{ A}$, $V_{GS} = -5/18\text{ V}$, $R_g = 2\text{ Ω}$	-	18	25	ns
Rise Time	t_r		-	24	55	
Turn-Off Delay Time	$t_{d(off)}$		-	80	-	
Fall Time	t_f		-	12	-	
Gate Input Resistance	R_g	$f = 1\text{ MHz}$, open drain	-	3.2	-	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	60	A
Pulsed Diode Forward Current	I_{SM}		-	-	160	
Diode Forward Voltage	V_{SD}	$T_J = 25\text{ °C}$, $I_S = 30\text{ A}$, $V_{GS} = 0$	-	-	4.1	V
Reverse Recovery Time	t_{rr}	$T_J = 25\text{ °C}$, $I_F = I_S = 30\text{ A}$, $di/dt = 1000\text{ A/μs}$, $V_R = 800\text{ V}$	-	47	-	ns
Reverse Recovery Charge	Q_{rr}		-	220	-	μC
Reverse Recovery Current	I_{RRM}		-	60	-	A

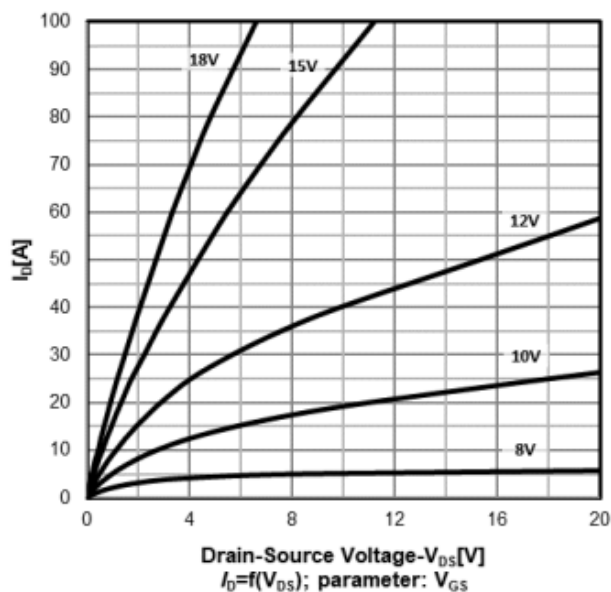
Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
 b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .

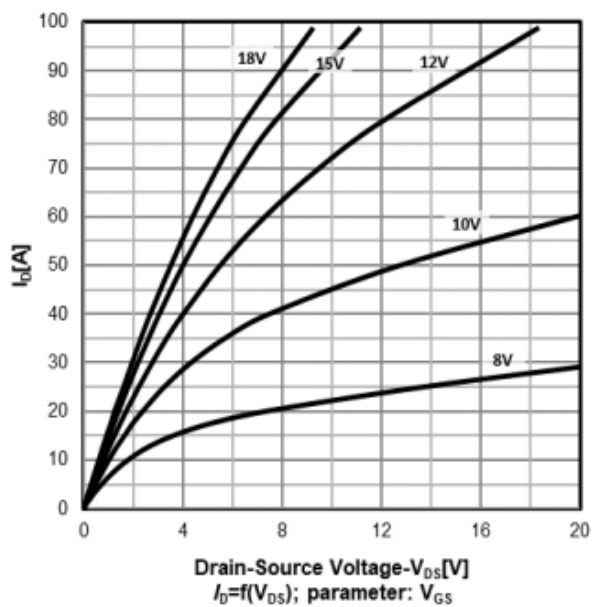
Safe operating area $T_c=25^\circ\text{C}$
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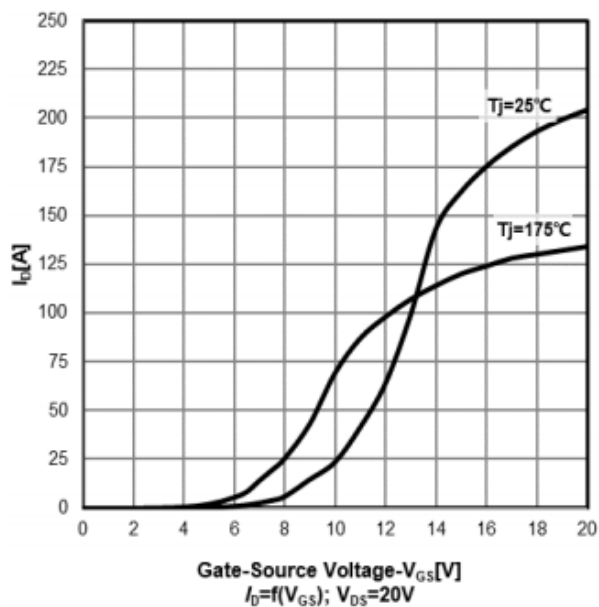
On-Region characteristics $T_j=25^\circ\text{C}$



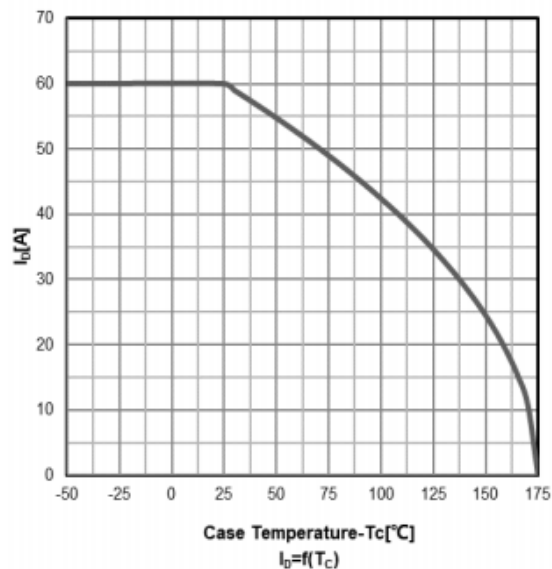
On-Region characteristics $T_j=175^\circ\text{C}$



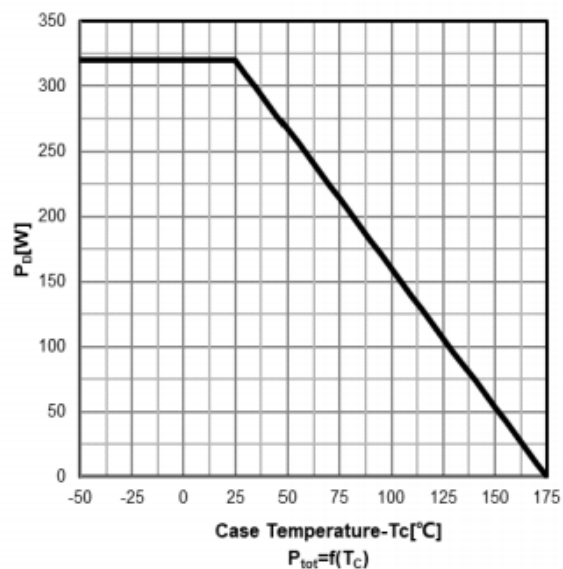
Transfer characteristics



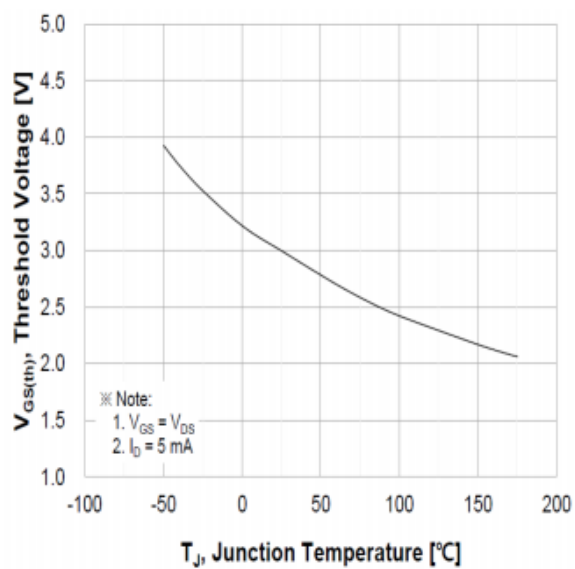
Drain current vs temperature



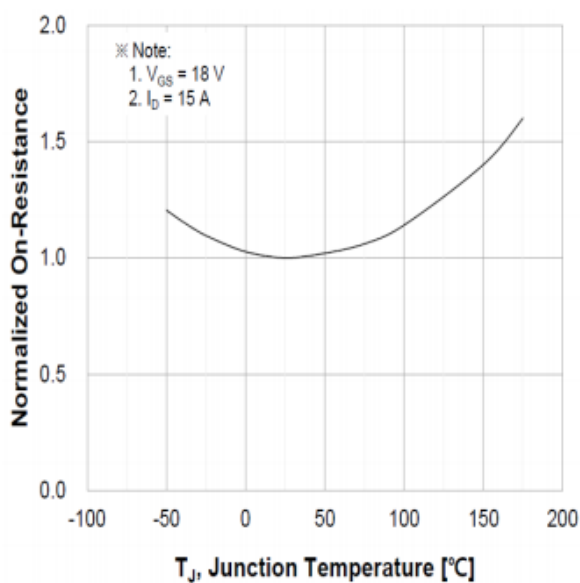
Power dissipation



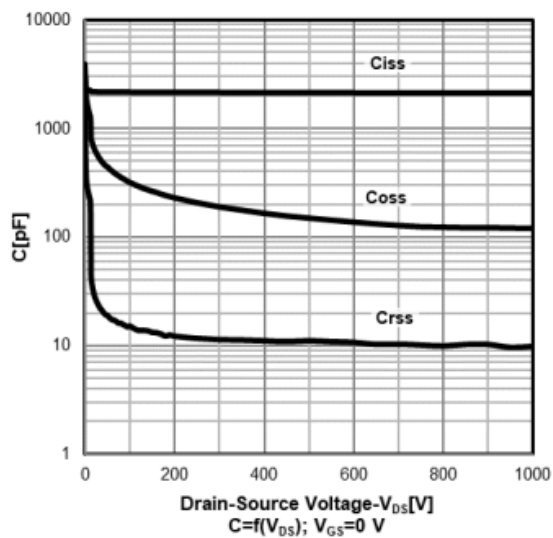
Threshold voltage vs temperature



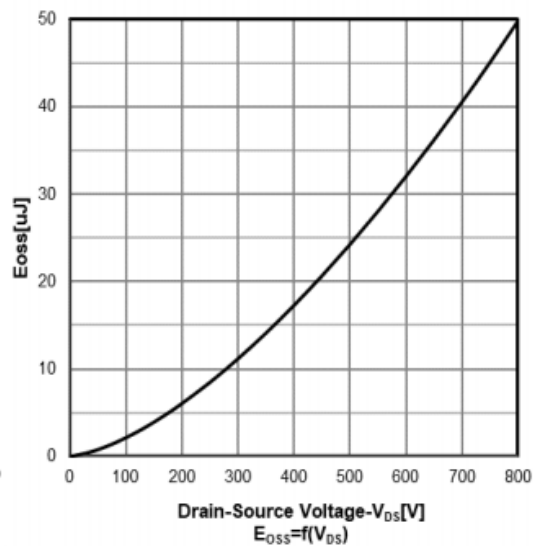
Normalized On-resistance vs temperature



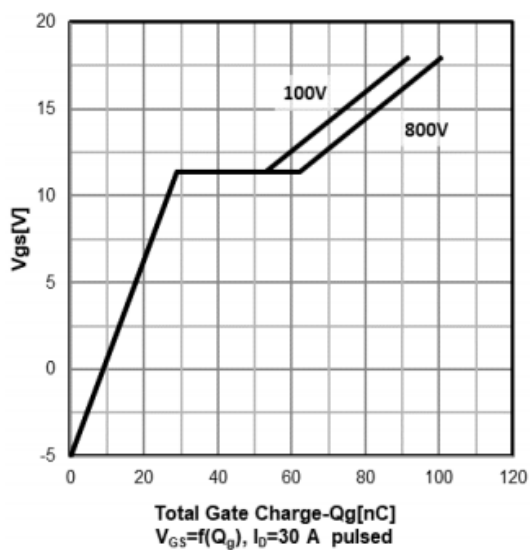
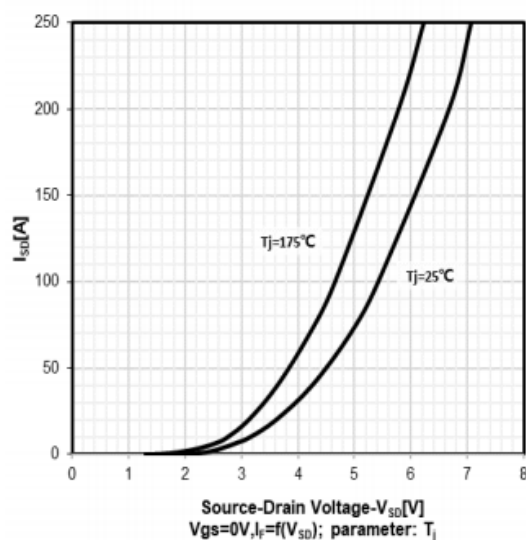
Typ. capacitances



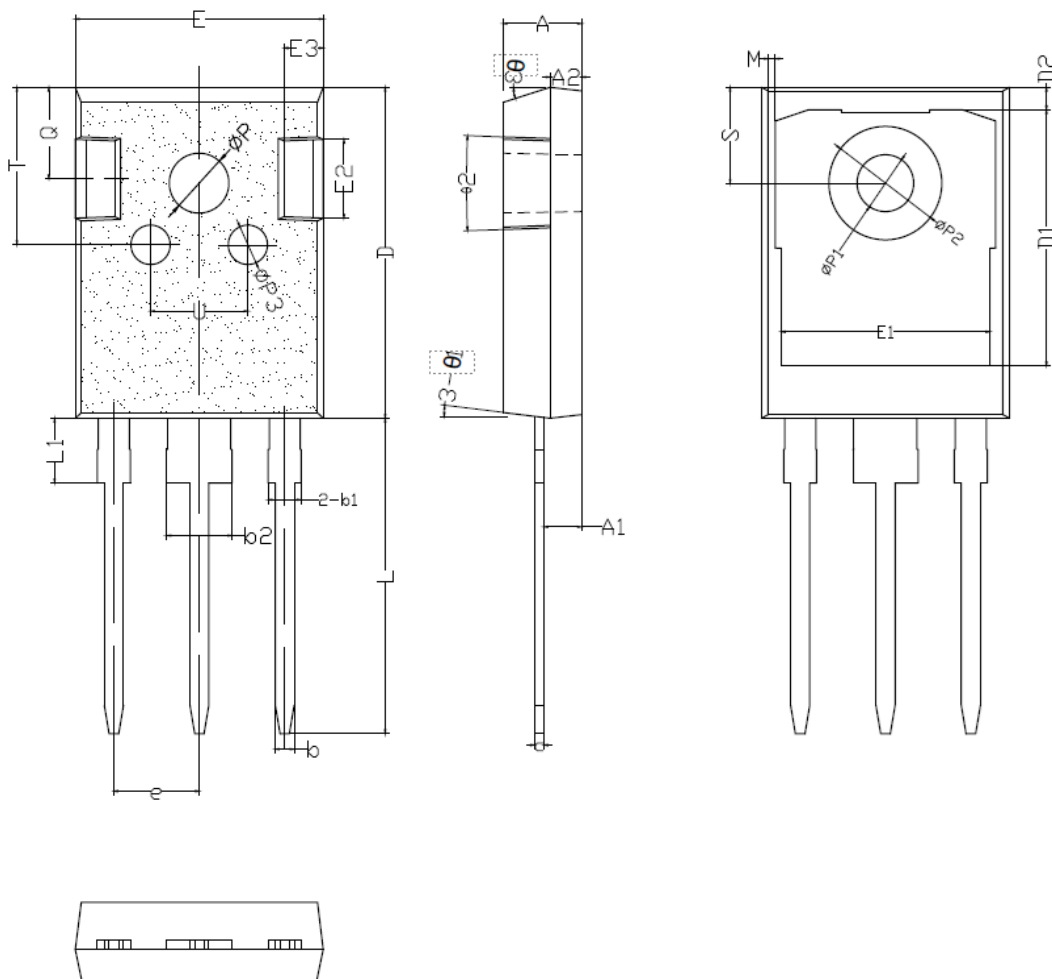
Coss stored energy



Typ. gate charge characteristics

Diode forward voltage characteristics
 $T_J=25^\circ\text{C}/175^\circ\text{C}$ 

TO-247 PACKAGE OUTLINE DIMENSIONS



SYMBOL	mm		
	MIN	NOM	MAX
*A	4.90	5.00	5.10
*A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
*b	1.15	1.20	1.25
*b1	1.95	2.10	2.25
*b2	2.95	3.10	3.25
*c	0.55	0.60	0.65
*D	20.90	21.00	21.10
D1	16.35	16.55	16.75
D2	1.05	1.20	1.35

*E	15.70	15.80	15.90
E1	13.10	13.25	13.40
E2	4.85	4.95	5.10
E3	2.40	2.50	2.60
*e	5.40	5.44	5.48
*L	19.80	19.98	20.15
*L1	-	-	4.30
*ΦP	3.40	3.50	3.60
*ΦP1	6.90	7.10	7.30
ΦP2	2.40	2.50	2.60
ΦP3	2.40	2.50	2.60
Q	5.60	5.80	6.00
*S	6.05	6.15	6.25
T	9.80	10.00	10.20
U	6.00	6.20	6.40
θ1	5°	7°	9°
θ2	1°	3°	5°
θ3	13°	15°	17°

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