

IPW65R099C6-VB Datasheet

Power MOSFET

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	750	
$R_{DS(on)}$ typ. (Ω) at 25 °C	$V_{GS} = 10$ V	0.070
Q_g max. (nC)	278	
Q_{gs} (nC)	46	
Q_{gd} (nC)	76	
Configuration	Single	

FEATURES

- Fast body diode MOSFET using E series technology
- Reduced t_{rr} , Q_{rr} , and I_{RRM}
- Low figure-of-merit (FOM): $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Low switching losses due to reduced Q_{rr}
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)

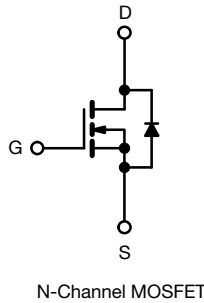
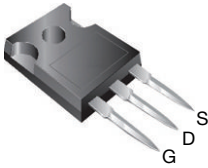


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APPLICATIONS

- Telecommunications
 - Server and telecom power supplies
- Lighting
 - High intensity discharge (HID)
 - Light emitting diodes (LEDs)
- Consumer and computing
 - ATX power supplies
- Industrial
 - Welding
 - Battery chargers
- Renewable energy
 - Solar (PV inverters)
- Switch mode power supplies (SMPS)
- Applications using the following topologies
 - LLC
 - Phase shifted bridge (ZVS)
 - 3-level inverter
 - AC/DC bridge

TO-247AC

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	700	V
Gate-Source Voltage			V_{GS}	± 30	
Continuous Drain Current ($T_J = 150\text{ }^{\circ}\text{C}$)	V_{GS} at 10 V	$T_C = 25\text{ }^{\circ}\text{C}$	I_D	46	A
		$T_C = 100\text{ }^{\circ}\text{C}$		29	
Pulsed Drain Current ^a			I_{DM}	154	
Linear Derating Factor				3.3	W/ $^{\circ}\text{C}$
Single Pulse Avalanche Energy ^b			E_{AS}	596	mJ
Maximum Power Dissipation			P_D	427	W
Operating Junction and Storage Temperature Range			T_J, T_{stg}	-55 to +150	$^{\circ}\text{C}$
Drain-Source Voltage Slope	$T_J = 125\text{ }^{\circ}\text{C}$		dV/dt	70	V/ns
Reverse Diode dV/dt ^d		5.3			
Soldering Recommendations (Peak Temperature) ^c	for 10 s			300	$^{\circ}\text{C}$

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature.
 b. $V_{DD} = 140$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 6.5$ A.
 c. 1.6 mm from case.
 d. $I_{SD} \leq I_D$, $dI/dt = 100$ A/ μ s, starting $T_J = 25$ °C.

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.3	

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	700	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^{\circ}\text{C}$, $I_D = 10\text{ mA}$	-	0.75	-	V/ $^{\circ}\text{C}$
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
		$V_{GS} = \pm 30\text{ V}$	-	-	± 1	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 560\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 560\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}$	-	-	500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 22\text{ A}$	-	0.070	-	Ω
Forward Transconductance ^a	g_{fs}	$V_{DS} = 30\text{ V}$, $I_D = 22\text{ A}$	-	17	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$	-	5892	-	pF
Output Capacitance	C_{oss}		-	244	-	
Reverse Transfer Capacitance	C_{rss}		-	4	-	
Effective Output Capacitance, Energy Related ^a	$C_{o(er)}$	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ V to } 560\text{ V}$	-	739	-	
Effective Output Capacitance, Time Related ^b	$C_{o(tr)}$		-	178	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$, $I_D = 22\text{ A}$, $V_{DS} = 560\text{ V}$	-	185	278	nC
Gate-Source Charge	Q_{gs}		-	46	-	
Gate-Drain Charge	Q_{gd}		-	76	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 560\text{ V}$, $I_D = 22\text{ A}$ $R_g = 9.1\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	46	92	ns
Rise Time	t_r		-	77	116	
Turn-Off Delay Time	$t_{d(off)}$		-	157	236	
Fall Time	t_f		-	100	150	
Gate Input Resistance	R_g	$f = 1\text{ MHz}$, open drain	0.2	0.5	1.0	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	46	A
Pulsed Diode Forward Current	I_{SM}		-	-	154	
Diode Forward Voltage	V_{SD}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_S = 22\text{ A}$, $V_{GS} = 0\text{ V}$	-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_F = I_S = 22\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$, $V_R = 25\text{ V}$	-	202	404	ns
Reverse Recovery Charge	Q_{rr}		-	1.5	3.0	μC
Reverse Recovery Current	I_{RRM}		-	14	-	A

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .
 b. $C_{oss(tr)}$ is a fixed capacitance that gives the charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

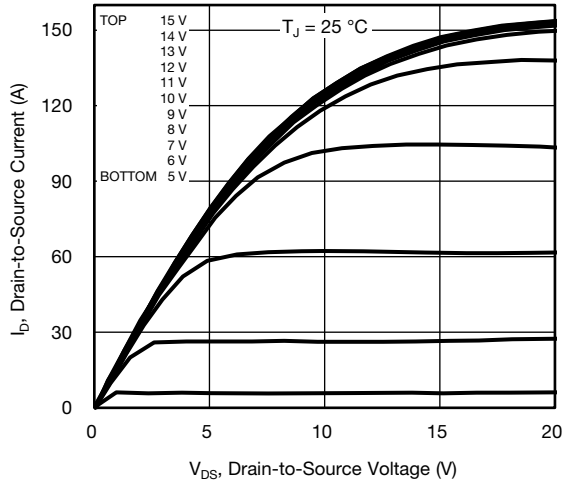


Fig. 1 - Typical Output Characteristics

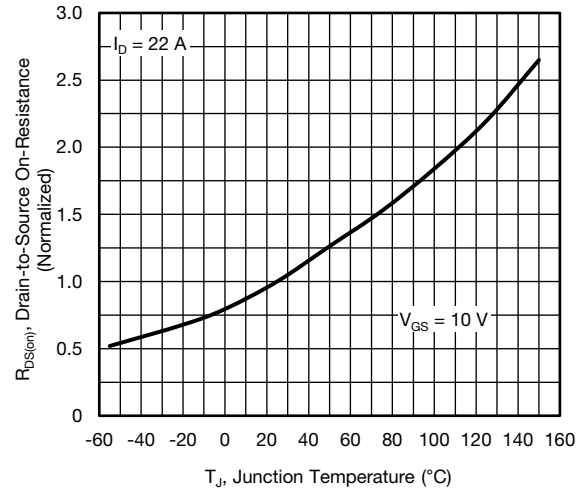


Fig. 4 - Normalized On-Resistance vs. Temperature

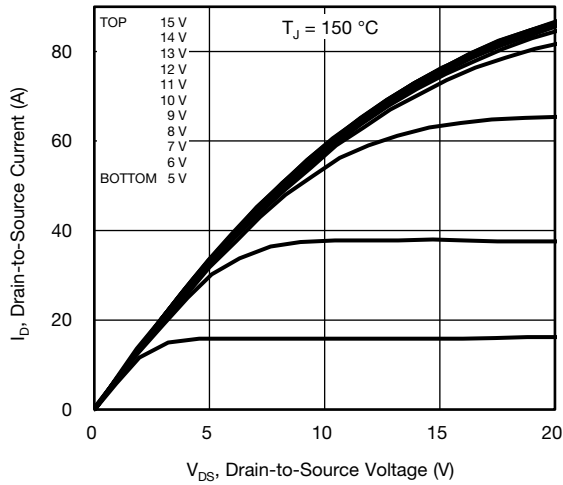


Fig. 2 - Typical Output Characteristics

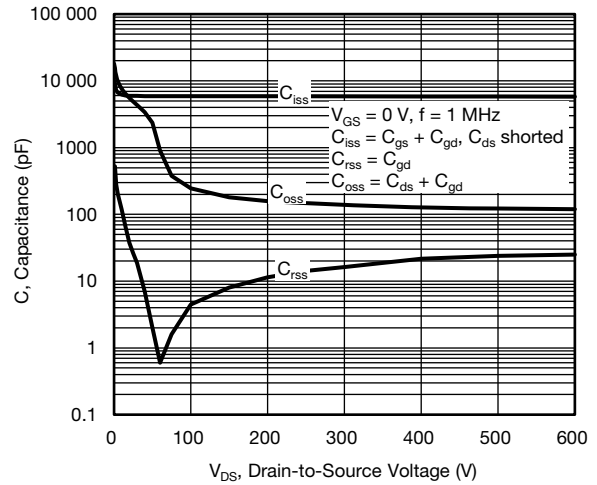


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

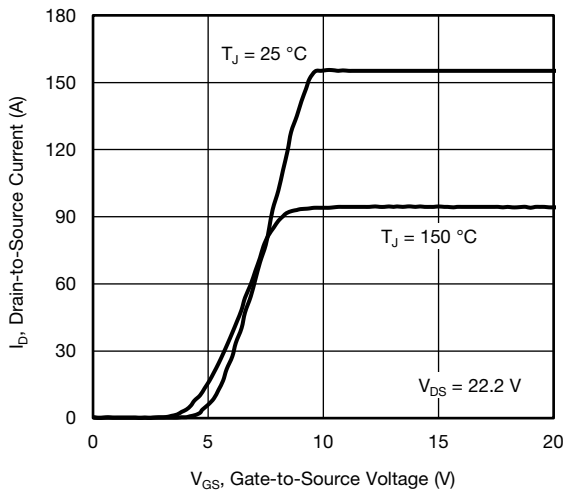


Fig. 3 - Typical Transfer Characteristics

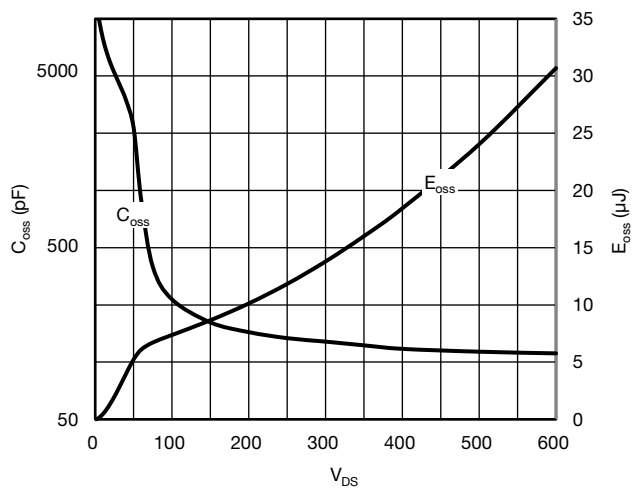


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

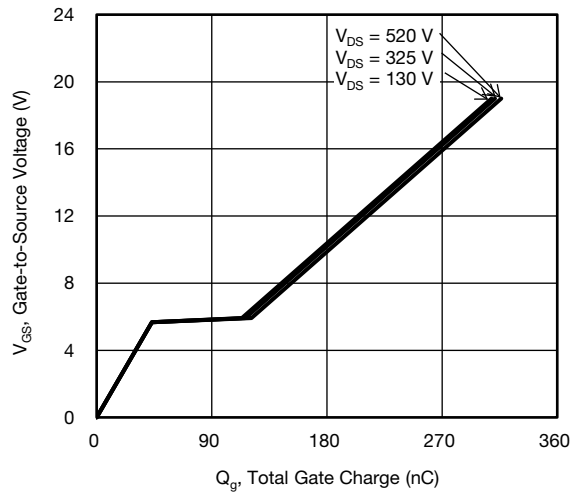


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

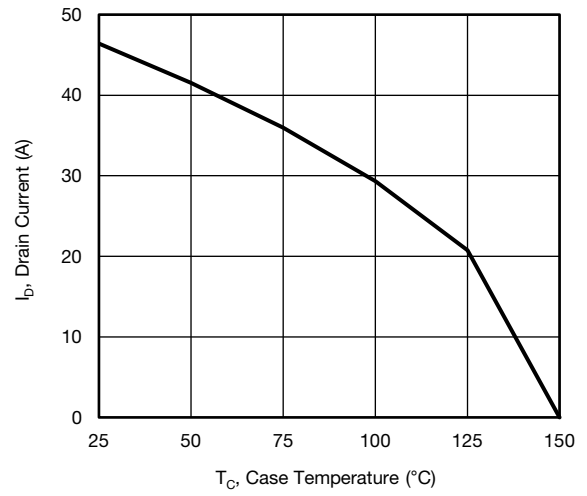


Fig. 10 - Maximum Drain Current vs. Case Temperature

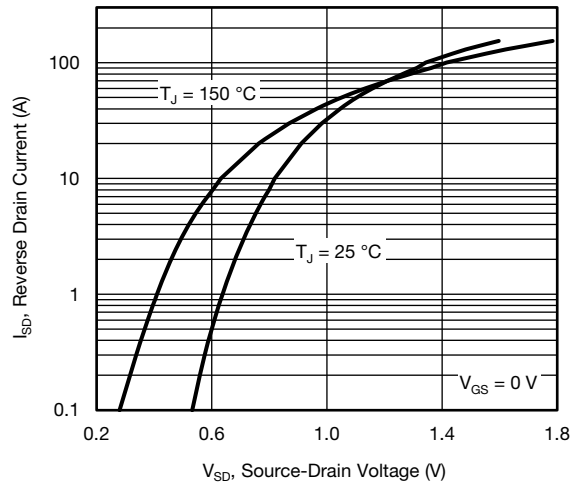


Fig. 8 - Typical Source-Drain Diode Forward Voltage

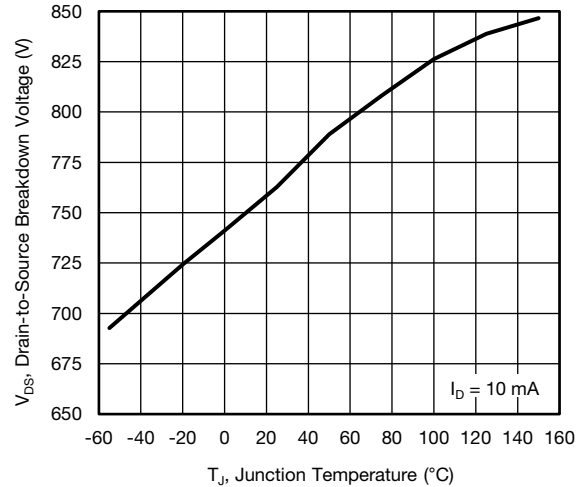


Fig. 11 - Typical Drain-to-Source Voltage vs. Temperature

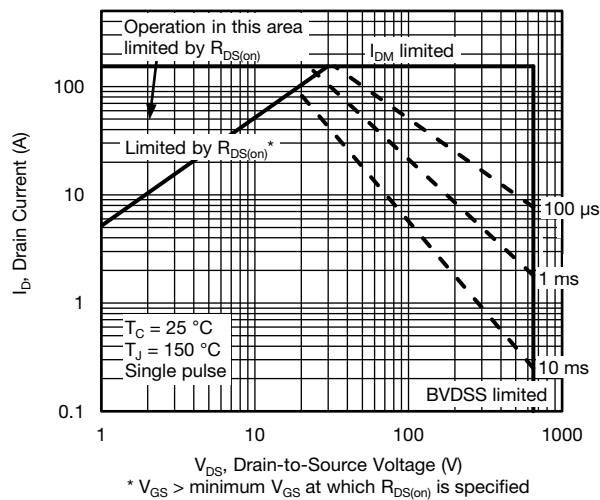


Fig. 9 - Maximum Safe Operating Area

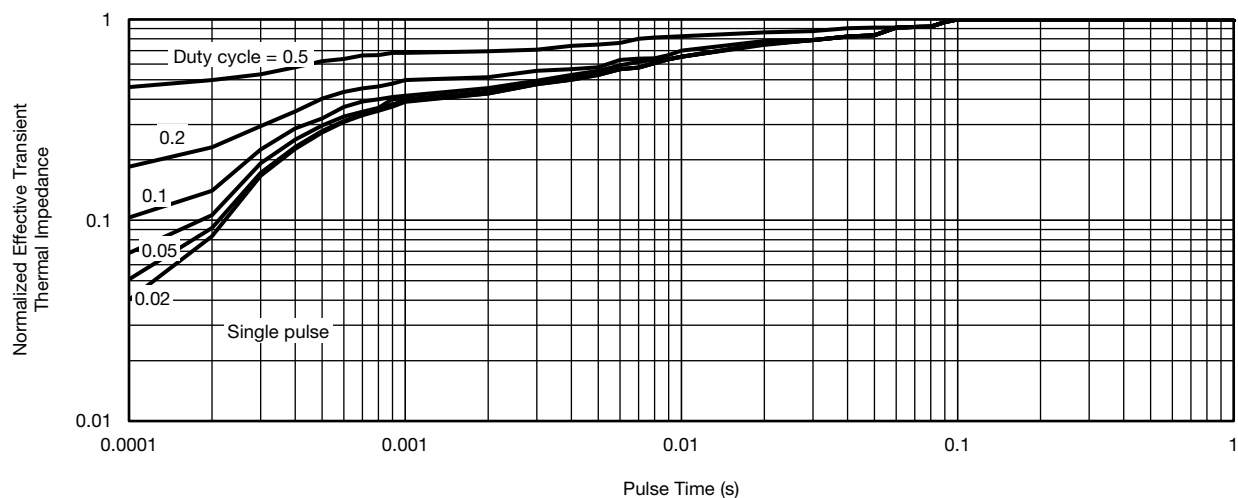


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

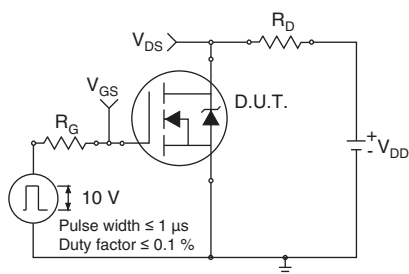


Fig. 13 - Switching Time Test Circuit

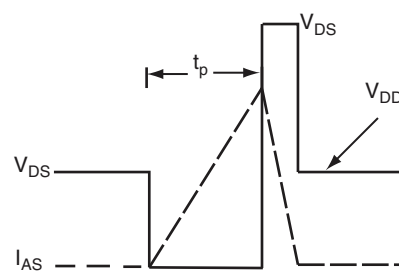


Fig. 16 - Unclamped Inductive Waveforms

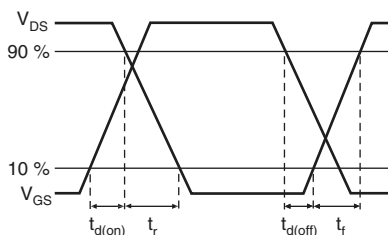


Fig. 14 - Switching Time Waveforms

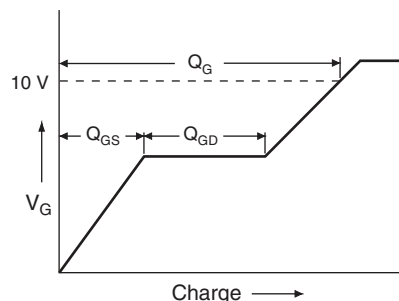


Fig. 17 - Basic Gate Charge Waveform

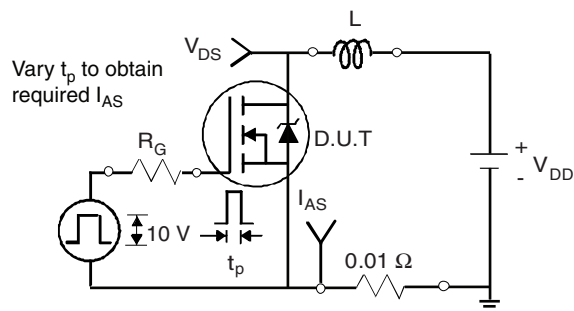


Fig. 15 - Unclamped Inductive Test Circuit

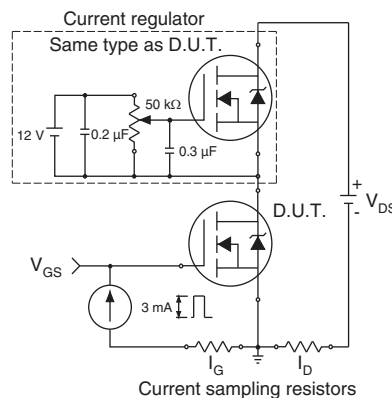
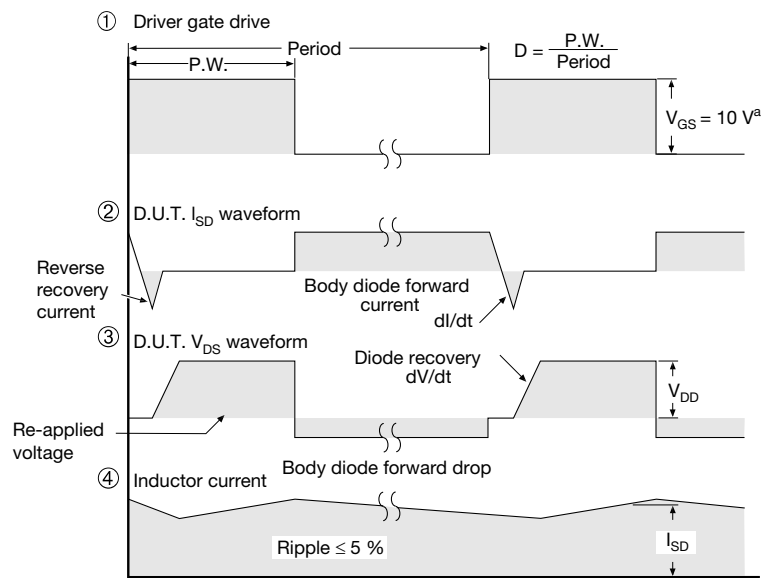
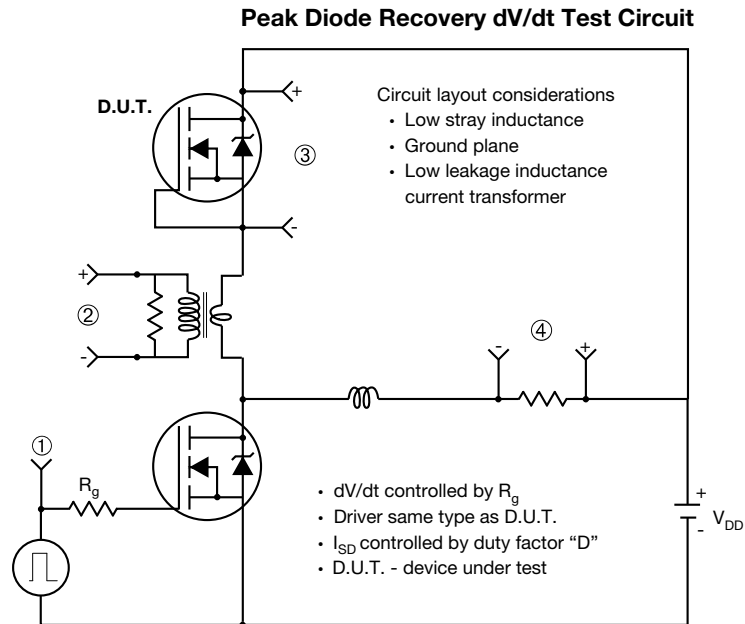


Fig. 18 - Gate Charge Test Circuit

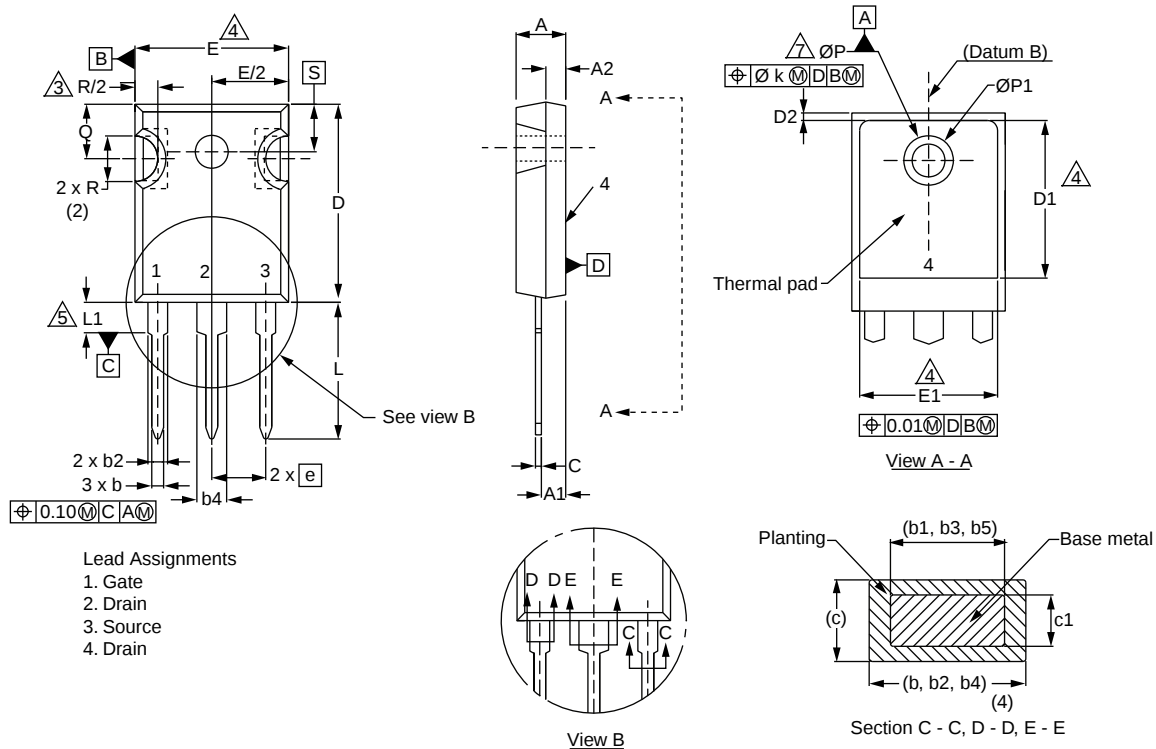


Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 19 - For N-Channel

TO-247AC (High Voltage)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.58	5.31	0.180	0.209
A1	2.21	2.59	0.087	0.102
A2	1.17	2.49	0.046	0.098
b	0.99	1.40	0.039	0.055
b1	0.99	1.35	0.039	0.053
b2	1.53	2.39	0.060	0.094
b3	1.65	2.37	0.065	0.093
b4	2.42	3.43	0.095	0.135
b5	2.59	3.38	0.102	0.133
c	0.38	0.86	0.015	0.034
c1	0.38	0.76	0.015	0.030
D	19.71	20.82	0.776	0.820
D1	13.08	-	0.515	-

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D2	0.51	1.30	0.020	0.051
E	15.29	15.87	0.602	0.625
E1	13.72	-	0.540	-
e	5.46 BSC		0.215 BSC	
Ø k	0.254		0.010	
L	14.20	16.25	0.559	0.640
L1	3.71	4.29	0.146	0.169
N	7.62 BSC		0.300 BSC	
Ø P	3.51	3.66	0.138	0.144
Ø P1	-	7.39	-	0.291
Q	5.31	5.69	0.209	0.224
R	4.52	5.49	0.178	0.216
S	5.51 BSC		0.217 BSC	

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