

TF5N50-VB Datasheet

N-Channel 650V (D-S) Power MOSFET

PRODUCT SUMMARY

| | | |
|------------------------------------|------------------------|-----|
| V_{DS} (V) at T_J max. | 650 | |
| $R_{DS(on)}$ at 25 °C (Ω) | $V_{GS} = 10\text{ V}$ | 1.1 |
| Q_g max. (nC) | 25 | |
| Q_{gs} (nC) | 2.0 | |
| Q_{gd} (nC) | 2.7 | |
| Configuration | Single | |

FEATURES

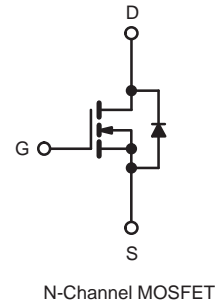
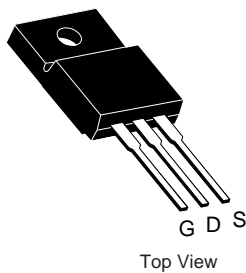
- Low figure-of-merit (FOM) $R_{DS(on)} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)



APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial

TO-220 FULLPAK



ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ °C}$, unless otherwise noted)

| PARAMETER | | | SYMBOL | LIMIT | UNIT |
|--|-------------------------------------|-------------------------------------|----------------|--------------|------|
| Drain-Source Voltage | | | V_{DS} | 650 | V |
| Gate-Source Voltage | | | V_{GS} | ± 30 | |
| Continuous Drain Current ($T_J = 150\text{ }^{\circ}\text{C}$) | V_{GS} at 10 V | $T_C = 25\text{ }^{\circ}\text{C}$ | I_D | 7.0 | A |
| | | $T_C = 100\text{ }^{\circ}\text{C}$ | | 5.6 | |
| Pulsed Drain Current ^a | | | I_{DM} | 28 | |
| Linear Derating Factor | | | | 1.67/1.5/0.3 | |
| Single Pulse Avalanche Energy ^b | | | E_{AS} | 86 | mJ |
| Maximum Power Dissipation | | | P_D | 83/83/31 | W |
| Operating Junction and Storage Temperature Range | | | T_J, T_{stg} | -55 to +150 | °C |
| Drain-Source Voltage Slope | $T_J = 125\text{ }^{\circ}\text{C}$ | | dV/dt | 50 | V/ns |
| Reverse Diode dV/dt ^d | | | | 4.5 | |
| Soldering Recommendations (Peak Temperature) ^c | for 10 s | | | 300 | °C |


Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DS} = 50\text{ V}$, starting $T_J = 25\text{ °C}$, $L = 28.2\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 3.5\text{ A}$.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, $dI/dt = 100\text{ A}/\mu\text{s}$, starting $T_J = 25\text{ °C}$.

THERMAL RESISTANCE RATINGS

| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
|----------------------------------|------------|------|------|------|
| Maximum Junction-to-Ambient | R_{thJA} | - | 63 | °C/W |
| Maximum Junction-to-Case (Drain) | R_{thJC} | - | 0.6 | |

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|----------------------------------|---|---|------|------|-------|------|
| Static | | | | | | | |
| Drain-Source Breakdown Voltage | V _{DS} | V _{GS} = 0 V, I _D = 250 μA | | 650 | - | - | V |
| V _{DS} Temperature Coefficient | ΔV _{DS} /T _J | Reference to 25 °C, I _D = 1 mA | | - | 0.65 | - | V/°C |
| Gate-Source Threshold Voltage (N) | V _{GS(th)} | V _{DS} = V _{GS} , I _D = 250 μA | | 2.5 | - | 5 | V |
| Gate-Source Leakage | I _{GSS} | V _{GS} = ± 20 V | | - | - | ± 100 | nA |
| | | V _{GS} = ± 30 V | | - | - | ± 1 | μA |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{DS} = 650 V, V _{GS} = 0 V | | - | - | 1 | μA |
| | | V _{DS} = 520 V, V _{GS} = 0 V, T _J = 125 °C | | - | - | 10 | |
| Drain-Source On-State Resistance | R _{DS(on)} | V _{GS} = 10 V | I _D = 4 A | - | 1.1 | - | Ω |
| Forward Transconductance | g _{fs} | V _{DS} = 30 V, I _D = 4 A | | - | 16 | - | S |
| Dynamic | | | | | | | |
| Input Capacitance | C _{iss} | V _{GS} = 0 V, V _{DS} = 100 V, f = 1 MHz | | - | 860 | - | pF |
| Output Capacitance | C _{oss} | | | - | 120 | - | |
| Reverse Transfer Capacitance | C _{rss} | | | - | 15 | - | |
| Effective Output Capacitance, Energy Related ^a | C _{o(er)} | V _{DS} = 0 V to 520 V, V _{GS} = 0 V | | - | 45 | - | pF |
| Effective Output Capacitance, Time Related ^b | C _{o(tr)} | | | - | 62 | - | |
| Total Gate Charge | Q _g | V _{GS} = 10 V | I _D = 4 A, V _{DS} = 520 V | - | 25 | - | nC |
| Gate-Source Charge | Q _{gs} | | | - | 2.0 | - | |
| Gate-Drain Charge | Q _{gd} | | | - | 2.7 | - | |
| Turn-On Delay Time | t _{d(on)} | V _{DD} = 520 V, I _D = 4 A, V _{GS} = 10 V, R _g = 9.1 Ω | | - | 25 | - | ns |
| Rise Time | t _r | | | - | 55 | - | |
| Turn-Off Delay Time | t _{d(off)} | | | - | 70 | - | |
| Fall Time | t _f | | | - | 40 | - | |
| Gate Input Resistance | R _g | f = 1 MHz, open drain | | - | 3.5 | - | Ω |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous Source-Drain Diode Current | I _S | MOSFET symbol showing the integral reverse p - n junction diode  | | - | - | 7 | A |
| Pulsed Diode Forward Current | I _{SM} | | | - | - | 18 | |
| Diode Forward Voltage | V _{SD} | T _J = 25 °C, I _S = 4 A, V _{GS} = 0 V | | - | - | 1.5 | V |
| Reverse Recovery Time | t _{rr} | T _J = 25 °C, I _F = I _S = 4 A, dI/dt = 100 A/μs, V _R = 400 V | | - | 190 | - | ns |
| Reverse Recovery Charge | Q _{rr} | | | - | 2.3 | - | μC |
| Reverse Recovery Current | I _{RRM} | | | - | 10 | - | A |

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
 b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



Fig. 7 - Typical Source-Drain Diode Forward Voltage



Fig. 9 - Maximum Drain Current vs. Case Temperature



Fig. 8 - Maximum Safe Operating Area



Fig. 10 - Temperature vs. Drain-to-Source Voltage



Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case



Fig. 12 - Switching Time Test Circuit



Fig. 16 - Basic Gate Charge Waveform



Fig. 13 - Switching Time Waveforms



Fig. 14 - Unclamped Inductive Test Circuit



Fig. 15 - Unclamped Inductive Waveforms



Fig. 17 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Fig. 18 - For N-Channel

TO-220 FULLPAK (HIGH VOLTAGE)

| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|--------|-----------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 4.570 | 4.830 | 0.180 | 0.190 |
| A1 | 2.570 | 2.830 | 0.101 | 0.111 |
| A2 | 2.510 | 2.850 | 0.099 | 0.112 |
| b | 0.622 | 0.890 | 0.024 | 0.035 |
| b2 | 1.229 | 1.400 | 0.048 | 0.055 |
| b3 | 1.229 | 1.400 | 0.048 | 0.055 |
| c | 0.440 | 0.629 | 0.017 | 0.025 |
| D | 8.650 | 9.800 | 0.341 | 0.386 |
| d1 | 15.88 | 16.120 | 0.622 | 0.635 |
| d3 | 12.300 | 12.920 | 0.484 | 0.509 |
| E | 10.360 | 10.630 | 0.408 | 0.419 |
| e | 2.54 BSC | | 0.100 BSC | |
| L | 13.200 | 13.730 | 0.520 | 0.541 |
| L1 | 3.100 | 3.500 | 0.122 | 0.138 |
| n | 6.050 | 6.150 | 0.238 | 0.242 |
| Ø P | 3.050 | 3.450 | 0.120 | 0.136 |
| u | 2.400 | 2.500 | 0.094 | 0.098 |
| v | 0.400 | 0.500 | 0.016 | 0.020 |

ECN: X09-0126-Rev. B, 26-Oct-09
 DWG: 5972

Notes

1. To be used only for process drawing.
2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads.
3. All critical dimensions should C meet $C_{pk} > 1.33$.
4. All dimensions include burrs and plating thickness.
5. No chipping or package damage.

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