

STF130N10F3-VB Datasheet

N-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY

| | | |
|---------------------------|------------------------|-------|
| V_{DS} (V) | 60 | |
| $R_{DS(on)}$ (Ω) | $V_{GS} = 10\text{ V}$ | 0.027 |
| Q_g (Max.) (nC) | 95 | |
| Q_{gs} (nC) | 27 | |
| Q_{gd} (nC) | 46 | |
| Configuration | Single | |

FEATURES

- Isolated Package
- High Voltage Isolation = 2.5 kV_{RMS} (t = 60 s; f = 60 Hz)
- Sink to Lead Creepage Distance = 4.8 mm
- 175 °C Operating Temperature
- Dynamic dV/dt Rating
- Low Thermal Resistance
- Lead (Pb)-free Available



TO-220 FULLPAK



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

| PARAMETER | SYMBOL | LIMIT | UNIT |
|--|------------------|-------------------------------------|-----------------------|
| Drain-Source Voltage | V_{DS} | 60 | V |
| Gate-Source Voltage | V_{GS} | ± 20 | |
| Continuous Drain Current | I_D | $T_C = 25\text{ }^{\circ}\text{C}$ | A |
| | | $T_C = 100\text{ }^{\circ}\text{C}$ | |
| Pulsed Drain Current ^a | I_{DM} | 220 | |
| Linear Derating Factor | | 0.32 | W/ $^{\circ}\text{C}$ |
| Single Pulse Avalanche Energy ^b | E_{AS} | 100 | mJ |
| Maximum Power Dissipation | P_D | 52 | W |
| Peak Diode Recovery dV/dt ^c | dV/dt | 4.5 | V/ns |
| Operating Junction and Storage Temperature Range | T_J, T_{stg} | - 55 to + 175 | $^{\circ}\text{C}$ |
| Soldering Recommendations (Peak Temperature) | for 10 s | 300 ^d | |
| Mounting Torque | 6-32 or M3 screw | 10 | lbf · in |
| | | 1.1 | N · m |

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25\text{ V}$, starting $T_J = 25\text{ }^{\circ}\text{C}$, $L = 129\text{ }\mu\text{H}$, $R_G = 25\text{ }\Omega$, $I_{AS} = 30\text{ A}$ (see fig. 12).
- $I_{SD} \leq 52\text{ A}$, $dI/dt \leq 250\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 175\text{ }^{\circ}\text{C}$.
- 1.6 mm from case.

THERMAL RESISTANCE RATINGS

| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
|----------------------------------|------------|------|------|------|
| Maximum Junction-to-Ambient | R_{thJA} | - | 65 | °C/W |
| Maximum Junction-to-Case (Drain) | R_{thJC} | - | 3.1 | |

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|----------------------------------|--|--|------|-------|-------|------|
| Static | | | | | | | |
| Drain-Source Breakdown Voltage | V _{DS} | V _{GS} = 0 V, I _D = 250 μA | | 60 | - | - | V |
| V _{DS} Temperature Coefficient | ΔV _{DS} /T _J | Reference to 25 °C, I _D = 1 mA | | - | 0.060 | - | V/°C |
| Gate-Source Threshold Voltage | V _{GS(th)} | V _{DS} = V _{GS} , I _D = 250 μA | | 1.0 | - | 3.0 | V |
| Gate-Source Leakage | I _{GSS} | V _{GS} = ± 20 V | | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{DS} = 60 V, V _{GS} = 0 V | | - | - | 25 | μA |
| | | V _{DS} = 48 V, V _{GS} = 0 V, T _J = 150 °C | | - | - | 250 | |
| Drain-Source On-State Resistance | R _{DS(on)} | V _{GS} = 10 V | I _D = 18 A ^b | - | 0.027 | - | Ω |
| Forward Transconductance | g _{fs} | V _{DS} = 25 V, I _D = 18 A ^b | | 15 | - | - | S |
| Dynamic | | | | | | | |
| Input Capacitance | C _{iss} | V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5 | | - | 1500 | - | pF |
| Output Capacitance | C _{oss} | | | - | 720 | - | |
| Reverse Transfer Capacitance | C _{rss} | | | - | 100 | - | |
| Drain to Sink Capacitance | C | f = 1.0 MHz | | - | 12 | - | |
| Total Gate Charge | Q _g | V _{GS} = 10 V | I _D = 52 A, V _{DS} = 48 V, see fig. 6 and 13 ^b | - | - | 95 | nC |
| Gate-Source Charge | Q _{gs} | | | - | - | 27 | |
| Gate-Drain Charge | Q _{gd} | | | - | - | 46 | |
| Turn-On Delay Time | t _{d(on)} | V _{DD} = 30 V, I _D = 52 A, R _G = 9.1 Ω, R _D = 0.54 Ω, see fig. 10 ^b | | - | 19 | - | ns |
| Rise Time | t _r | | | - | 120 | - | |
| Turn-Off Delay Time | t _{d(off)} | | | - | 55 | - | |
| Fall Time | t _f | | | - | 86 | - | |
| Internal Drain Inductance | L _D | Between lead, 6 mm (0.25") from package and center of die contact | | - | 4.5 | - | nH |
| Internal Source Inductance | L _S | | | - | 7.5 | - | |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous Source-Drain Diode Current | I _S | MOSFET symbol showing the integral reverse p - n junction diode | | - | - | 45 | A |
| Pulsed Diode Forward Current ^a | I _{SM} | | | - | - | 120 | |
| Body Diode Voltage | V _{SD} | T _J = 25 °C, I _S = 30 A, V _{GS} = 0 V ^b | | - | - | 2.5 | V |
| Body Diode Reverse Recovery Time | t _{rr} | T _J = 25 °C, I _F = 52 A, dI/dt = 100 A/μs ^b | | - | 140 | 300 | ns |
| Body Diode Reverse Recovery Charge | Q _{rr} | | | - | 1.2 | 2.8 | μC |
| Forward Turn-On Time | t _{on} | Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D) | | | | | |

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^{\circ}\text{C}$



Fig. 3 - Typical Transfer Characteristics



Fig. 2 - Typical Output Characteristics, $T_C = 175\text{ }^{\circ}\text{C}$



Fig. 4 - Normalized On-Resistance vs. Temperature



Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

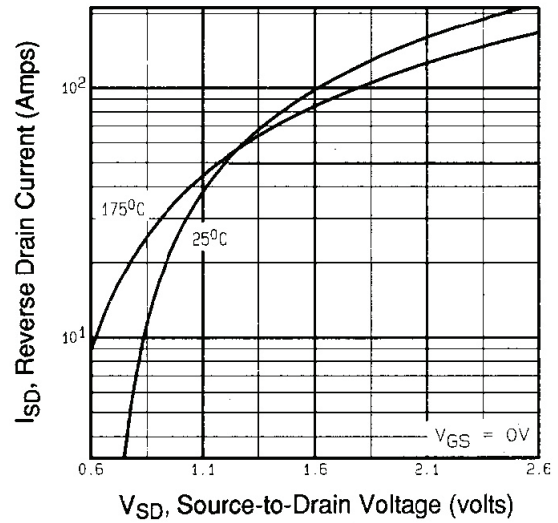


Fig. 7 - Typical Source-Drain Diode Forward Voltage



Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



Fig. 8 - Maximum Safe Operating Area

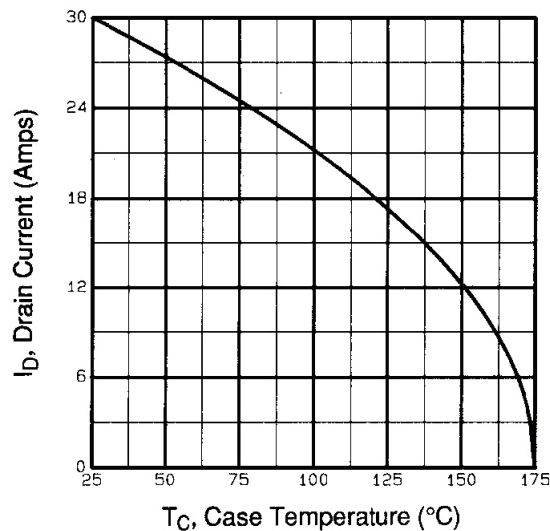


Fig. 9 - Maximum Drain Current vs. Case Temperature

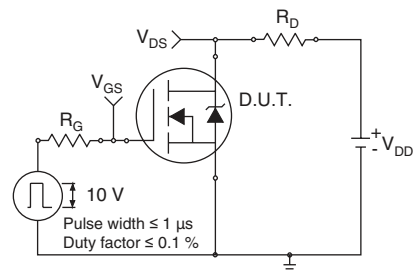


Fig. 10a - Switching Time Test Circuit

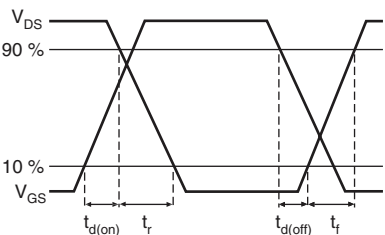


Fig. 10b - Switching Time Waveforms

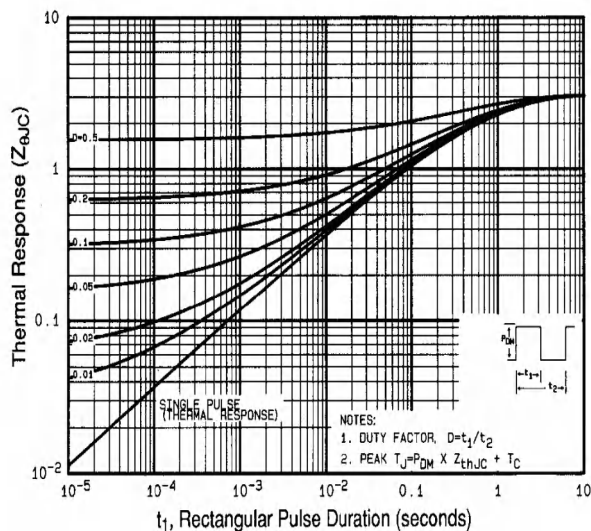


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

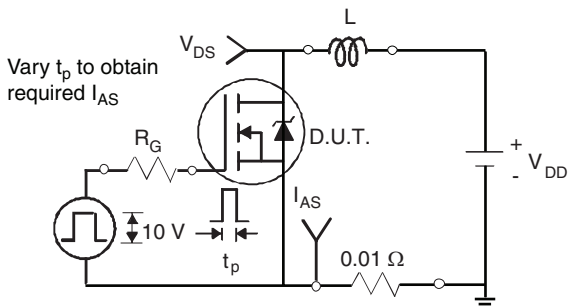


Fig. 12a - Unclamped Inductive Test Circuit

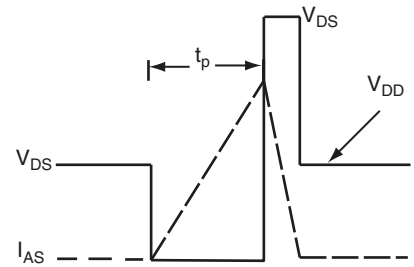


Fig. 12b - Unclamped Inductive Waveforms

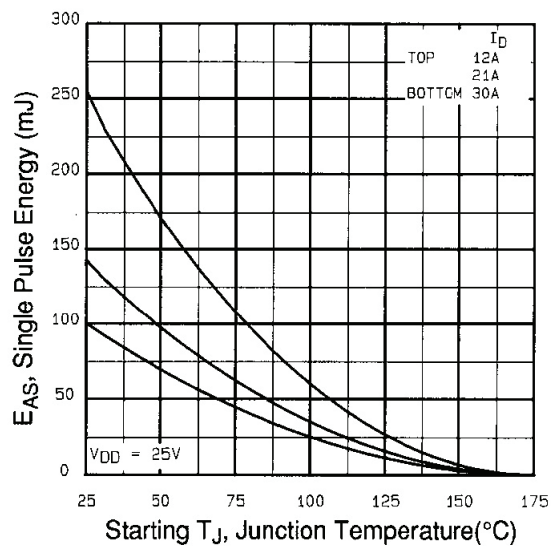


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

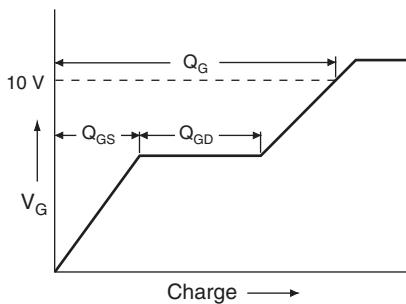


Fig. 13a - Basic Gate Charge Waveform

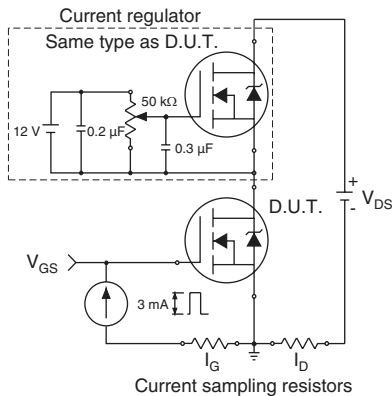


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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