

## LND08R085-VB Datasheet

### N-Channel 80 V (D-S) MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)
80	0.0064 at V <sub>GS</sub> = 10 V	75 <sup>a</sup>	17.1 nC
	0.0070 at V <sub>GS</sub> = 6.0 V	65 <sup>a</sup>	
	0.0087 at V <sub>GS</sub> = 4.5 V	54	

#### FEATURES

- Trench Power MOSFET
- 100 % R<sub>g</sub> and UIS Tested

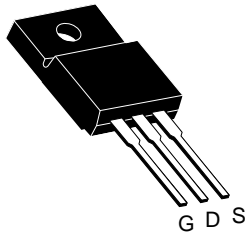
#### APPLICATIONS

- Primary Side Switching
- Synchronous Rectification
- DC/AC Inverters
- LED Backlighting

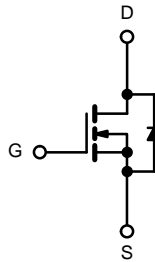


**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

TO-220 FULLPAK



Top View



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V <sub>DS</sub>	80	V
Gate-Source Voltage		V <sub>GS</sub>	± 20	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>C</sub> = 25 °C	I <sub>D</sub>	75 <sup>a</sup>	A
	T <sub>C</sub> = 70 °C		62.7	
	T <sub>A</sub> = 25 °C		28.6 <sup>b, c</sup>	
	T <sub>A</sub> = 70 °C		24.9 <sup>b, c</sup>	
Pulsed Drain Current (t = 100 μs)		I <sub>DM</sub>	150	
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C	I <sub>S</sub>	75 <sup>a</sup>	
	T <sub>A</sub> = 25 °C		4.5 <sup>b, c</sup>	
Single Pulse Avalanche Current		I <sub>AS</sub>	30	
Single Pulse Avalanche Energy		E <sub>AS</sub>	45	mJ
Maximum Power Dissipation	T <sub>C</sub> = 25 °C	P <sub>D</sub>	62.5	W
	T <sub>C</sub> = 70 °C		40	
	T <sub>A</sub> = 25 °C		5 <sup>b, c</sup>	
	T <sub>A</sub> = 70 °C		3.2 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>			260	

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Typical	Maximum
Maximum Junction-to-Ambient <sup>b, f</sup>	t ≤ 10 s	R <sub>thJA</sub>	20	25
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	1.5	2.0

#### Notes

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- The TO-220 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 70 °C/W.

SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	80			V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA		37		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>			- 6.1		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.4		2.6	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	30			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		0.0064		Ω
		V <sub>GS</sub> = 6 V, I <sub>D</sub> = 15 A		0.0070		
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A		0.0087		
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 20 A		60		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V, f = 1 MHz		1855		pF
Output Capacitance	C <sub>oss</sub>			950		
Reverse Transfer Capacitance	C <sub>rss</sub>			76		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		35.5	54	nC
		V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 6 V, I <sub>D</sub> = 10 A		22	33	
		V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A		17.1	26	
Gate-Source Charge	Q <sub>gs</sub>			5.3		
Gate-Drain Charge	Q <sub>gd</sub>			7.3		
Output Charge	Q <sub>oss</sub>	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V		57	86	
Gate Resistance	R <sub>g</sub>	f = 1 MHz	0.5	1.3	2	Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 40 V, R <sub>L</sub> = 4 Ω I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		12	24	ns
Rise Time	t <sub>r</sub>			8	16	
Turn-Off DelayTime	t <sub>d(off)</sub>			32	64	
Fall Time	t <sub>f</sub>			7	14	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 40 V, R <sub>L</sub> = 4 Ω I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 6.0 V, R <sub>g</sub> = 1 Ω		14	28	
Rise Time	t <sub>r</sub>			11	22	
Turn-Off DelayTime	t <sub>d(off)</sub>			30	60	
Fall Time	t <sub>f</sub>			8	16	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			75	A
Pulse Diode Forward Current (t = 100 μs)	I <sub>SM</sub>				150	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 5 A		0.76	1.1	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 10 A, dI/dt = 100 A/μs, T <sub>J</sub> = 25 °C		38	75	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			36	70	nC
Reverse Recovery Fall Time	t <sub>a</sub>			19		ns
Reverse Recovery Rise Time	t <sub>b</sub>			19		

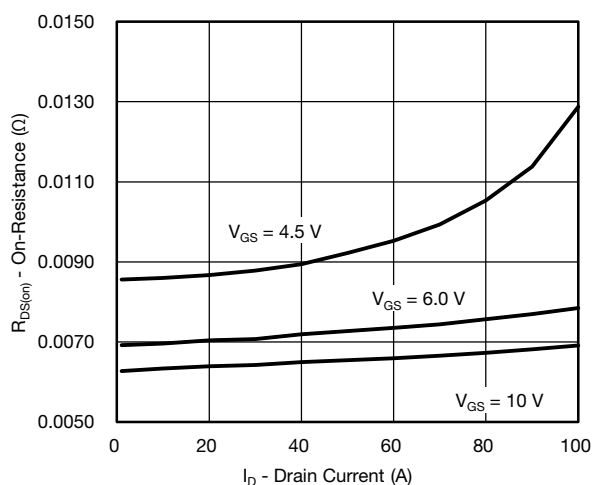
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
 b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

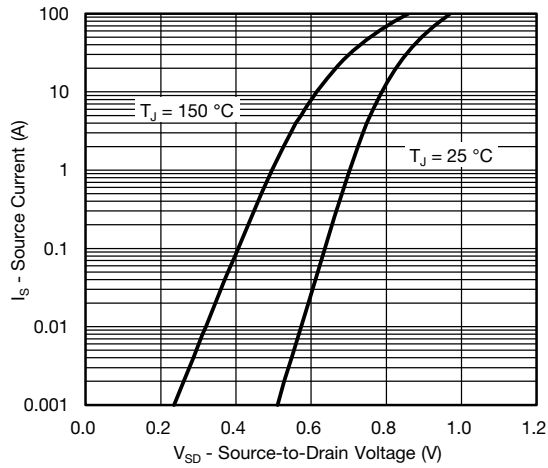
**Output Characteristics**

**Transfer Characteristics**

**On-Resistance vs. Drain Current**

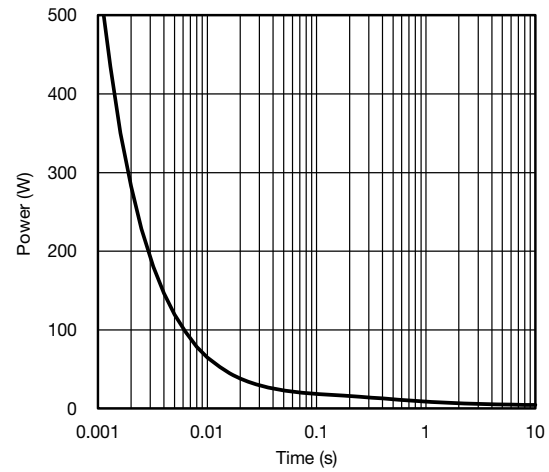
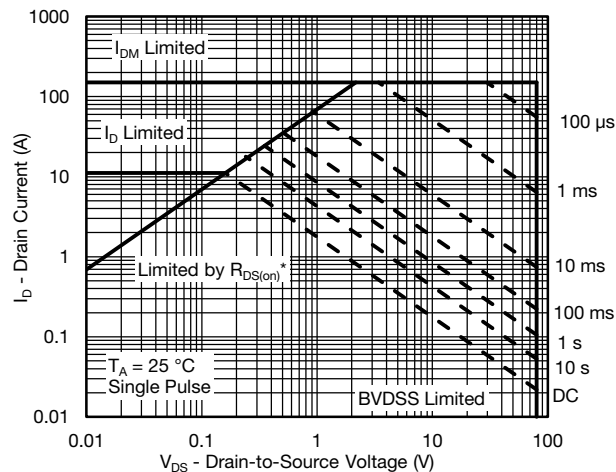
**Capacitance**

**Gate Charge**

**On-Resistance vs. Junction Temperature**

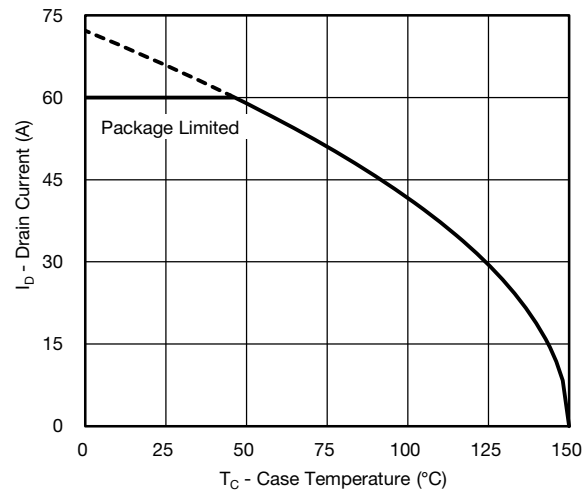
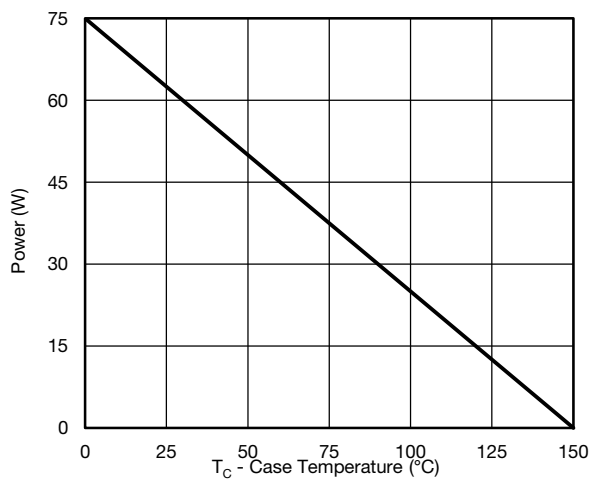
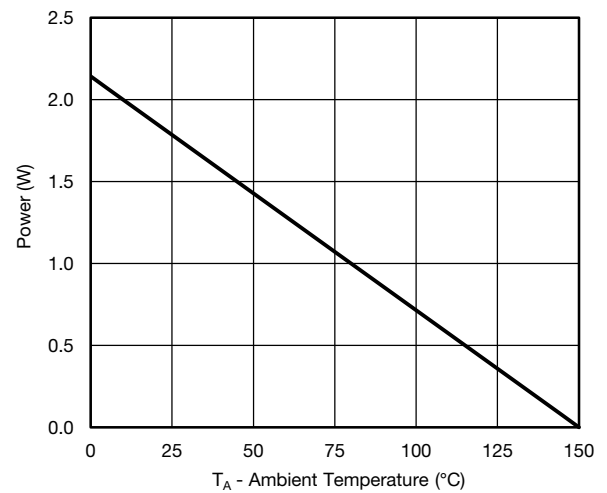
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Source-Drain Diode Forward Voltage**

**On-Resistance vs. Gate-to-Source Voltage**

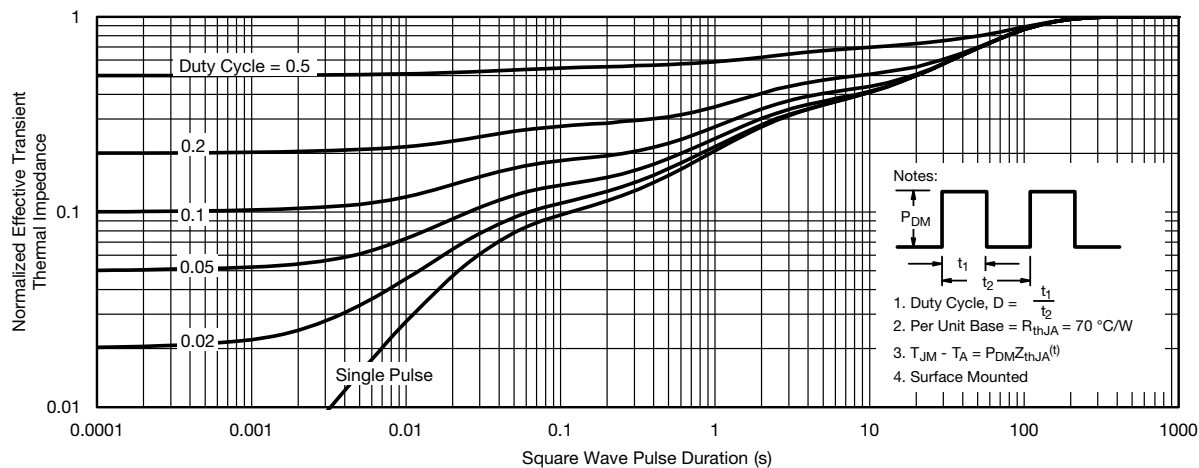
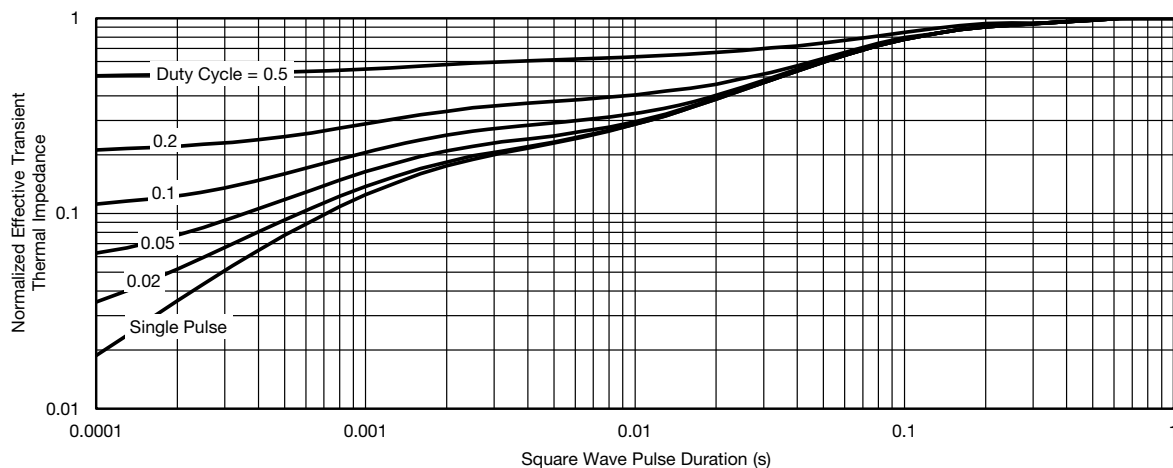
**Threshold Voltage**

**Single Pulse Power, Junction-to-Ambient**


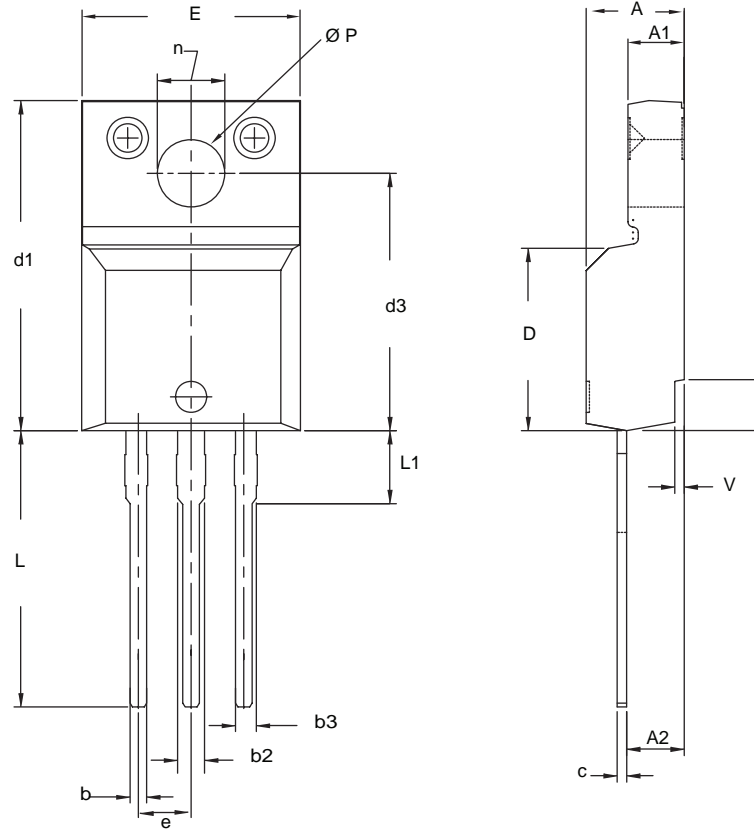
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

**Safe Operating Area, Junction-to-Ambient**

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Current Derating\*****Power, Junction-to-Case****Power, Junction-to-Ambient**

\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Normalized Thermal Transient Impedance, Junction-to-Ambient**

**Normalized Thermal Transient Impedance, Junction-to-Case**

**TO-220 FULLPAK (HIGH VOLTAGE)**

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
v	0.400	0.500	0.016	0.020

ECN: X09-0126-Rev. B, 26-Oct-09  
DWG: 5972

**Notes**

1. To be used only for process drawing.
2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads.
3. All critical dimensions should C meet  $C_{pk} > 1.33$ .
4. All dimensions include burrs and plating thickness.
5. No chipping or package damage.

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