

K897-VB Datasheet

N-Channel 650V (D-S) Power MOSFET

PRODUCT SUMMARY					
V _{DS} (V) at T _J max.	650)			
R _{DS(on)} at 25 °C (Ω)	V _{GS} = 10 V	1.1			
Q _g max. (nC)	25				
Q _{gs} (nC)	2.0)			
Q _{gd} (nC)	2.7				
Configuration	Single				

Top View

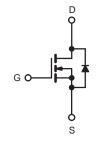
TO-220 FULLPAK

FEATURES

- Low figure-of-merit (FOM) Ron x Qa
- Low input capacitance (Ciss)
- · Reduced switching and conduction losses
- Ultra low gate charge (Qq)
- Avalanche energy rated (UIS)

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)							
PARAMETER			SYMBOL	LIMIT	UNIT		
Drain-Source Voltage	Drain-Source Voltage			650	V		
Gate-Source Voltage			V_{GS}	± 30	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \		
Continuous Drain Current (T, = 150 °C)	V _{GS} at 10 V	T _C = 25 °C	l _D	7.0			
Continuous Drain Current (1) = 130 C)		T _C = 100 °C		5.6	А		
Pulsed Drain Current ^a			I _{DM}	28			
Linear Derating Factor				1.67/1.5/0.3	W/°C		
Single Pulse Avalanche Energy ^b Maximum Power Dissipation Operating Junction and Storage Temperature Range			E _{AS}	86	mJ		
			P_{D}	83/83/31	W		
			T _J , T _{stg}	-55 to +150	°C		
Drain-Source Voltage Slope	T _J = 125 °C		dV/dt	50	V/ns		
Reverse Diode dV/dt ^d			uv/ul	4.5	V/NS		
Soldering Recommendations (Peak Temperature) ^c	for 10 s			300	°C		

- a. Repetitive rating; pulse width limited by maximum junction temperature. b. $V_{DD}=50$ V, starting $T_J=25$ °C, L=28.2 mH, $R_g=25$ Ω , $I_{AS}=3.5$ A.

- c. 1.6 mm from case. d. $I_{SD} \le I_D$, dl/dt = 100 A/ μ s, starting $T_J = 25$ °C.



THERMAL RESISTANCE RAT	INGS			
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R _{thJA}	-	63	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	-	0.6	C/ VV

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static		<u> </u>					•
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		650	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference	Reference to 25 °C, I _D = 1 mA		0.65	-	V/°C
Gate-Source Threshold Voltage (N)	V _{GS(th)}	V _{DS} =	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$		-	5	V
		$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA
Gate-Source Leakage	I_{GSS}		$V_{GS} = \pm 30 \text{ V}$		-	± 1	μA
		V _{DS} = 650 V, V _{GS} = 0 V		_	-	1	i i
Zero Gate Voltage Drain Current	I _{DSS}		/, V _{GS} = 0 V, T _J = 125 °C	-	-	10	μΑ
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 4 A	-	1.1	-	Ω
Forward Transconductance	9 _{fs}	V _{DS}	= 30 V, I _D = 4 A	-	16	-	S
Dynamic							
Input Capacitance	C _{iss}	V - 0 V		_	860	-	
Output Capacitance	Coss	1	$V_{GS} = 0 \text{ V},$ $V_{DS} = 100 \text{ V},$		120	-	
Reverse Transfer Capacitance	C _{rss}	1	f = 1 MHz	-	15	-	1
Effective Output Capacitance, Energy Related ^a	C _{o(er)}	V _{DS} = 0 V to 520 V, V _{GS} = 0 V		-	45	-	pF
Effective Output Capacitance, Time Related ^b	C _{o(tr)}			-	62	-	
Total Gate Charge	Qg			-	25		
Gate-Source Charge	Q _{gs}	V _{GS} = 10 V	$V_{GS} = 10 \text{ V}$ $I_{D} = 4 \text{ A}, V_{DS} = 520 \text{ V}$	-	2.0	-	nC
Gate-Drain Charge	Q _{gd}	1			2.7	-	1
Turn-On Delay Time	t _{d(on)}	V _{DD} = 520 V, I _D = 4 A,		-	25	-	
Rise Time	t _r			-	55	-]
Turn-Off Delay Time	t _{d(off)}	V _{GS} =	= 10 V, $R_g = 9.1 \Omega$	-	70	-	ns
Fall Time	t _f	1		-	40	-	
Gate Input Resistance	R_g	f = 1 MHz, open drain		-	3.5	-	Ω
Drain-Source Body Diode Characteristic	s						
Continuous Source-Drain Diode Current	I _S	MOSFET sym	bol	-	-	7	
Pulsed Diode Forward Current	I _{SM}	integral reverse p - n junction diode		-	-	18	_ A
Diode Forward Voltage	V _{SD}	T _J = 25 °C, I _S = 4 A, V _{GS} = 0 V		-	-	1.5	V
Reverse Recovery Time	t _{rr}	$T_J = 25 \text{ °C}, I_F = I_S = 4 \text{ A},$ $dI/dt = 100 \text{ A/µs}, V_R = 400 \text{ V}$		-	190	-	ns
Reverse Recovery Charge	Q _{rr}			_	2.3	-	μC
Reverse Recovery Current	I _{RRM}			_	10	_	A

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} . b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

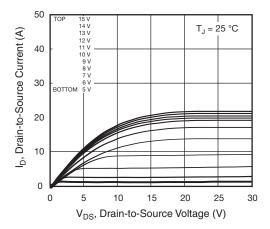


Fig. 1 - Typical Output Characteristics

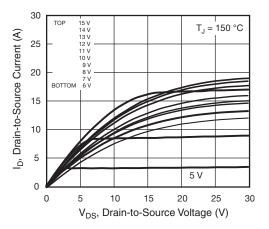


Fig. 2 - Typical Output Characteristics

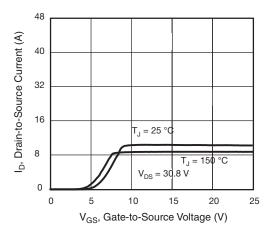


Fig. 3 - Typical Transfer Characteristics

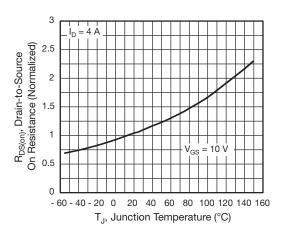


Fig. 4 - Normalized On-Resistance vs. Temperature

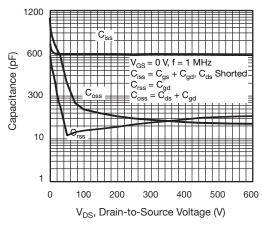


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

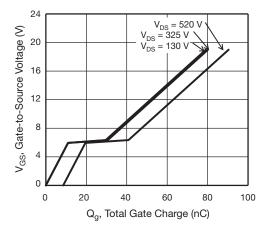


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



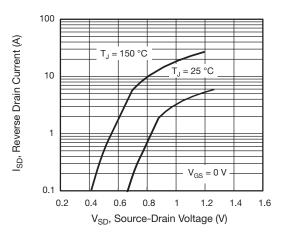


Fig. 7 - Typical Source-Drain Diode Forward Voltage

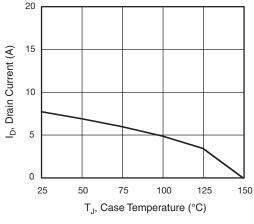


Fig. 9 - Maximum Drain Current vs. Case Temperature

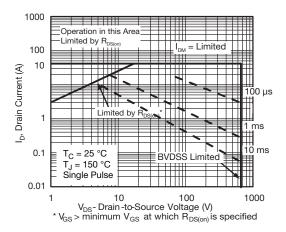


Fig. 8 - Maximum Safe Operating Area

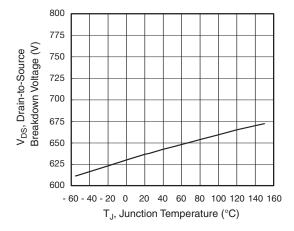


Fig. 10 - Temperature vs. Drain-to-Source Voltage

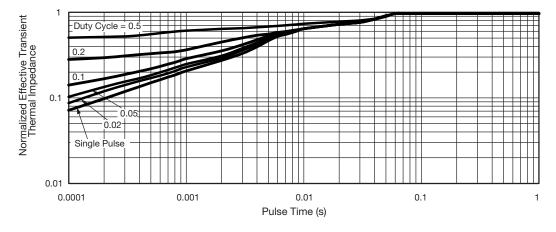


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case



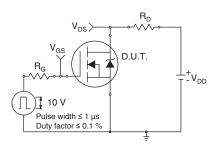


Fig. 12 - Switching Time Test Circuit

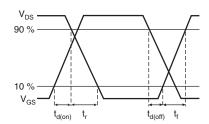


Fig. 13 - Switching Time Waveforms

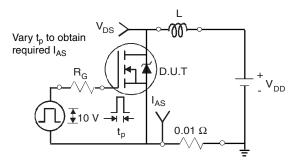


Fig. 14 - Unclamped Inductive Test Circuit

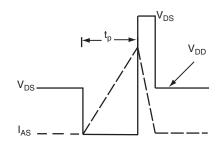


Fig. 15 - Unclamped Inductive Waveforms

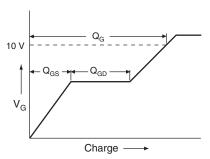


Fig. 16 - Basic Gate Charge Waveform

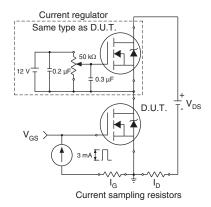
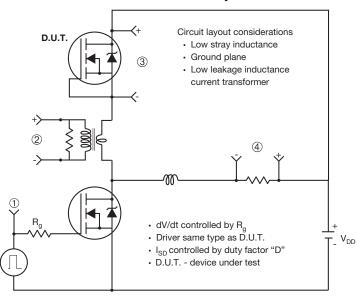


Fig. 17 - Gate Charge Test Circuit

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Peak Diode Recovery dV/dt Test Circuit



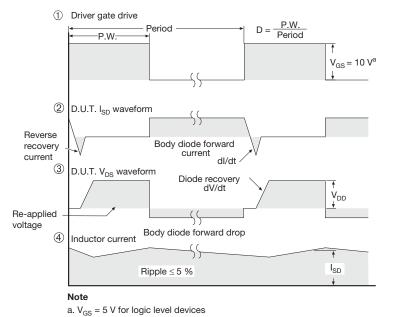
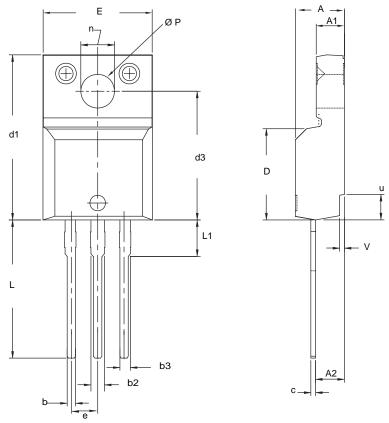


Fig. 18 - For N-Channel

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TO-220 FULLPAK (HIGH VOLTAGE)



	MILLIMETERS		INCHES		
DIM.	MIN.	MAX.	MIN.	MAX.	
Α	4.570	4.830	0.180	0.190	
A1	2.570	2.830	0.101	0.111	
A2	2.510	2.850	0.099	0.112	
b	0.622	0.890	0.024	0.035	
b2	1.229	1.400	0.048	0.055	
b3	1.229	1.400	0.048	0.055	
С	0.440	0.629	0.017	0.025	
D	8.650	9.800	0.341	0.386	
d1	15.88	16.120	0.622	0.635	
d3	12.300	12.920	0.484	0.509	
E	10.360	10.630	0.408	0.419	
е	2.54	BSC	0.100 BSC		
L	13.200	13.730	0.520	0.541	
L1	3.100	3.500	0.122	0.138	
n	6.050	6.150	0.238	0.242	
ØΡ	3.050	3.450	0.120	0.136	
u	2.400	2.500	0.094	0.098	
V	0.400	0.500	0.016	0.020	

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- To be used only for process drawing.
 These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads.
 All critical dimensions should C meet C_{pk} > 1.33.
 All dimensions include burrs and plating thickness.

- 5. No chipping or package damage.



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