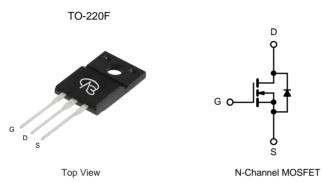


IRLI3103-VB Datasheet

N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^{a, e}	Q _g (Typ)		
30	0.010 at V _{GS} = 10 V	68	82 nC		
- 30	0.012 at V_{GS} = 4.5 V	62	02110		



FEATURES

- Trench Power MOSFET
- 100 % R_g and UIS Tested •
- Compliant to RoHS Directive 2011/65/EU

APPLICATIONS

- OR-ing
- Server
- DC/DC

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	30	V		
Gate-Source Voltage		V _{GS}		± 20	
	T _C = 25 °C		68 ^{a, e}	A	
Continuous Drain Current (T ₁ = 175 °C)	T _C = 70 °C		62 ^e		
Continuous Drain Current $(T_j = T/5 C)$	T _A = 25 °C	I _D	68.8 ^{b, c}		
	T _A = 70 °C		57 ^{b, c}	^	
Pulsed Drain Current		I _{DM}	90	-	
Avalanche Current Pulse	L = 0.1 mH	I _{AS}	36		
Single Pulse Avalanche Energy	L = 0.1 1111	E _{AS}	64.8	V	
Continuous Source-Drain Diode Current	T _C = 25 °C	I _S	90 ^{a, e}	Α	
Continuous Source-Drain Diode Current	T _A = 25 °C	'S	3.13 ^{b, c}	A	
	T _C = 25 °C		250 ^a	w	
Maximum Power Dissipation	T _C = 70 °C	P _D	175		
	T _A = 25 °C	' D	3.75 ^{b, c}		
	T _A = 70 °C		2.63 ^{b, c}		
Operating Junction and Storage Temperature R	ange	T _J , T _{stg}	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Тур.	Max.	Unit	
Maximum Junction-to-Ambient ^{b, d}	$t \le 10 \text{ sec}$	R _{thJA}	32	40	°C/W	
Maximum Junction-to-Case	Steady State	R _{thJC}	0.5	0.6	0,00	

Notes:

a. Based on $T_C = 25 \text{ °C}$. b. Surface mounted on 1" x 1" FR4 board.

d. Maximum under steady state conditions is 90 °C/W.

e. Calculated based on maximum junction temperature. Package limitation current is 90 A.

Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static			•	+	•	•	
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 V, I_D = 250 \mu A$	30			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	L _ 250 uA		35		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA		- 7.5		mv/°C	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	1.5		2.5	V	
Gate-Source Leakage	I _{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA	
-		$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			1		
Zero Gate Voltage Drain Current	IDSS	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 \text{ °C}$			10	μA	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, \text{ V}_{GS} = 10 \text{ V}$	90			A	
	_	V _{GS} = 10 V, I _D = 28.8 A		0.010			
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 27 A		0.012		Ω	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 28.8 A		160		S	
Dynamic ^b			<u> </u>	1	<u> </u>	I	
Input Capacitance	C _{iss}			1400			
Output Capacitance	C _{oss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		1200		pF	
Reverse Transfer Capacitance	C _{rss}			970			
Tatal Oats Observe		V_{DS} = 15 V, V_{GS} = 10 V, I_{D} = 28.8 A		171	257	nC	
Total Gate Charge	Qg			81.5	123		
Gate-Source Charge	Q _{gs}	V_{DS} = 15 V, V_{GS} = 4.5 V, I_{D} = 28.8 A		34			
Gate-Drain Charge	Q _{gd}			29			
Gate Resistance	R _g	f = 1 MHz		1.4	2.1	Ω	
Turn-On Delay Time	t _{d(on)}			18	27		
Rise Time	t _r	V_{DD} = 15 V, R_L = 0.625 Ω		11	17		
Turn-Off Delay Time	t _{d(off)}	$\text{I}_\text{D}\cong$ 24 A, V_GEN = 10 V, R_g = 1 Ω		70	105		
Fall Time	t _f			10	15		
Turn-On Delay Time	t _{d(on)}			55	83	ns	
Rise Time	t _r	V_{DD} = 15 V, R_L = 0.67 Ω		180	270		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong$ 22.5 A, V_{GEN} = 4.5 V, R_g = 1 Ω		55	83		
Fall Time	t _f			12	18	1	
Drain-Source Body Diode Characteristic	s		<u> </u>	1	<u> </u>	I	
Continuous Source-Drain Diode Current	۱ _S	T _C = 25 °C			90	•	
Pulse Diode Forward Current ^a	I _{SM}				90	A	
Body Diode Voltage	V _{SD}	I _S = 22 A		0.8	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			52	78	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	L = 20.4 di/dt = 100.4/ma T = 25.90		70.2	105	nC	
Reverse Recovery Fall Time	t _a	I _F = 20 A, di/dt = 100 A/μs, T _J = 25 °C		27			
Reverse Recovery Rise Time	t _b			25		ns	

Notes:

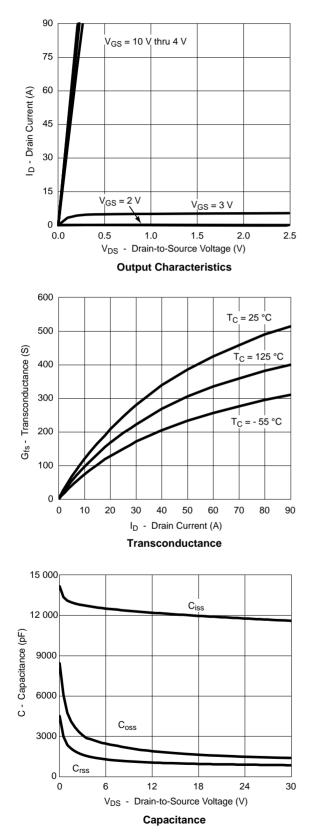
a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

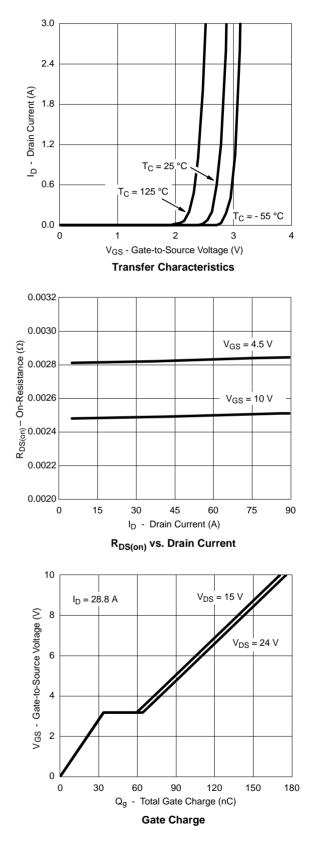
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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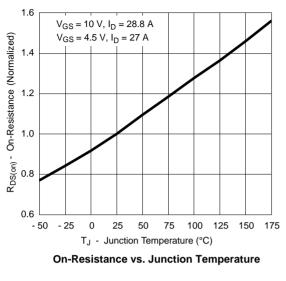




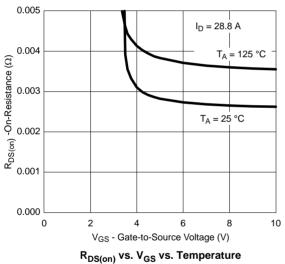
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

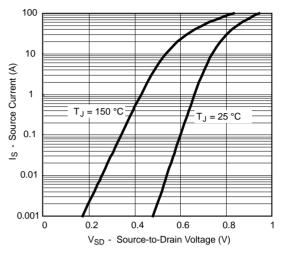




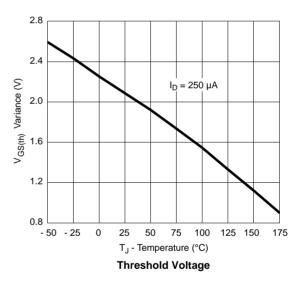


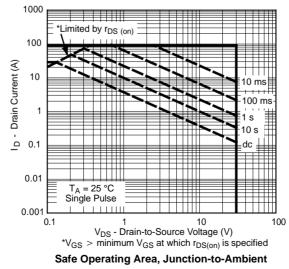
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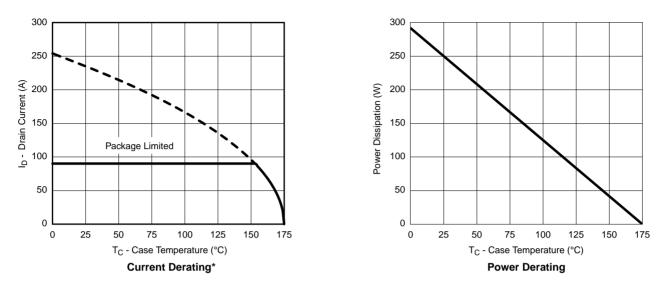


Forward Diode Voltage vs. Temperature



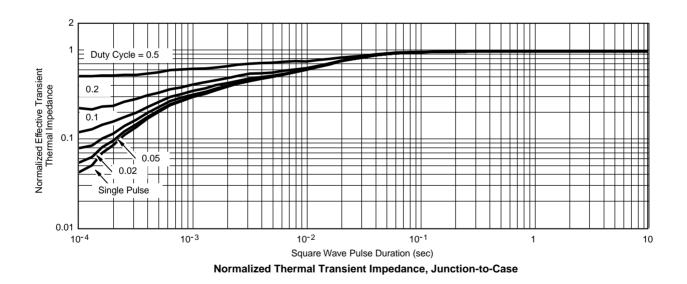






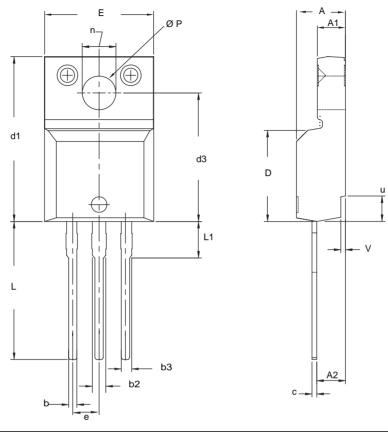
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

*The power dissipation P_D is based on $T_{J(max)} = 175$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





TO-220 FULLPAK (HIGH VOLTAGE)



DIM.	MILLI	METERS	INC	CHES	
	MIN.	MAX.	MIN.	MAX.	
А	4.570	4.830	0.180	0.190	
A1	2.570	2.830	0.101	0.111	
A2	2.510	2.850	0.099	0.112	
b	0.622	0.890	0.024	0.035	
b2	1.229	1.400	0.048	0.055	
b3	1.229	1.400	0.048	0.055	
С	0.440	0.629	0.017	0.025	
D	8.650	9.800	0.341	0.386	
d1	15.88	16.120	0.622	0.635	
d3	12.300	12.920	0.484	0.509	
E	10.360	10.630	0.408	0.419	
е	2.54 BSC		0.100 BSC		
L	13.200	13.730	0.520	0.541	
L1	3.100	3.500	0.122	0.138	
n	6.050	6.150	0.238	0.242	
ØP	3.050	3.450	0.120	0.136	
u	2.400	2.500	0.094	0.098	
V	0.400	0.500	0.016	0.020	

Notes

1. To be used only for process drawing. 2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads. 3. All critical dimensions should C meet $C_{pk} > 1.33$. 4. All dimensions include burrs and plating thickness. 5. No chipping or package damage.



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