

## CEF1195-VB Datasheet

### Power MOSFET

#### PRODUCT SUMMARY

$V_{DS}$ (V)	950	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	2.4
$Q_g$ (Max.) (nC)	28	
$Q_{gs}$ (nC)	5	
$Q_{gd}$ (nC)	12	
Configuration	Single	

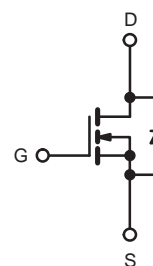
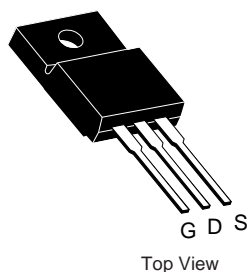
#### FEATURES

- Dynamic  $dV/dt$  Rating
- Repetitive Avalanche Rated
- Isolated Central Mounting Hole
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC



**RoHS\***  
COMPLIANT

TO-220 FULLPAK



N-Channel MOSFET

#### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			$V_{DS}$	950	V
Gate-Source Voltage			$V_{GS}$	$\pm 20$	
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25\text{ }^{\circ}\text{C}$	$I_D$	6	A
		$T_C = 100\text{ }^{\circ}\text{C}$		3.9	
Pulsed Drain Current <sup>a</sup>			$I_{DM}$	24	
Linear Derating Factor				1.5	W/ $^{\circ}\text{C}$
Single Pulse Avalanche Energy <sup>b</sup>			$E_{AS}$	770	mJ
Repetitive Avalanche Current <sup>a</sup>			$I_{AR}$	7.8	A
Repetitive Avalanche Energy <sup>a</sup>			$E_{AR}$	19	mJ
Maximum Power Dissipation	$T_C = 25\text{ }^{\circ}\text{C}$		$P_D$	190	W
Peak Diode Recovery $dV/dt$ <sup>c</sup>			$dV/dt$	5.0	V/ns
Operating Junction and Storage Temperature Range			$T_J, T_{stg}$	- 55 to + 150	$^{\circ}\text{C}$
Soldering Recommendations (Peak Temperature)		for 10 s		300 <sup>d</sup>	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

#### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
 b.  $V_{DD} = 50\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 23\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 7.8\text{ A}$  (see fig. 12).  
 c.  $I_{SD} \leq 7.8\text{ A}$ ,  $dI/dt \leq 140\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq 600\text{ V}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .  
 d. 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.24	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.65	

SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		950	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.98	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 800 V, V <sub>GS</sub> = 0 V		-	-	1	μA
		V <sub>DS</sub> = 640 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	45	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 3.7 A <sup>b</sup>	-	2.4	-	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 100 V, I <sub>D</sub> = 3.7 A <sup>b</sup>		4.5	-	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz, see fig. 5		-	816	-	pF
Output Capacitance	C <sub>oss</sub>			-	68	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	17	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 3.8 A, V <sub>DS</sub> = 400 V, see fig. 6 and 13 <sup>b</sup>	-	-	28	nC
Gate-Source Charge	Q <sub>gs</sub>			-	-	5	
Gate-Drain Charge	Q <sub>gd</sub>			-	-	12	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 400 V, I <sub>D</sub> = 3.8 A, R <sub>g</sub> = 6.2 Ω, R <sub>D</sub> = 52 Ω see fig. 10 <sup>b</sup>		-	15	-	ns
Rise Time	t <sub>r</sub>			-	27	-	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	66	-	
Fall Time	t <sub>f</sub>			-	30	-	
Internal Drain Inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from package and center of die contact		-	5.0	-	nH
Internal Source Inductance	L <sub>S</sub>			-	13	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		-	-	5.0	A
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	21	
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 3.8 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	1.8	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 3.8 A, di/dt = 100 A/μs <sup>b</sup>		-	320		ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			-	3.3		μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

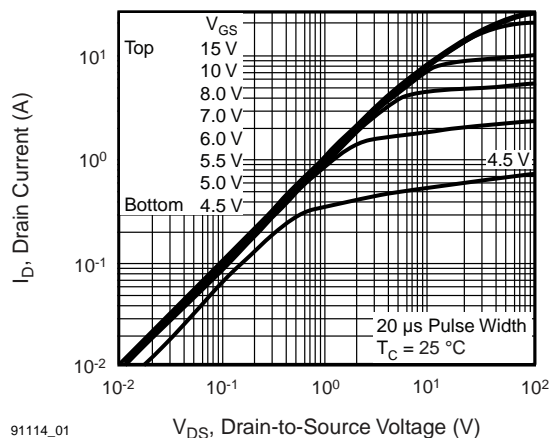


Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^{\circ}\text{C}$

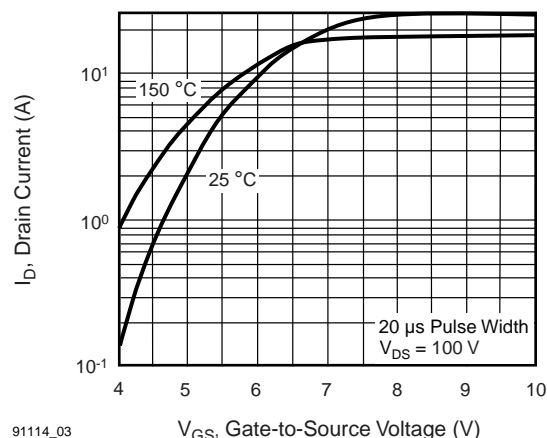


Fig. 3 - Typical Transfer Characteristics

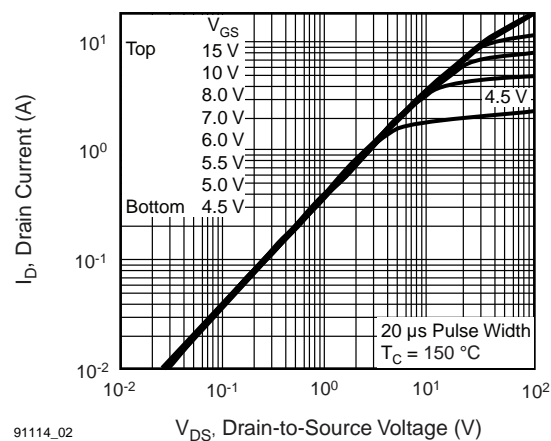


Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^{\circ}\text{C}$

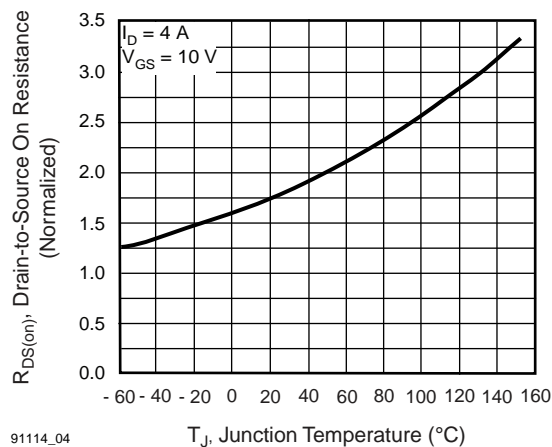
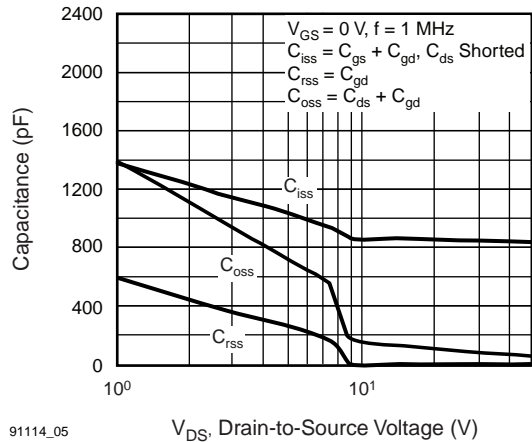
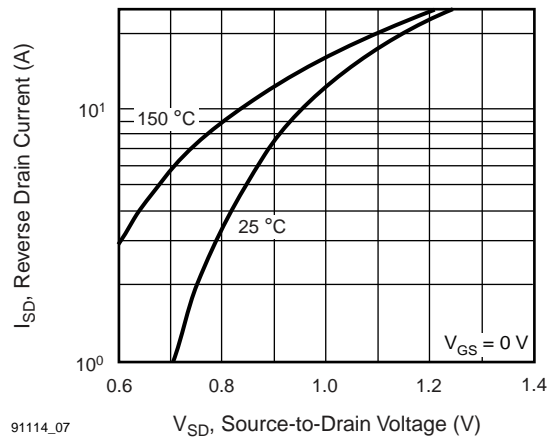


Fig. 4 - Normalized On-Resistance vs. Temperature



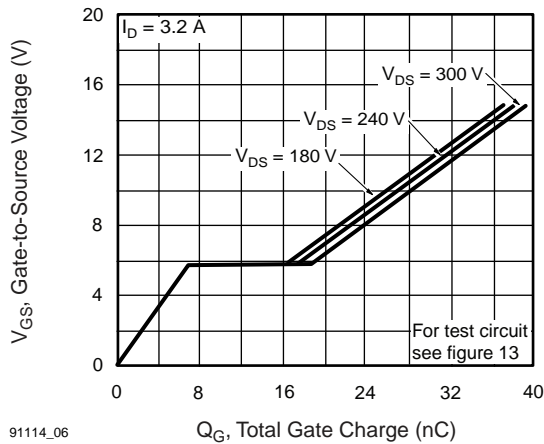
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Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



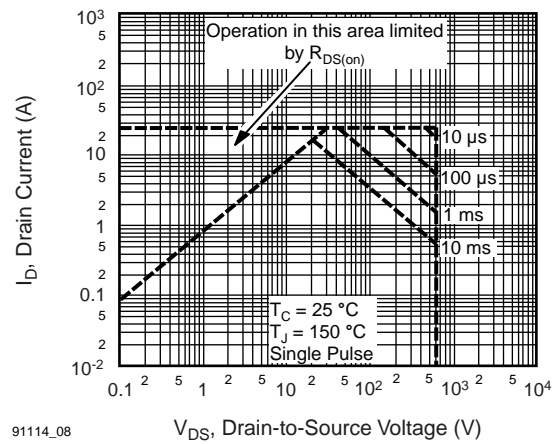
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Fig. 7 - Typical Source-Drain Diode Forward Voltage



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Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



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Fig. 8 - Maximum Safe Operating Area

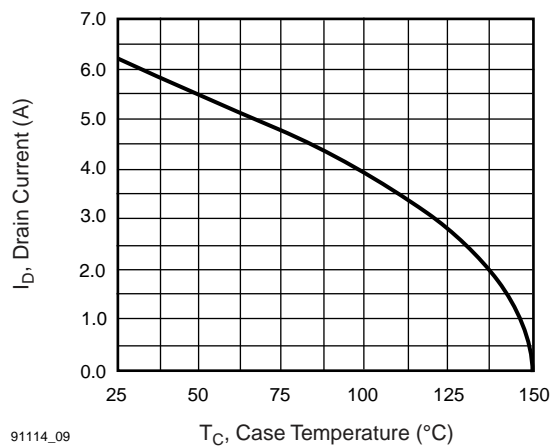


Fig. 9 - Maximum Drain Current vs. Case Temperature

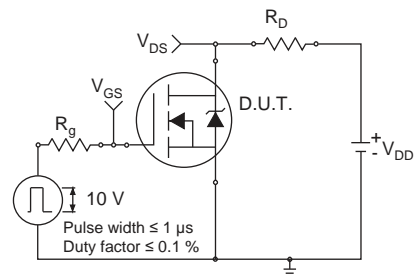


Fig. 10a - Switching Time Test Circuit

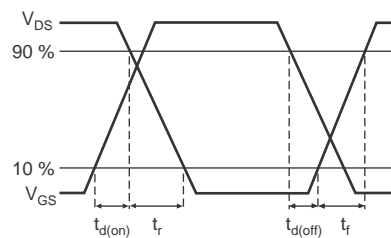


Fig. 10b - Switching Time Waveforms

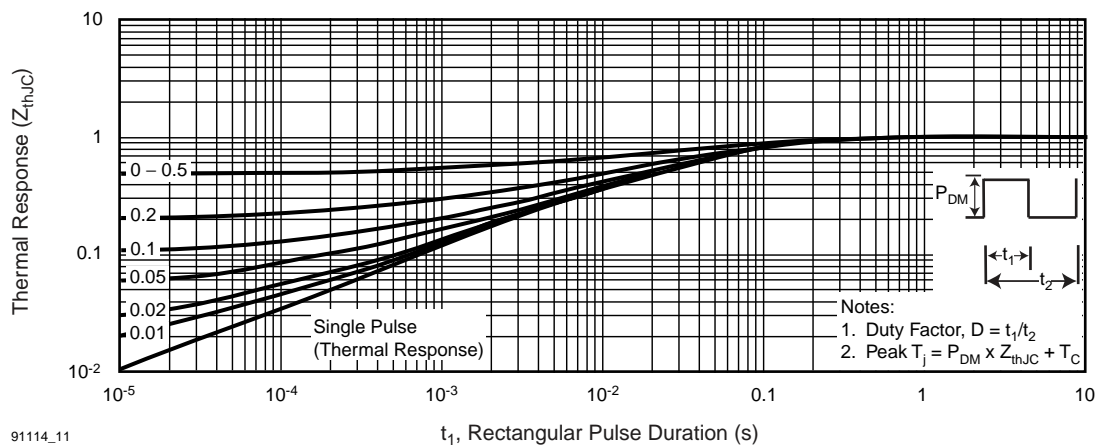


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

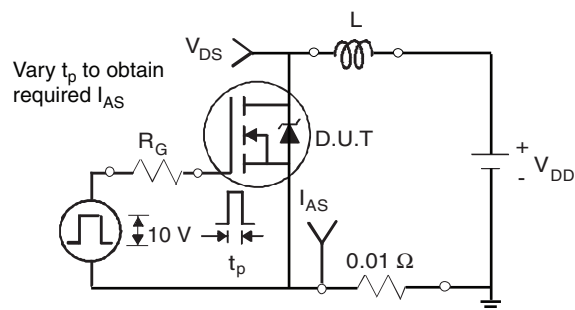


Fig. 12a - Unclamped Inductive Test Circuit

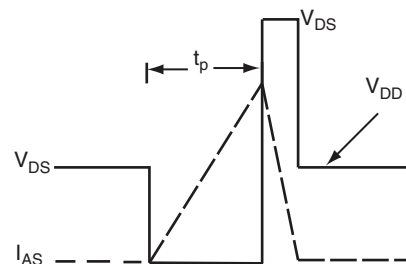


Fig. 12b - Unclamped Inductive Waveforms

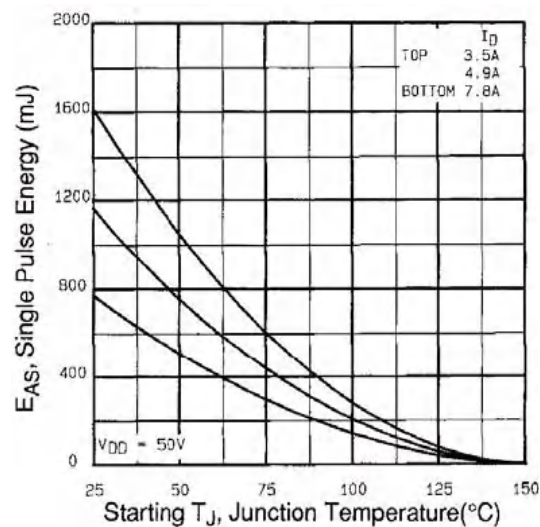


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

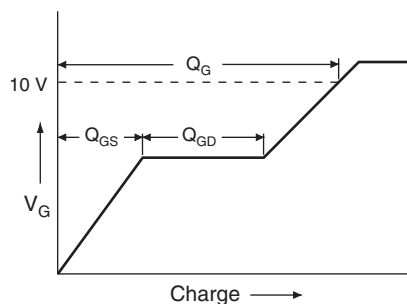


Fig. 13a - Basic Gate Charge Waveform

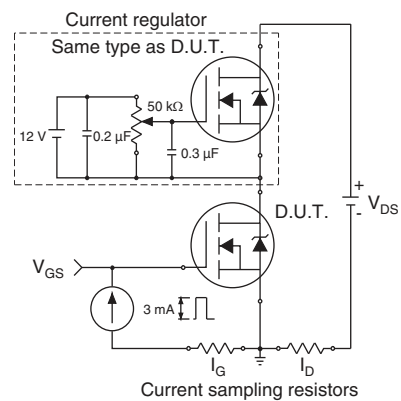


Fig. 13b - Gate Charge Test Circuit

**D.U.T.**

③

②

④

①

$R_g$

$V_{DD}$

Circuit layout considerations

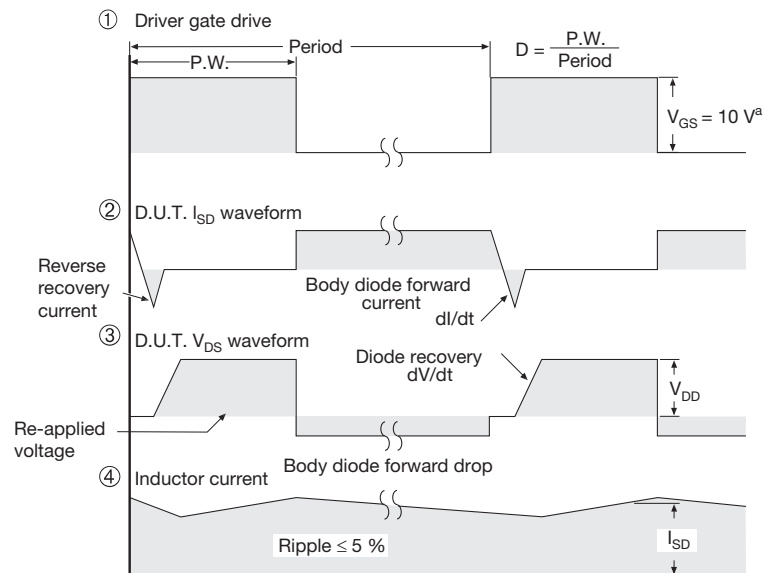
- Low stray inductance
- Ground plane
- Low leakage inductance current transformer

•  $dV/dt$  controlled by  $R_g$

• Driver same type as D.U.T.

•  $I_{SD}$  controlled by duty factor "D"

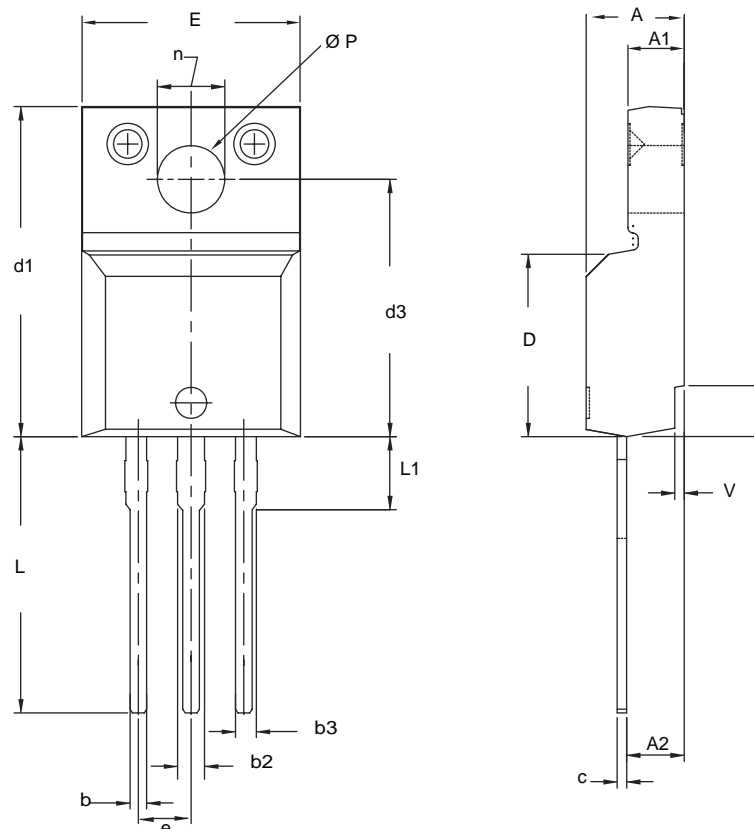
• D.U.T. - device under test



a.  $V_{GS} = 5 \text{ V}$  for logic level devices

7

**TO-220 FULLPAK (HIGH VOLTAGE)**



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
v	0.400	0.500	0.016	0.020

ECN: X09-0126-Rev. B, 26-Oct-09  
DWG: 5972

**Notes**

1. To be used only for process drawing.
2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads.
3. All critical dimensions should C meet  $C_{pk} > 1.33$ .
4. All dimensions include burrs and plating thickness.
5. No chipping or package damage.



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