

## 2SK2101-01MR-VB Datasheet

## N-Channel 800V (D-S) Super Junction Power MOSFET

## PRODUCT SUMMARY

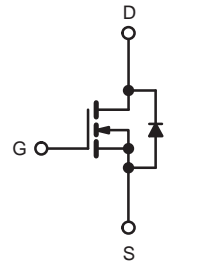
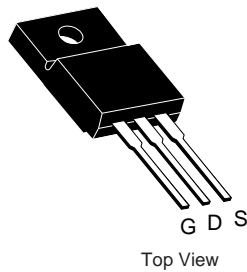
$V_{DS}$ (V)	800	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	1.2
$Q_g$ (Max.) (nC)	200	
$Q_{gs}$ (nC)	24	
$Q_{gd}$ (nC)	110	
Configuration	Single	

## FEATURES

- Dynamic  $dV/dt$  Rating
- Repetitive Avalanche Rated
- Isolated Central Mounting Hole
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC


**RoHS\***  
 COMPLIANT

TO-220 FULLPAK



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V <sub>DS</sub>	800	V
Gate-Source Voltage			V <sub>GS</sub>	± 30	
Continuous Drain Current	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	I <sub>D</sub>	5	A
		T <sub>C</sub> = 100 °C		3.9	
Pulsed Drain Current <sup>a</sup>			I <sub>DM</sub>	21	
Linear Derating Factor				1.5	W/°C
Single Pulse Avalanche Energy <sup>b</sup>			E <sub>AS</sub>	770	mJ
Repetitive Avalanche Current <sup>a</sup>			I <sub>AR</sub>	7.8	A
Repetitive Avalanche Energy <sup>a</sup>			E <sub>AR</sub>	19	mJ
Maximum Power Dissipation	T <sub>C</sub> = 25 °C		P <sub>D</sub>	190	W
Peak Diode Recovery dV/dt <sup>c</sup>			dV/dt	2.0	V/ns
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)		for 10 s		300 <sup>d</sup>	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

## Notes

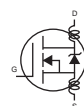

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
 b.  $V_{DD} = 50\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 23\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 7.8\text{ A}$  (see fig. 12).  
 c.  $I_{SD} \leq 7.8\text{ A}$ ,  $dI/dt \leq 140\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq 600\text{ V}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .  
 d. 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.24	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.65	

**SPECIFICATIONS** ( $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$		800	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^{\circ}\text{C}$ , $I_D = 1\text{ mA}$		-	0.98	-	V/ $^{\circ}\text{C}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 800\text{ V}$ , $V_{GS} = 0\text{ V}$		-	-	100	$\mu\text{A}$
		$V_{DS} = 640\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 125\text{ }^{\circ}\text{C}$		-	-	500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 3.7\text{ A}^b$	-	1.2	-	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 100\text{ V}$ , $I_D = 3.7\text{ A}^b$		5.6	-	-	S
Dynamic							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 25\text{ V}$ , $f = 1.0\text{ MHz}$ , see fig. 5		-	3100	-	pF
Output Capacitance	$C_{oss}$			-	800	-	
Reverse Transfer Capacitance	$C_{rss}$			-	490	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 3.8\text{ A}$ , $V_{DS} = 400\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	200	nC
Gate-Source Charge	$Q_{gs}$			-	-	24	
Gate-Drain Charge	$Q_{gd}$			-	-	110	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 400\text{ V}$ , $I_D = 3.8\text{ A}$ , $R_g = 6.2\text{ }\Omega$ , $R_D = 52\text{ }\Omega$ see fig. 10 <sup>b</sup>		-	19	-	ns
Rise Time	$t_r$			-	38	-	
Turn-Off Delay Time	$t_{d(off)}$			-	120	-	
Fall Time	$t_f$			-	39	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact 		-	5.0	-	nH
Internal Source Inductance	$L_S$			-	13	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	5.0	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	21	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^{\circ}\text{C}$ , $I_S = 3.8\text{ A}$ , $V_{GS} = 0\text{ V}^b$		-	-	1.8	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^{\circ}\text{C}$ , $I_F = 3.8\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}^b$		-	650	980	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	3.8	5.7	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
 b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

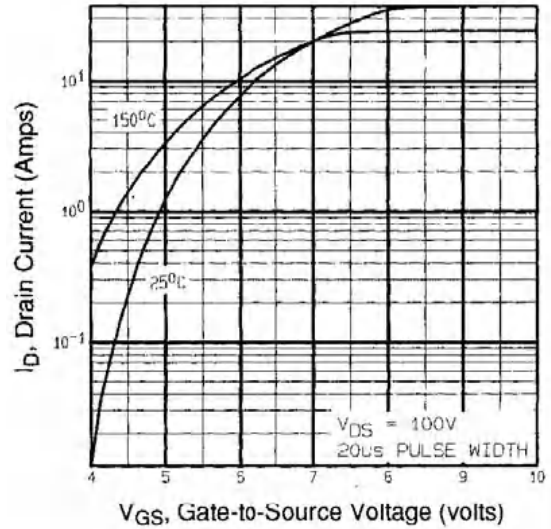
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^{\circ}\text{C}$ 

Fig. 3 - Typical Transfer Characteristics

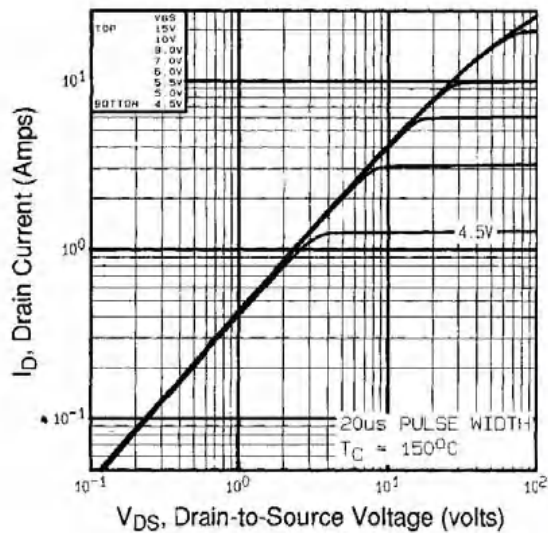
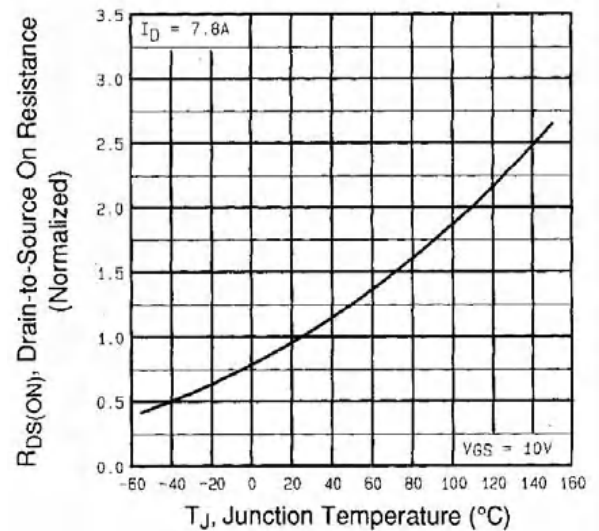
Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^{\circ}\text{C}$ 

Fig. 4 - Normalized On-Resistance vs. Temperature



Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



Fig. 7 - Typical Source-Drain Diode Forward Voltage



Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



Fig. 8 - Maximum Safe Operating Area

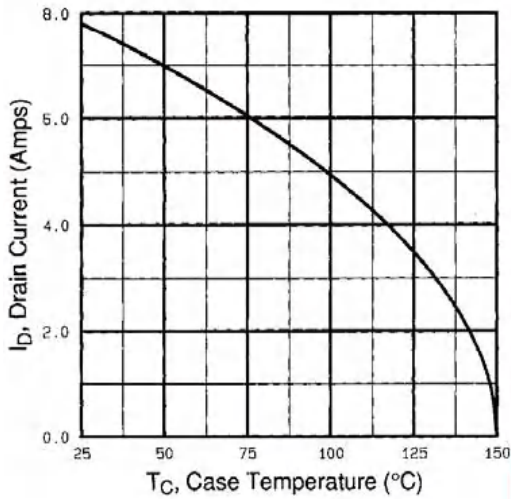


Fig. 9 - Maximum Drain Current vs. Case Temperature

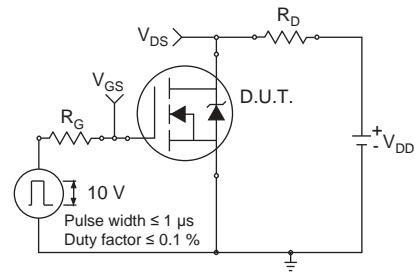


Fig. 10a - Switching Time Test Circuit

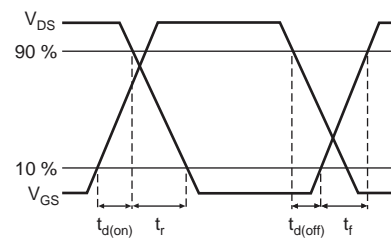


Fig. 10b - Switching Time Waveforms

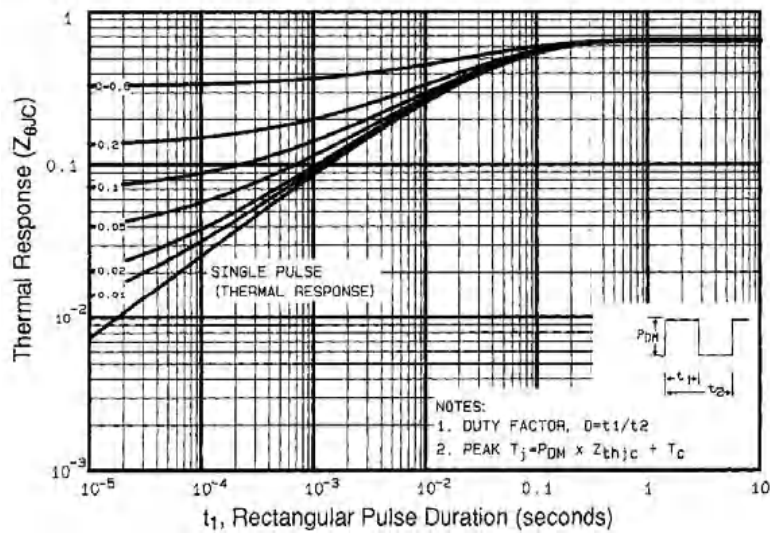


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



Fig. 12a - Unclamped Inductive Test Circuit

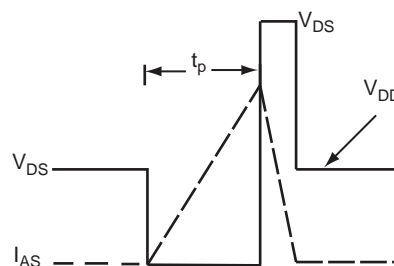


Fig. 12b - Unclamped Inductive Waveforms



Fig. 12c - Maximum Avalanche Energy vs. Drain Current



Fig. 13a - Basic Gate Charge Waveform

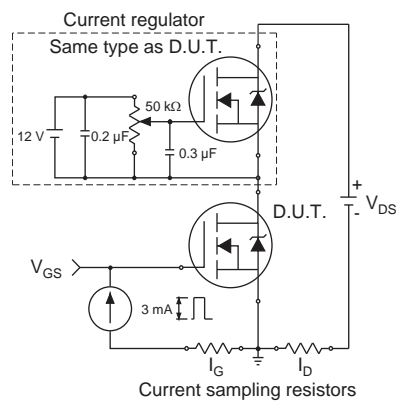
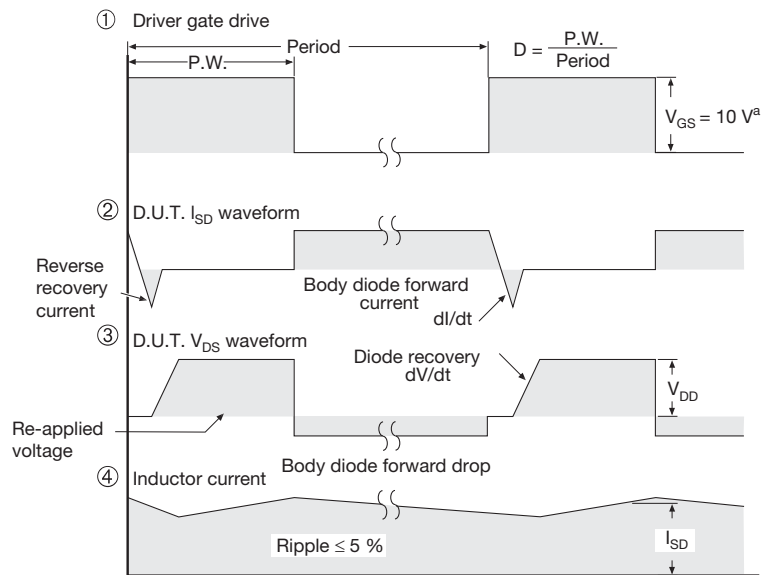
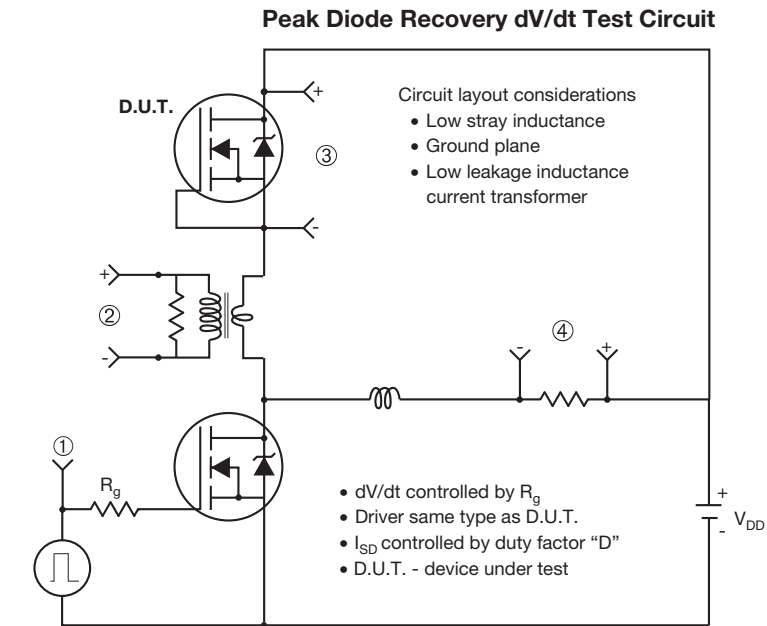


Fig. 13b - Gate Charge Test Circuit

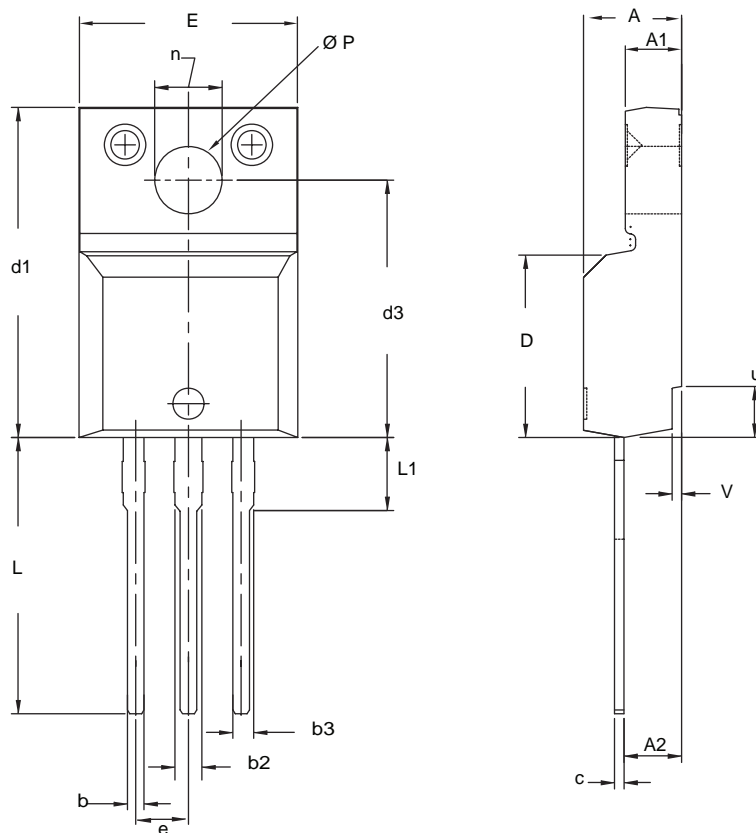




**Note**

a.  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 14 - For N-Channel**

**TO-220 FULLPAK (HIGH VOLTAGE)**

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
v	0.400	0.500	0.016	0.020

ECN: X09-0126-Rev. B, 26-Oct-09  
 DWG: 5972

**Notes**

1. To be used only for process drawing.
2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads.
3. All critical dimensions should C meet  $C_{pk} > 1.33$ .
4. All dimensions include burrs and plating thickness.
5. No chipping or package damage.



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