

2N90L-TF3-T-VB Datasheet

N-Channel 950 V (D-S) Power MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	950				
R _{DS(on)} (Ω)	V _{GS} = 10 V 3.5				
Q _g (Max.) (nC)	78				
Q _{gs} (nC)	10				
Q _{gd} (nC)	42				
Configuration	Single				

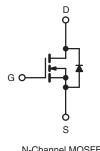
FEATURES

- · Isolated Package
- High Voltage Isolation = 2.5 kV_{RMS} (t = 60 s; f = 60 Hz)
- Sink to Lead Creepage Distance = 4.8 mm
- · Dynamic dV/dt Rating
- · Low Thermal Resistance
- Lead (Pb)-free Available



COMPLIANT





ABSOLUTE MAXIMUM RATINGS $T_C = 25 \degree C$, unless otherwise noted						
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			V _{DS}	950	V	
Gate-Source Voltage			V _{GS}	± 20	1 ^v	
Continuous Drain Current	inuous Drain Current V_{GS} at 10 V $T_C = 25 \degree C$		1-	3.0		
V_{GS} at 10 V $T_{C} = 100 ^{\circ}C$			I _D	2.3	A	
Pulsed Drain Current ^a			I _{DM}	10	1	
Linear Derating Factor				0.28	W/°C	
Single Pulse Avalanche Energy ^b			E _{AS}	220	mJ	
Repetitive Avalanche Current ^a			I _{AR}	1.9	A	
Repetitive Avalanche Energy ^a			E _{AR}	3.5	mJ	
Maximum Power Dissipation T _C = 25 °C			PD	35	W	
Peak Diode Recovery dV/dt ^c			dV/dt	1.5	V/ns	
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150	°C	
Soldering Recommendations (Peak Temperature)	for	10 s		300 ^d		
Mounting Torque	6-32 or M3 screw			10	lbf ⋅ in	
Mounting Torque 6-			F	1.1	N · m	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. $V_{DD} = 50$ V, starting $T_J = 25$ °C, L = 115 mH, $R_G = 25 \Omega$, $I_{AS} = 1.9$ A (see fig. 12). c. $I_{SD} \leq 3.6$ A, dl/dt ≤ 70 A/µs, $V_{DD} \leq 600$, $T_J \leq 150$ °C.

d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

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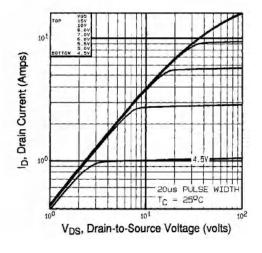
THERMAL RESISTANCE RATINGS								
PARAMETER	SYMBOL	TYP. MAX.			UNIT			
Maximum Junction-to-Ambient	R _{thJA}	- 65			°C 44/			
Maximum Junction-to-Case (Drain)	R _{thJC}	- 3.6			°C/W			
SPECIFICATIONS $T_J = 25 \ ^{\circ}C$,	unless otherw	ise noted			1	T	T	
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static						1	1	
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} =	= 0 V, I _D = 2	50 μΑ	950	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference	e to 25 °C,	$I_D = 1 \text{ mA}$	-	1.1	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} =	= V _{GS} , I _D = 2	250 μΑ	2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	,	$V_{GS} = \pm 20$	V	-	-	± 100	nA
Zero Gate Voltage Drain Current	lass	V _{DS} =	= 900 V, V _G s	₆ = 0 V	-	-	100	
Zelo Gale Voltage Dialit Guiterit	IDSS	V _{DS} = 720 V	$V_{DS} = 720 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 125 ^{\circ}\text{C}$		-	-	500	μΑ
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V I _D = 1.1 A ^b		-	3.5	-	Ω	
Forward Transconductance	g fs	$V_{DS} = 50 \text{ V}, \text{ I}_{D} = 1.1 \text{ A}^{b}$		1.7	-	-	S	
Dynamic								
Input Capacitance	C _{iss}	$V_{GS} = 0 V,$ $V_{DS} = 25 V,$		-	1200	-		
Output Capacitance	C _{oss}			-	320	-		
Reverse Transfer Capacitance	C _{rss}	f = 1.	.0 MHz, see	e fig. 5	-	200	-	pF
Drain to Sink Capacitance	С	f = 1.0 MHz		-	12	-		
Total Gate Charge	Qg	$V_{GS} = 10 \text{ V} \qquad \begin{array}{c} I_D = 3.6 \text{ A}, \text{ V}_{DS} = 360 \text{ V},\\ \text{see fig. 6 and } 13^{\text{b}} \end{array}$		-	-	78	nC	
Gate-Source Charge	Q _{gs}			-	-	10		
Gate-Drain Charge	Q _{gd}			-	-	42		
Turn-On Delay Time	t _{d(on)}	$\label{eq:V_DD} \begin{array}{l} V_{DD} = 450 \ \text{V}, \ \text{I}_{D} = 3.6 \ \text{A}, \\ R_{G} = 12 \ \Omega, \ R_{D} = 120 \ \Omega, \\ \text{see fig. } 10^{b} \end{array}$		-	14	-	ns	
Rise Time	t _r			-	25	-		
Turn-Off Delay Time	t _{d(off)}			-	90	-		
Fall Time	t _f			-	30	-		
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-		
Internal Source Inductance	Ls			-	7.5	-	nH	
Drain-Source Body Diode Characteristic	cs							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	1.9	A	
Pulsed Diode Forward Current ^a	I _{SM}			-	-	7.6		
Body Diode Voltage	V _{SD}	T _J = 25 °C	, I _S = 1.9 A,	$V_{GS} = 0 \ V^{b}$	-	-	1.8	V
Body Diode Reverse Recovery Time	t _{rr}	T 05 °C I	- 36 4 4	/dt - 100 A/uch	-	430	650	ns
Body Diode Reverse Recovery Charge	Q _{rr}	i j = 25 °C, I _F	= 3.6 A, dl/	′dt = 100 A/μs ^b	-	1.4	2.1	μC
Forward Turn-On Time	t _{on}	Intrinsic tu	Irn-on time	s negligible (turn	-on is don	ninated by	y L _S and I	_D)

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width \leq 300 $\mu s;$ duty cycle \leq 2 %.





TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Fig. 1 - Typical Output Characteristics, T_C = 25 °C

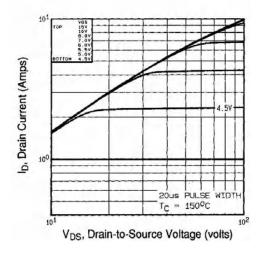


Fig. 2 - Typical Output Characteristics, $T_C = 150 \ ^\circ C$

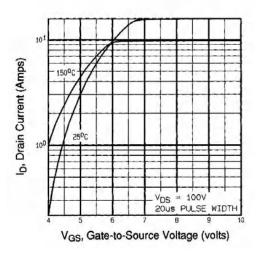


Fig. 3 - Typical Transfer Characteristics

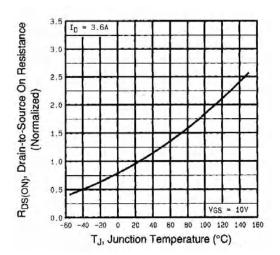


Fig. 4 - Normalized On-Resistance vs. Temperature



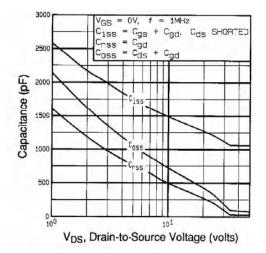


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

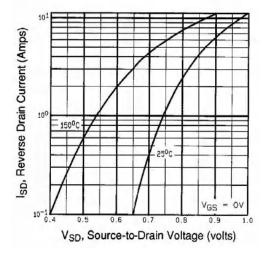


Fig. 7 - Typical Source-Drain Diode Forward Voltage

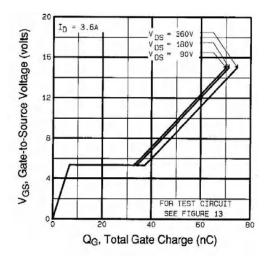


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

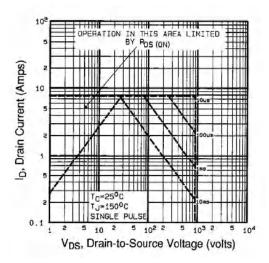


Fig. 8 - Maximum Safe Operating Area



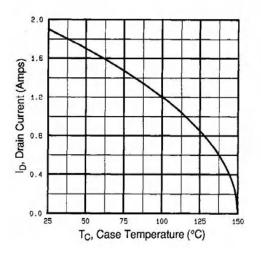


Fig. 9 - Maximum Drain Current vs. Case Temperature

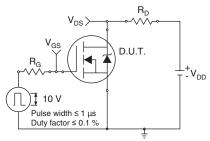


Fig. 10a - Switching Time Test Circuit

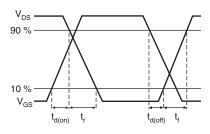


Fig. 10b - Switching Time Waveforms

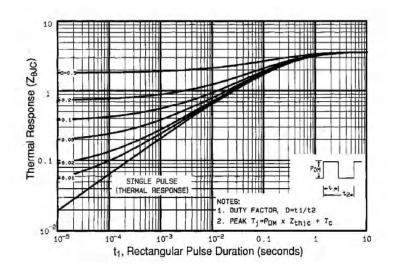


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

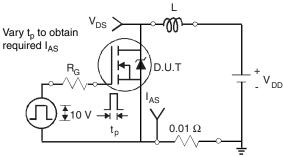


Fig. 12a - Unclamped Inductive Test Circuit

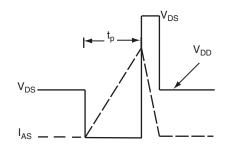


Fig. 12b - Unclamped Inductive Waveforms



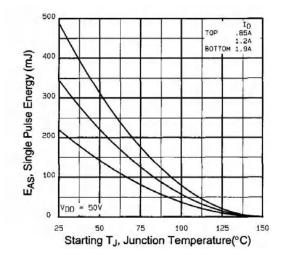


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

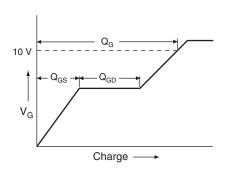
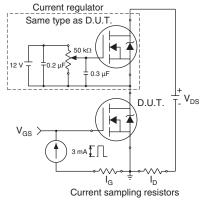
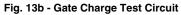
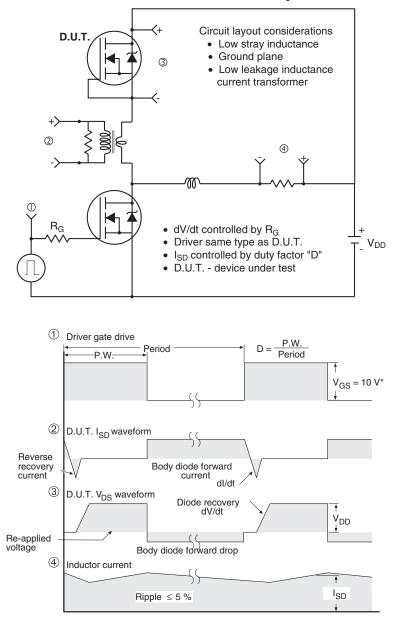


Fig. 13a - Basic Gate Charge Waveform









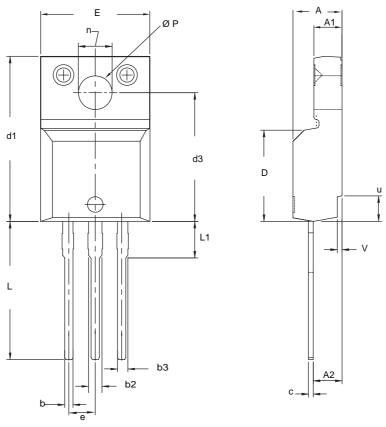
Peak Diode Recovery dV/dt Test Circuit

* $V_{GS} = 5 V$ for logic level devices

Fig.14 - For N-Channel



TO-220 FULLPAK (HIGH VOLTAGE)



	MILLI	METERS	INC	HES
DIM.	MIN.	MAX.	MIN.	MAX.
А	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
C	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
е	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
V	0.400	0.500	0.016	0.020
ECN: X09-0126-Rev. B, 2 DWG: 5972	26-Oct-09		•	·

Notes

1. To be used only for process drawing. 2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads. 3. All critical dimensions should C meet $C_{pk} > 1.33$. 4. All dimensions include burrs and plating thickness. 5. No chipping or package damage.



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