

13N50L-TF3-T-VB Datasheet

N-Channel 550V (D-S) Power MOSFET**PRODUCT SUMMARY**

V_{DS} (V)	550	
$R_{DS(on)}$ at 25 °C (Ω)	$V_{GS} = 10\text{ V}$	0.26
Q_g max. (nC)	150	
Q_{gs} (nC)	12	
Q_{gd} (nC)	25	
Configuration	Single	

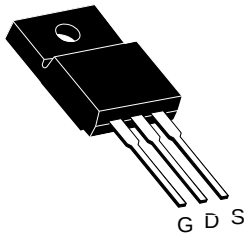
FEATURES

- Optimal Design
 - Low Area Specific On-Resistance
 - Low Input Capacitance (C_{iss})
 - Reduced Capacitive Switching Losses
 - High Body Diode Ruggedness
 - Avalanche Energy Rated (UIS)
- Optimal Efficiency and Operation
 - Low Cost
 - Simple Gate Drive Circuitry
 - Low Figure-of-Merit (FOM): $R_{on} \times Q_g$
 - Fast Switching

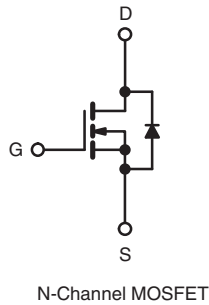


RoHS*
 COMPLIANT
 HALOGEN
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 Available

TO-220 FULLPAK



Top View

**APPLICATIONS**

- Consumer Electronics
 - Displays (LCD or Plasma TV)
- Server and Telecom Power Supplies
 - SMPS
- Industrial
 - Welding
 - Induction Heating
 - Motor Drives
- Battery Chargers
- SMPS
 - Power Factor Correction (PFC)

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ °C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	550	V
Gate-Source Voltage	V_{GS}	± 20	
Gate-Source Voltage AC ($f > 1\text{ Hz}$)		30	
Continuous Drain Current ($T_J = 150\text{ °C}$)	V_{GS} at 10 V	$T_C = 25\text{ °C}$	A
		$T_C = 100\text{ °C}$	
Pulsed Drain Current ^a	I_{DM}	56	
Linear Derating Factor		2.2	W/°C
Single Pulse Avalanche Energy ^b	E_{AS}	281	mJ
Maximum Power Dissipation	P_D	60	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	°C
Drain-Source Voltage Slope	dV/dt	$T_J = 125\text{ °C}$	V/ns
Reverse Diode dV/dt ^d		24	
Soldering Recommendations (Peak Temperature)		0.36	
		300°	°C

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ °C}$, $L = 10\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 7.5\text{ A}$.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, starting $T_J = 25\text{ °C}$.

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.45	

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		550	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 250 μA		-	0.56	-	V/°C
Gate-Source Threshold Voltage (N)	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2	-	4	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 500 V, V _{GS} = 0 V		-	-	1	μA
		V _{DS} = 400 V, V _{GS} = 0 V, T _J = 125 °C		-	-	10	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 10 A	-	0.26	-	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 10 A		-	12	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 100 V, f = 1 MHz		-	3094	-	pF
Output Capacitance	C _{oss}			-	152	-	
Reverse Transfer Capacitance	C _{rss}			-	13	-	
Effective output capacitance, energy related ^a	C _{o(er)}	V _{GS} = 0 V, V _{DS} = 0 V to 400 V		-	131	-	
Effective output capacitance, time related ^b	C _{o(tr)}			-	189	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 10 A, V _{DS} = 400 V	-	80	150	nC
Gate-Source Charge	Q _{gs}			-	12	-	
Gate-Drain Charge	Q _{gd}			-	25	-	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 400 V, I _D = 10 A, V _{GS} = 10 V, R _g = 9.1 Ω		-	24	50	ns
Rise Time	t _r			-	31	62	
Turn-Off Delay Time	t _{d(off)}			-	117	176	
Fall Time	t _f			-	56	112	
Gate Input Resistance	R _g	f = 1 MHz, open drain		-	1.8	-	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	20	A
Pulsed Diode Forward Current	I _{SM}			-	-	80	
Diode Forward Voltage	V _{SD}	T _J = 25 °C, I _S = 10 A, V _{GS} = 0 V		-	-	1.2	V
Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = I _S = 10 A, dI/dt = 100 A/μs, V _R = 20 V		-	437	-	ns
Reverse Recovery Charge	Q _{rr}			-	5.9	-	μC
Reverse Recovery Current	I _{RRM}			-	25	-	A

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .
 b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

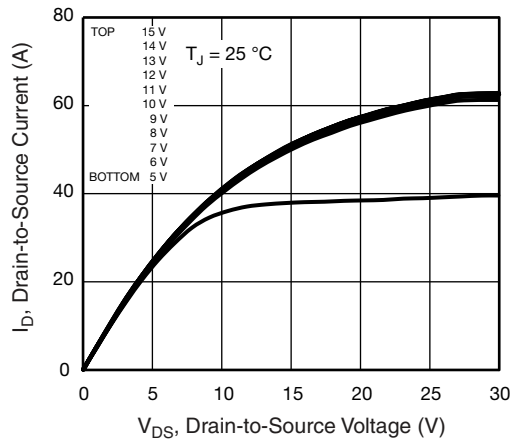


Fig. 1 - Typical Output Characteristics

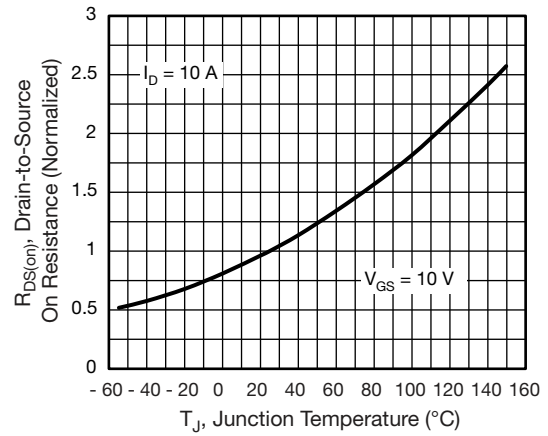


Fig. 4 - Normalized On-Resistance vs. Temperature

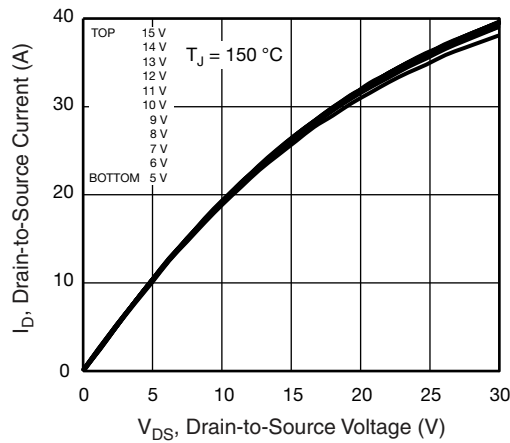


Fig. 2 - Typical Output Characteristics

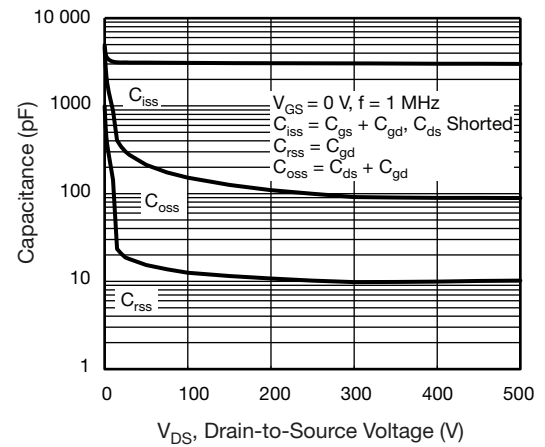


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

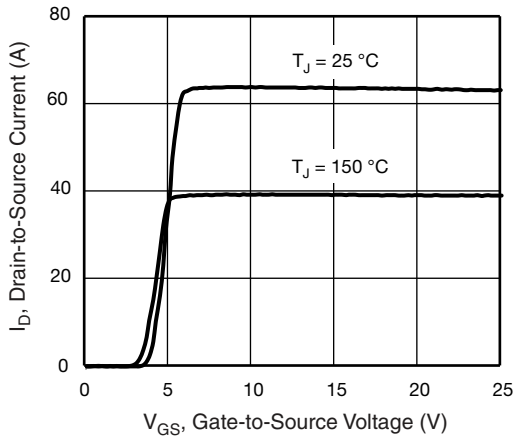


Fig. 3 - Typical Transfer Characteristics

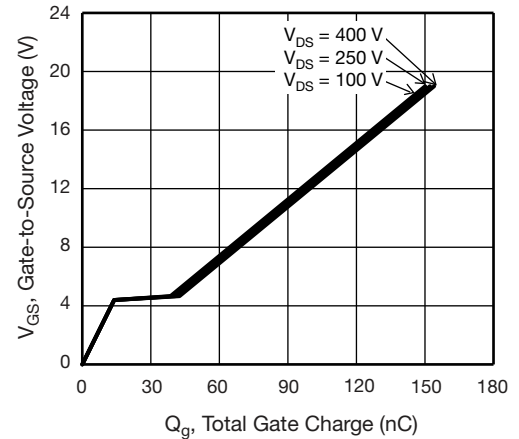


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

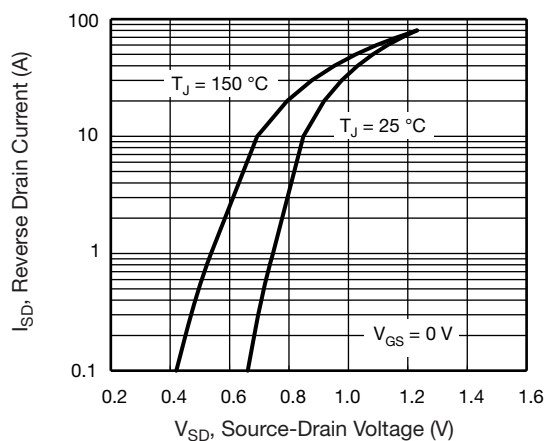


Fig. 7 - Typical Source-Drain Diode Forward Voltage

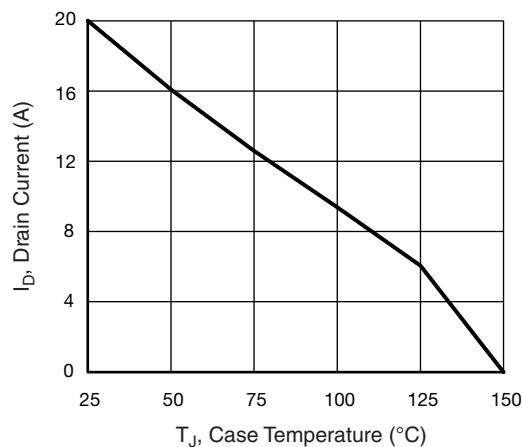


Fig. 9 - Maximum Drain Current vs. Case Temperature

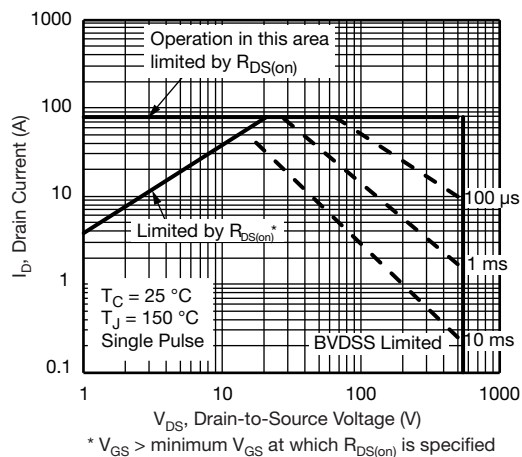


Fig. 8 - Maximum Safe Operating Area

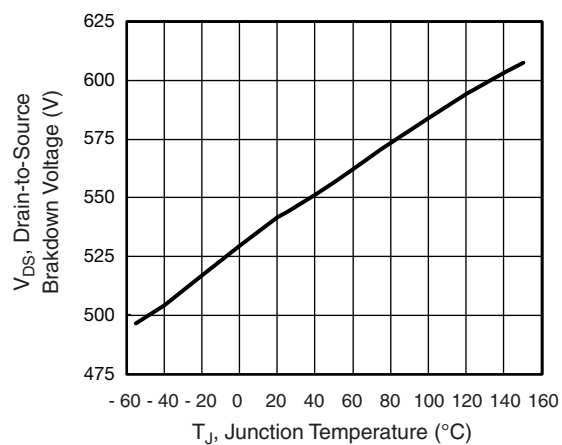


Fig. 10 - Temperature vs. Drain-to-Source Voltage

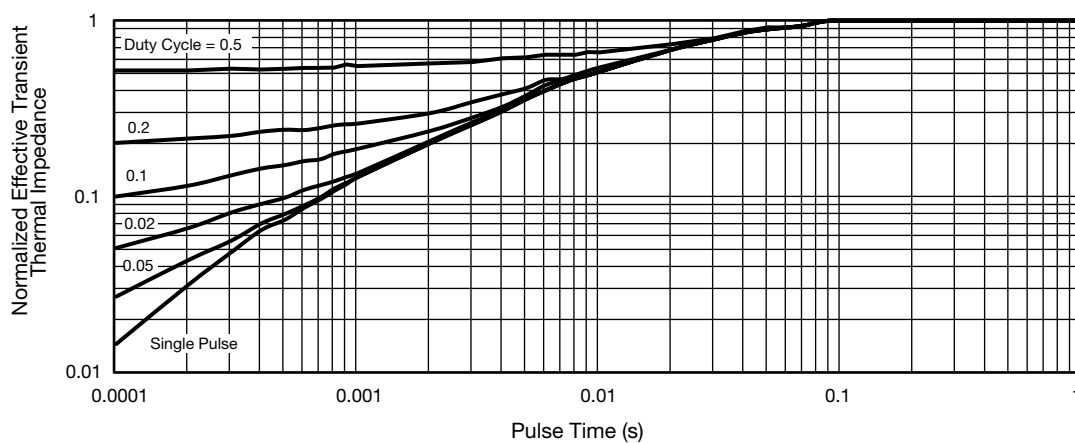


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

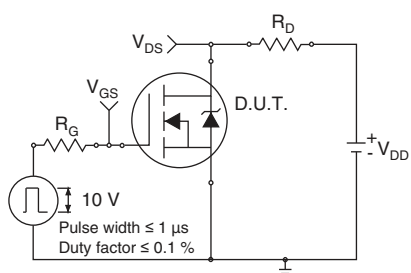


Fig. 12 - Switching Time Test Circuit

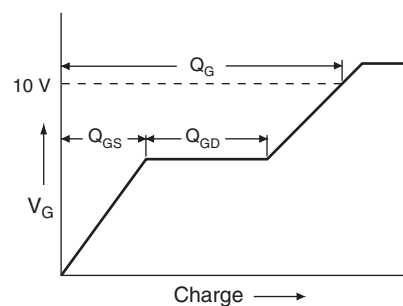


Fig. 16 - Basic Gate Charge Waveform

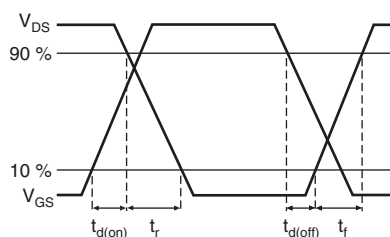


Fig. 13 - Switching Time Waveforms

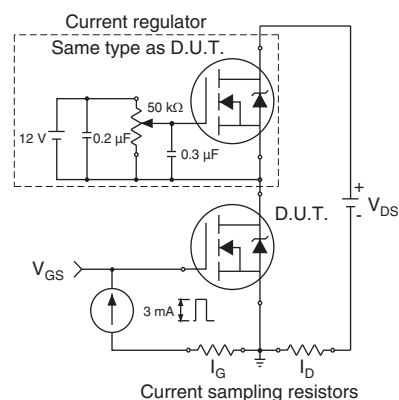


Fig. 17 - Gate Charge Test Circuit

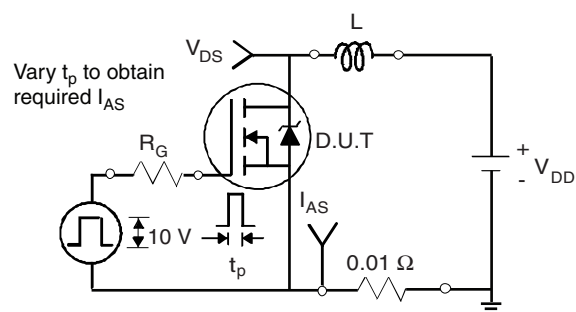


Fig. 14 - Unclamped Inductive Test Circuit

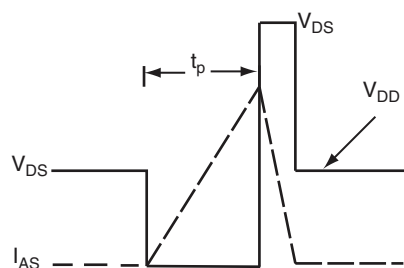
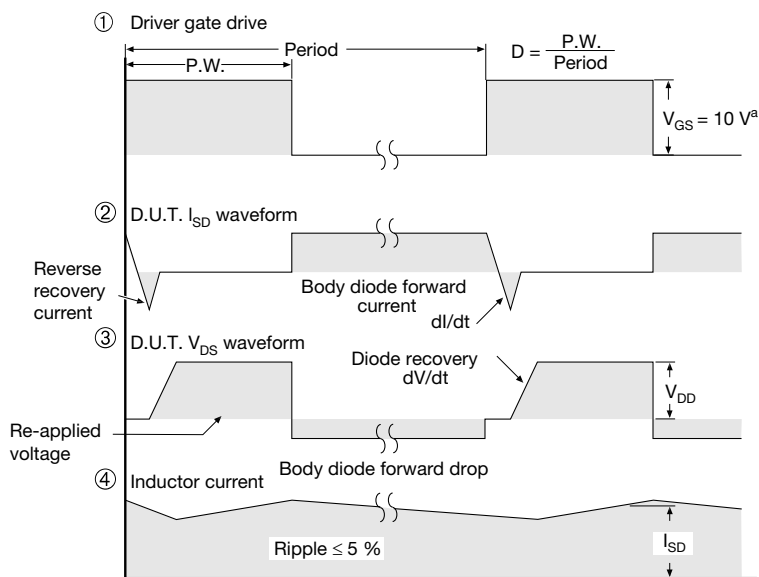
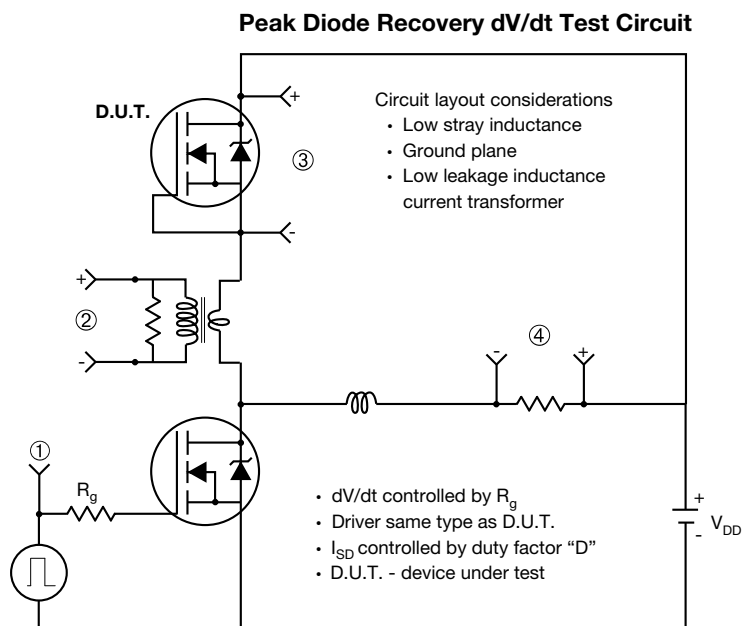
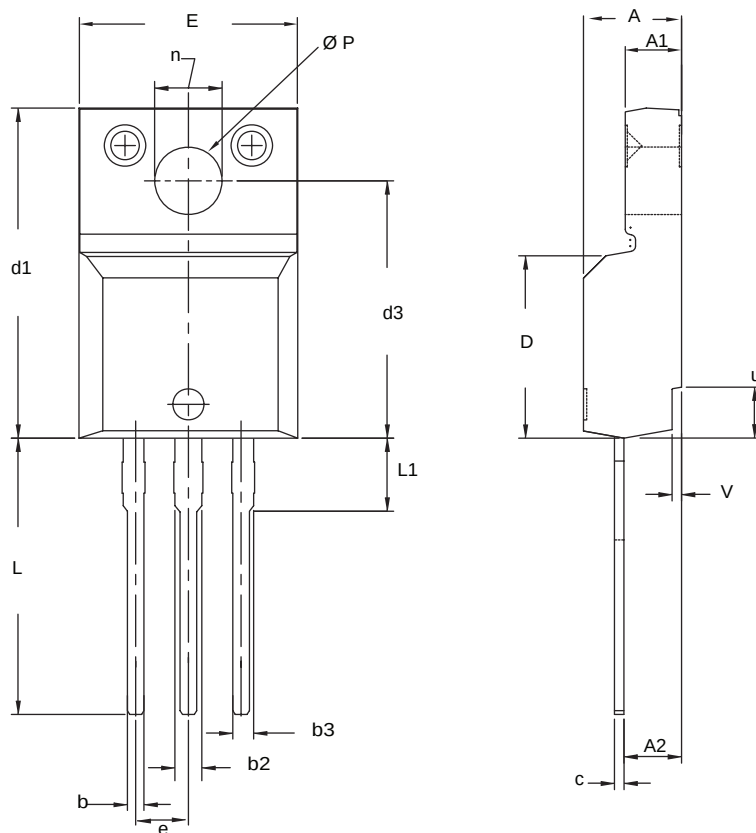


Fig. 15 - Unclamped Inductive Waveforms

**Note**a. $V_{GS} = 5\text{ V}$ for logic level devices**Fig. 18 - For N-Channel**

TO-220 FULLPAK (HIGH VOLTAGE)

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
v	0.400	0.500	0.016	0.020

ECN: X09-0126-Rev. B, 26-Oct-09
 DWG: 5972

Notes

1. To be used only for process drawing.
2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads.
3. All critical dimensions should C meet $C_{pk} > 1.33$.
4. All dimensions include burrs and plating thickness.
5. No chipping or package damage.

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