

WSR18P10-VB Datasheet

P-Channel 100 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY

V_{DS} (V)	- 100
$R_{DS(on)}$ (Ω) at $V_{GS} = -10$ V	0.033
$R_{DS(on)}$ (Ω) at $V_{GS} = -4.5$ V	0.037
I_D (A)	- 50
Configuration	Single

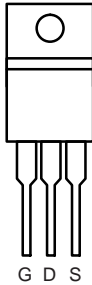
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Trench Power MOSFET
- Package with Low Thermal Resistance
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



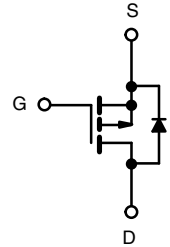
RoHS
COMPLIANT
HALOGEN
FREE

TO-220AB



G D S

Top View



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	- 100	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	I_D	- 50	A
		- 30	
Continuous Source Current (Diode Conduction) ^a	I_S	- 50	
Pulsed Drain Current ^b	I_{DM}	- 180	
Single Pulse Avalanche Current	I_{AS}	- 44	
Single Pulse Avalanche Energy	E_{AS}	96	mJ
Maximum Power Dissipation ^b	P_D	136	W
		45	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 175	°C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	R_{thJA}	50	°C/W
Junction-to-Case (Drain)	R_{thJC}	1.1	

Notes

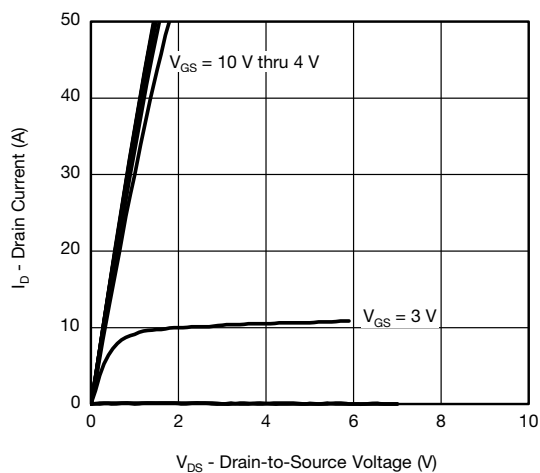
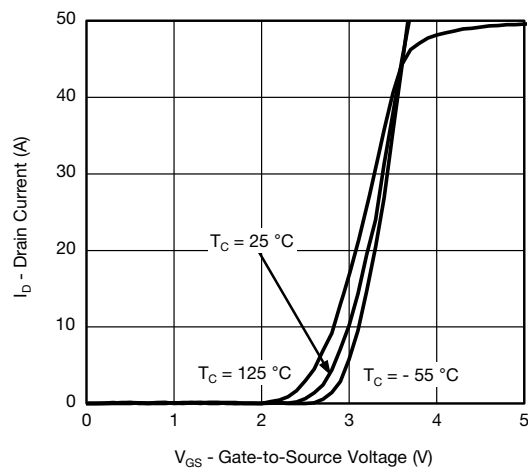
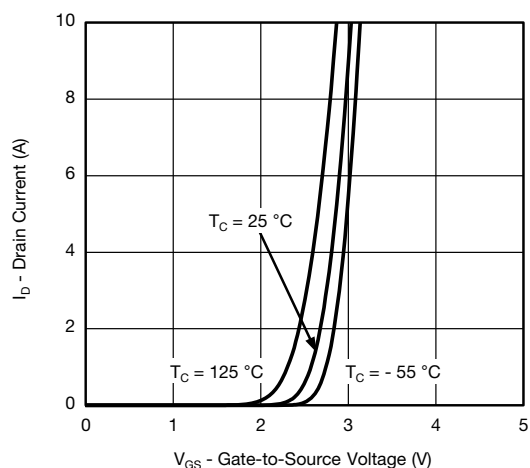
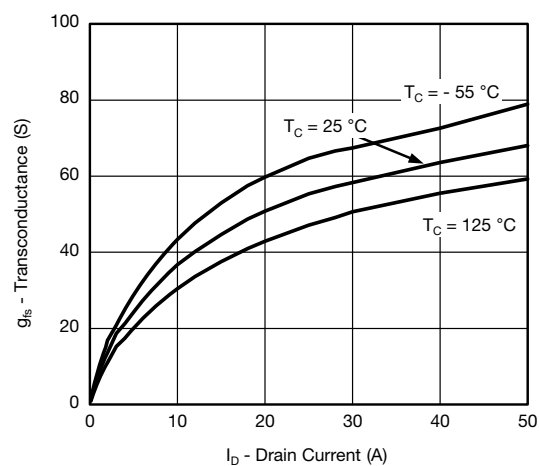
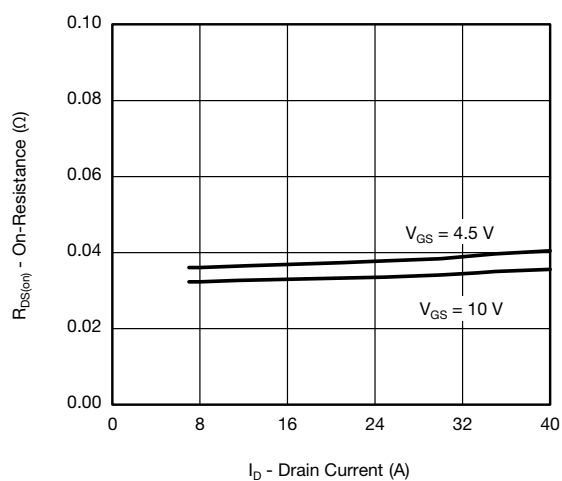
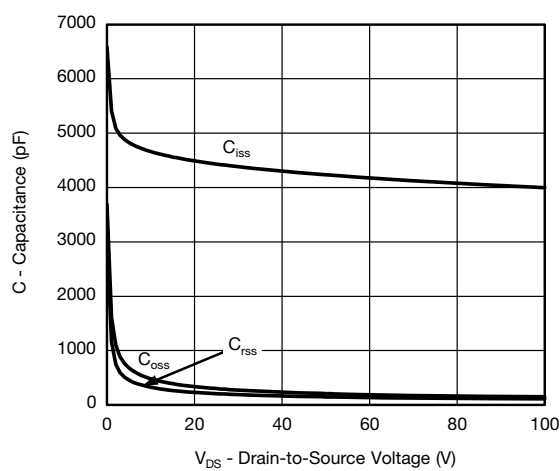
- Package limited.
- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR-4 material).
- Parametric verification ongoing.

SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA		- 100	-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA		- 1.0	-	-2.5	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V	V _{DS} = - 100 V	-	-	- 1	μA
		V _{GS} = 0 V	V _{DS} = - 100 V, T _J = 125 °C	-	-	- 50	
		V _{GS} = 0 V	V _{DS} = - 100 V, T _J = 175 °C	-	-	- 250	
On-State Drain Current ^a	I _{D(on)}	V _{GS} = - 10 V	V _{DS} ≤ - 5 V	- 30	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 10 V	I _D = - 9.2 A	-	0.033	-	Ω
		V _{GS} = - 10 V	I _D = - 9.2 A, T _J = 125 °C	-	0.074	-	
		V _{GS} = - 10 V	I _D = - 9.2 A, T _J = 175 °C	-	0.093	-	
		V _{GS} = - 4.5 V	I _D = - 7.7 A	-	0.037	-	
Forward Transconductance ^b	g _{fs}	V _{DS} = - 15 V, I _D = - 9.2 A		-	35	-	S
Dynamic ^b							
Input Capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = - 25 V, f = 1 MHz	-	4433	5545	pF
Output Capacitance	C _{oss}			-	301	380	
Reverse Transfer Capacitance	C _{rss}			-	208	260	
Total Gate Charge ^c	Q _g	V _{GS} = - 10 V	V _{DS} = - 50V, I _D = - 9.2 A	-	96	144	nC
Gate-Source Charge ^c	Q _{gs}			-	8.4	-	
Gate-Drain Charge ^c	Q _{gd}			-	23.5	-	
Gate Resistance	R _g	f = 1 MHz		1.5	3.13	4.7	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = - 50 V, R _L = 6.49 Ω I _D ≅ - 7.7 A, V _{GEN} = - 10 V, R _g = 1.0 Ω		-	11	17	ns
Rise Time ^c	t _r			-	11	17	
Turn-Off Delay Time ^c	t _{d(off)}			-	78	117	
Fall Time ^c	t _f			-	15	23	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed Current ^a	I _{SM}			-	-	- 150	A
Forward Voltage	V _{SD}	I _F = - 7.7 A, V _{GS} = 0 V		-	- 0.8	- 1.5	V

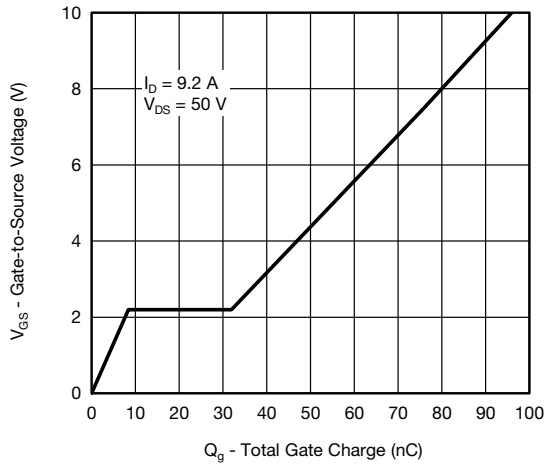
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.
 c. Independent of operating temperature.

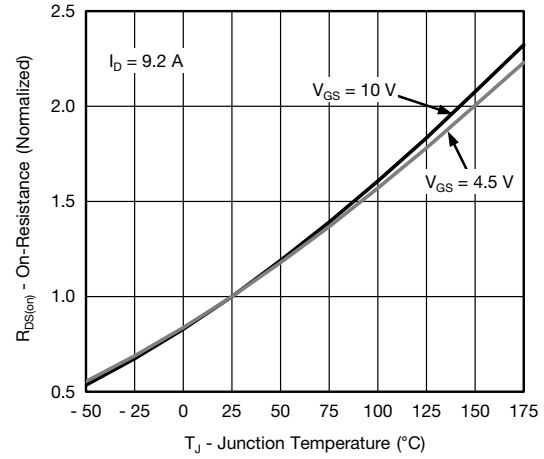
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Output Characteristics

Transfer Characteristics

Transfer Characteristics

Transconductance

On-Resistance vs. Drain Current

Capacitance

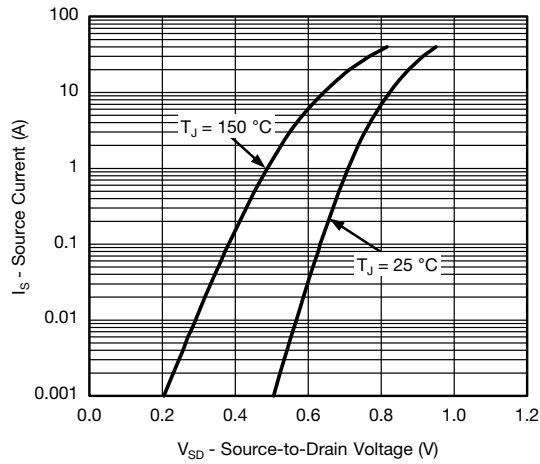
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



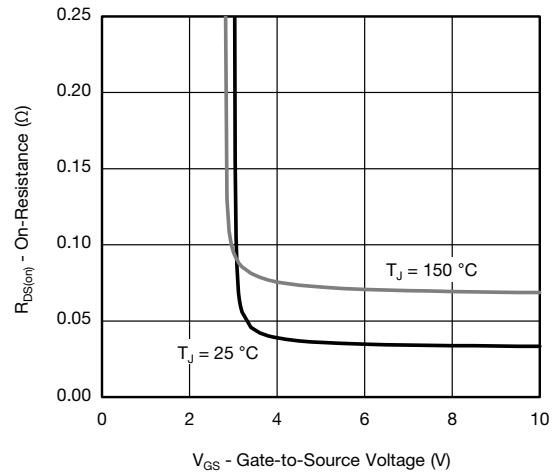
Gate Charge



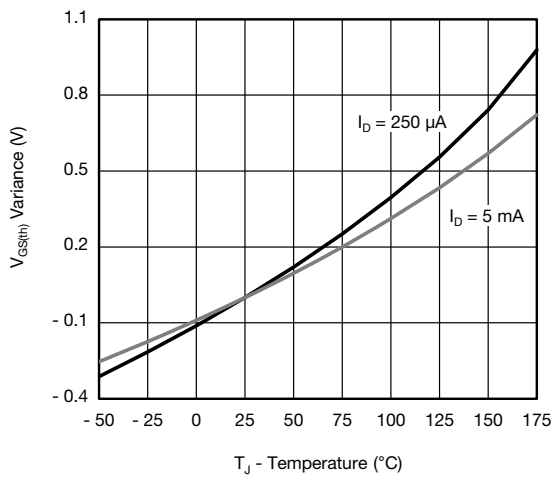
On-Resistance vs. Junction Temperature



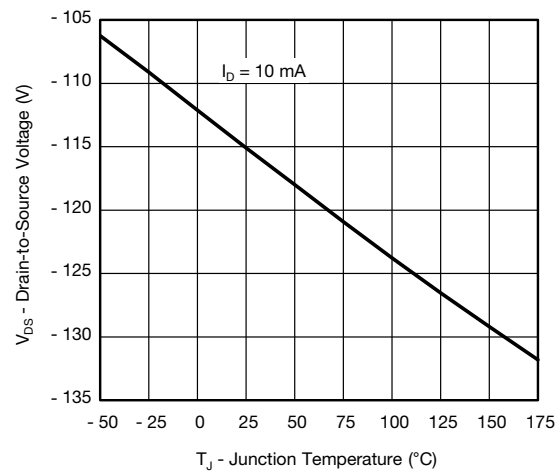
Source Drain Diode Forward Voltage



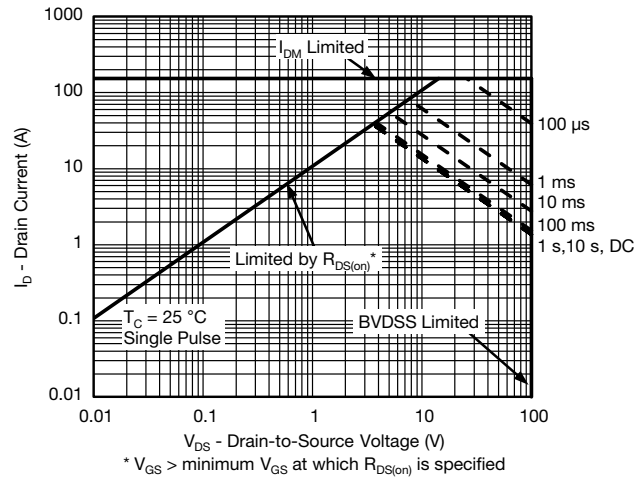
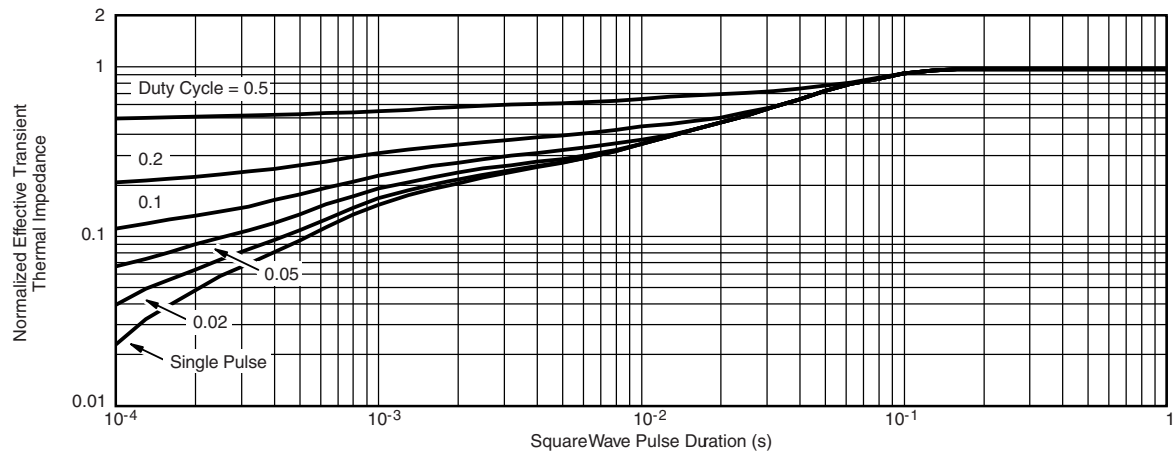
On-Resistance vs. Gate-to-Source Voltage

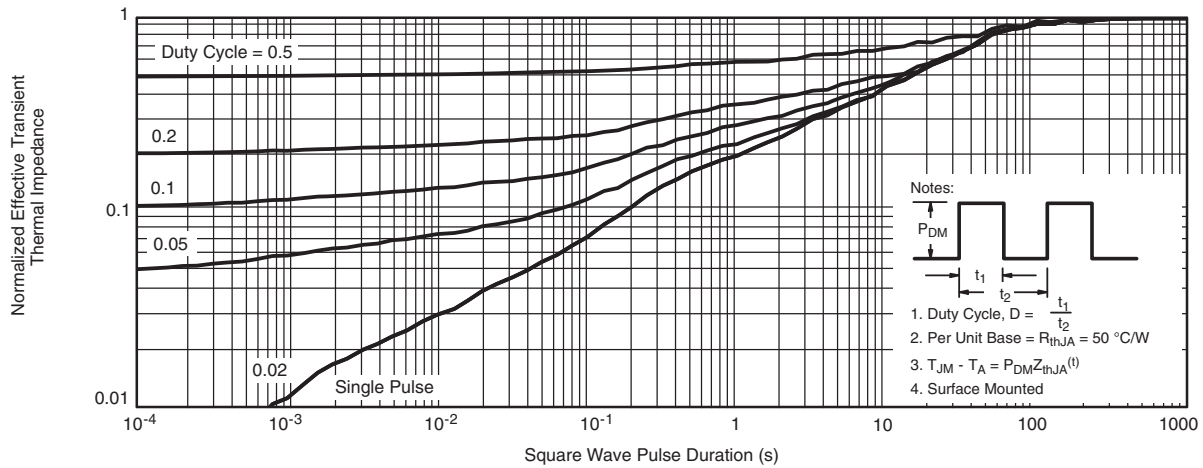


Threshold Voltage



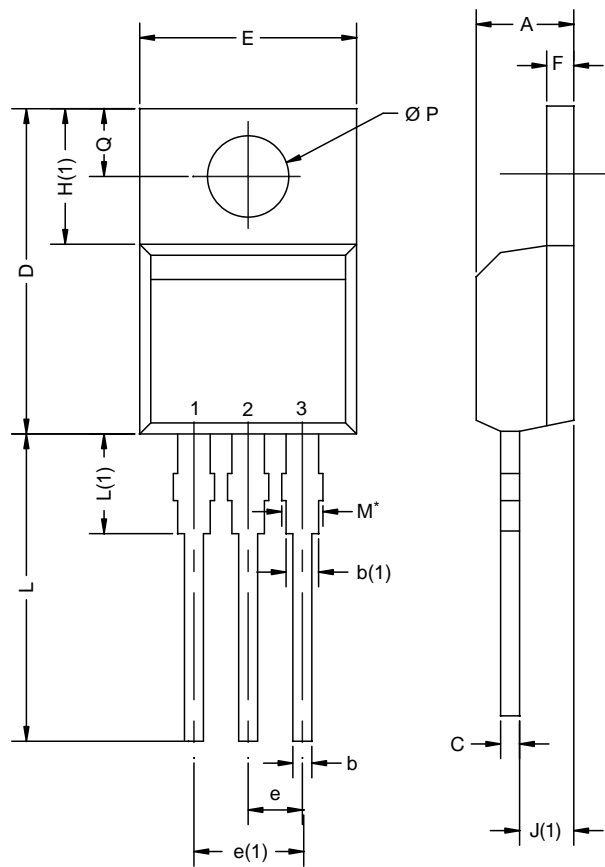
Drain Source Breakdown vs. Junction Temperature

THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Safe Operating Area

Normalized Thermal Transient Impedance, Junction-to-Case

THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient
Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction to Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction to Case ($25\text{ }^{\circ}\text{C}$)
- are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

TO-220AB



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
$\varnothing P$	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118
ECN: X12-0208-Rev. N, 08-Oct-12				
DWG: 5471				

Notes

* M = 1.32 mm to 1.62 mm (dimension including protrusion)
Heatsink hole for HVM

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