

UF9640G-TA3-T-VB Datasheet

P-Channel 200V (D-S)MOSFET

PRODUCT SUMMARY

V_{DS} (V)	-200	
$R_{DS(on)}$ (Ω)	$V_{GS} = -10\text{ V}$	0.50
Q_g max. (nC)	44	
Q_{gs} (nC)	7.1	
Q_{gd} (nC)	27	
Configuration	Single	

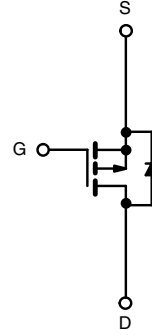
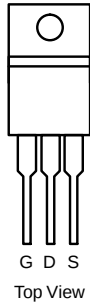
FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- P-channel
- Fast switching
- Ease of paralleling
- Simple drive requirements



Available
RoHS*
 Available

TO-220AB



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	-200	V
Gate-Source Voltage			V_{GS}	± 20	V
Continuous Drain Current	V_{GS} at -10 V	$T_C = 25\text{ }^{\circ}\text{C}$	I_D	-11	A
		$T_C = 100\text{ }^{\circ}\text{C}$		-6.8	
Pulsed Drain Current ^a			I_{DM}	-44	
Linear Derating Factor				1.0	W/ $^{\circ}\text{C}$
Single Pulse Avalanche Energy ^b			E_{AS}	700	mJ
Repetitive Avalanche Current ^a			I_{AR}	-11	A
Repetitive Avalanche Energy ^a			E_{AR}	13	mJ
Maximum Power Dissipation	$T_C = 25\text{ }^{\circ}\text{C}$		P_D	125	W
Peak Diode Recovery dV/dt ^c			dV/dt	-5.0	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	-55 to +150	$^{\circ}\text{C}$
Soldering Recommendations (Peak temperature) ^d	for 10 s			300	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

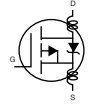
Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
 b. $V_{DD} = -50\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 8.7\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = -11\text{ A}$ (see fig. 12).
 c. $I_{SD} \leq -11\text{ A}$, $dI/dt \leq 150\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
 d. 1.6 mm from case.

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.0	

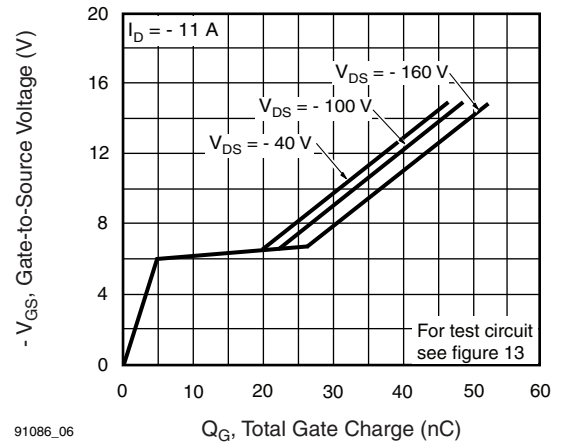
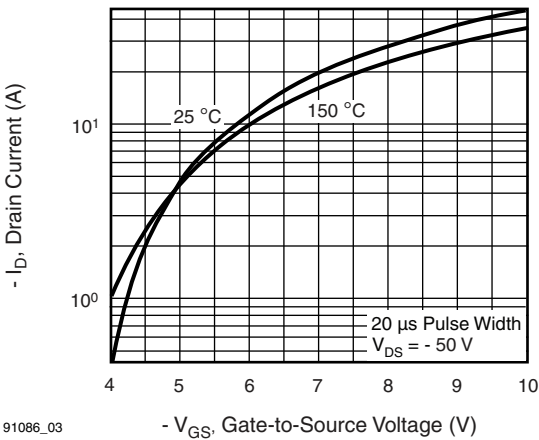
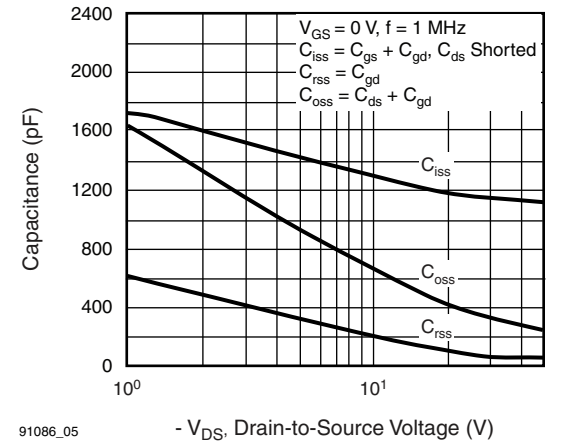
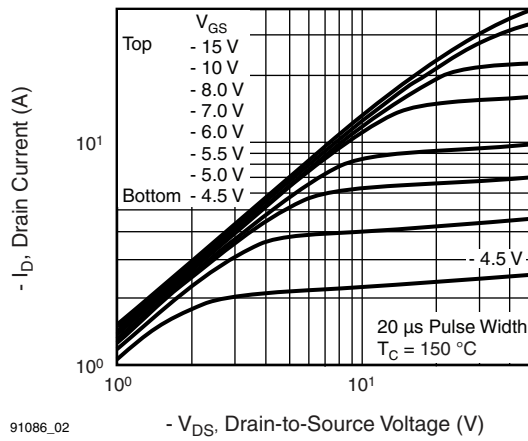
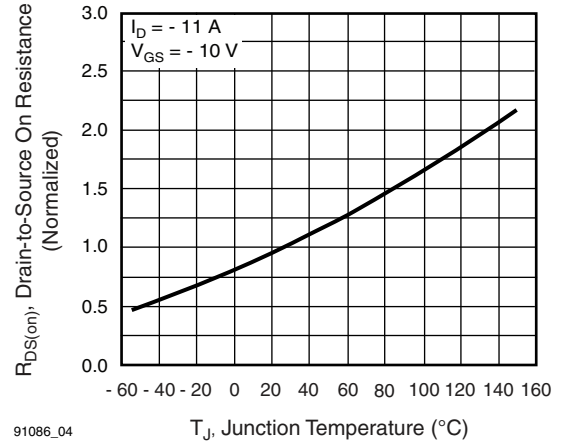
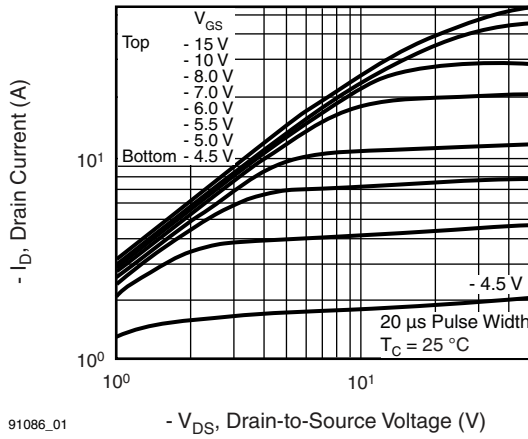
SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = -250\text{ }\mu\text{A}$	-200	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^{\circ}\text{C}$, $I_D = -1\text{ mA}$	-	-0.2	-	V/ $^{\circ}\text{C}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\text{ }\mu\text{A}$	-2.0	-	-4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -200\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	-100	μA
		$V_{DS} = -160\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}$	-	-	-500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$, $I_D = -6.6\text{ A}^b$	-	0.50	-	Ω
Forward Transconductance	g_{fs}	$V_{DS} = -50\text{ V}$, $I_D = -6.6\text{ A}^b$	4.1	-	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = -25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5	-	1200	-	pF
Output Capacitance	C_{oss}		-	370	-	
Reverse Transfer Capacitance	C_{rss}		-	81	-	
Total Gate Charge	Q_g	$V_{GS} = -10\text{ V}$, $I_D = -11\text{ A}$, $V_{DS} = -160\text{ V}$, see fig. 6 and 13 ^b	-	-	44	nC
Gate-Source Charge	Q_{gs}		-	-	7.1	
Gate-Drain Charge	Q_{gd}		-	-	27	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -100\text{ V}$, $I_D = -11\text{ A}$ $R_g = 9.1\text{ }\Omega$, $R_D = 8.6\text{ }\Omega$, see fig. 10 ^b	-	14	-	ns
Rise Time	t_r		-	43	-	
Turn-Off Delay Time	$t_{d(off)}$		-	39	-	
Fall Time	t_f		-	38	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal Source Inductance	L_S		-	7.5	-	
Gate Input Resistance	R_g	$f = 1\text{ MHz}$, open drain	0.3	-	1.7	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p-n junction diode 	-	-	-11	A
Pulsed Diode Forward Current ^a	I_{SM}		-	-	-44	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_S = -11\text{ A}$, $V_{GS} = 0\text{ V}^b$	-	-	-5	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_F = -11\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}^b$	-	250	300	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	2.9	3.6	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
 b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



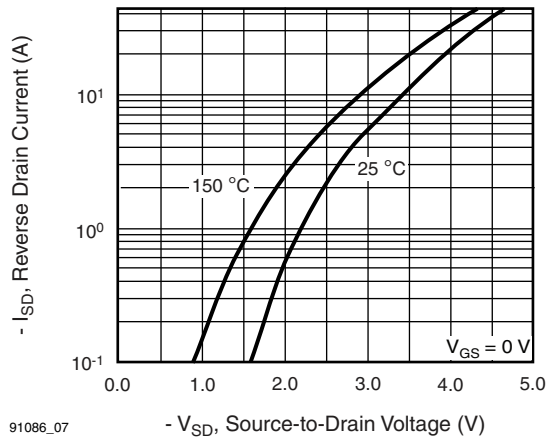


Fig. 7 - Typical Source-Drain Diode Forward Voltage

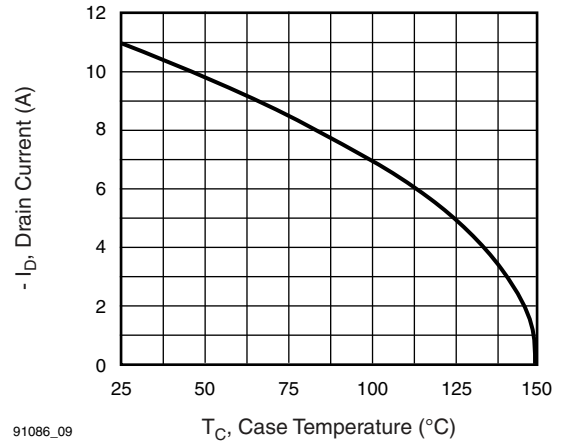


Fig. 9 - Maximum Drain Current vs. Case Temperature

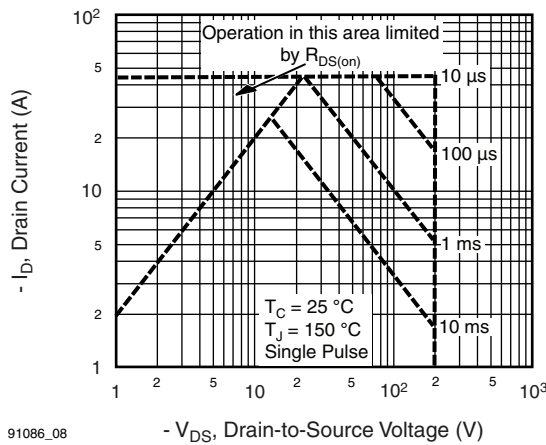


Fig. 8 - Maximum Safe Operating Area

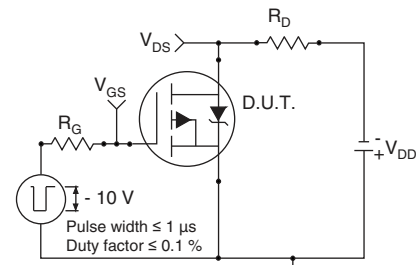


Fig. 10a - Switching Time Test Circuit

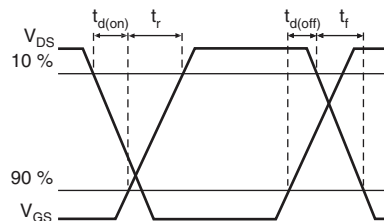


Fig. 10b - Switching Time Waveforms

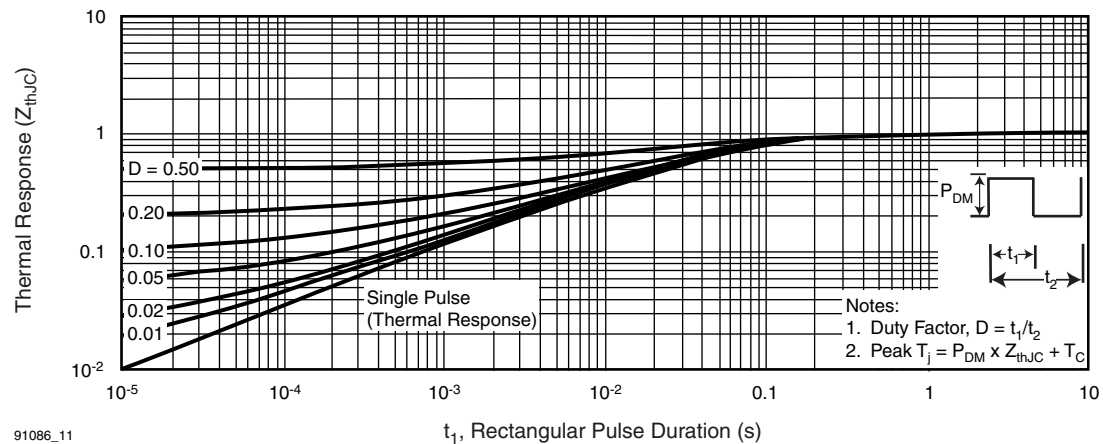


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

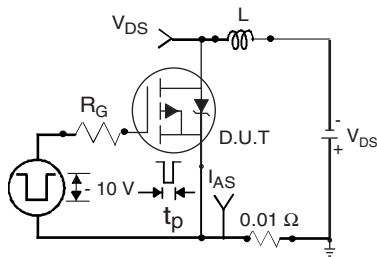


Fig. 12a - Unclamped Inductive Test Circuit

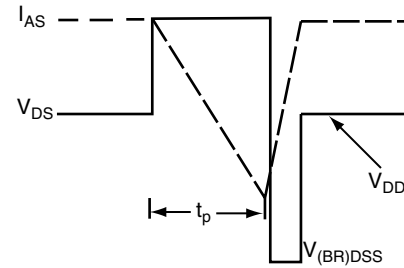


Fig. 12b - Unclamped Inductive Waveforms

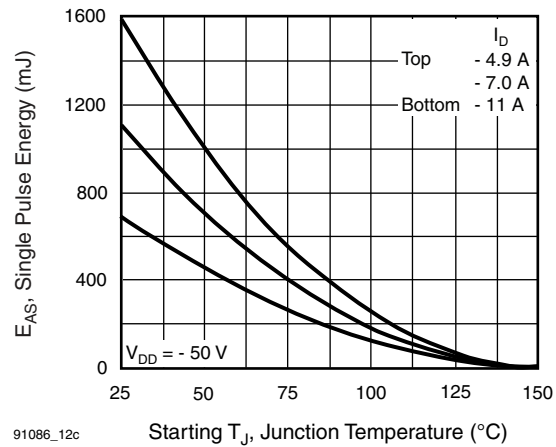


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

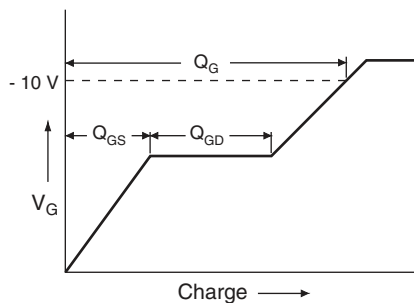


Fig. 13a - Basic Gate Charge Waveform

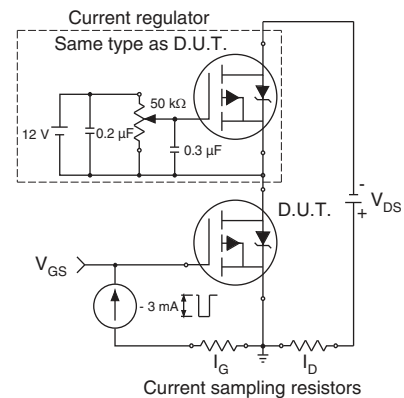


Fig. 13b - Gate Charge Test Circuit

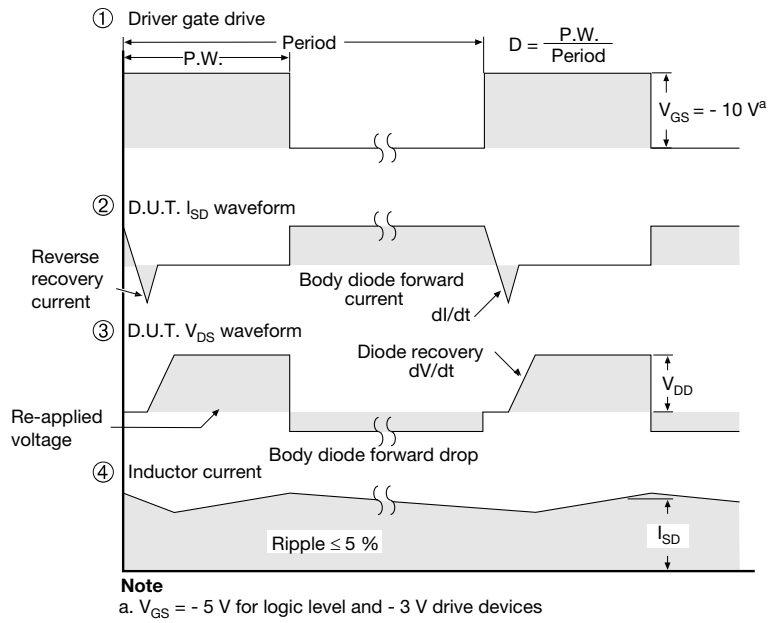
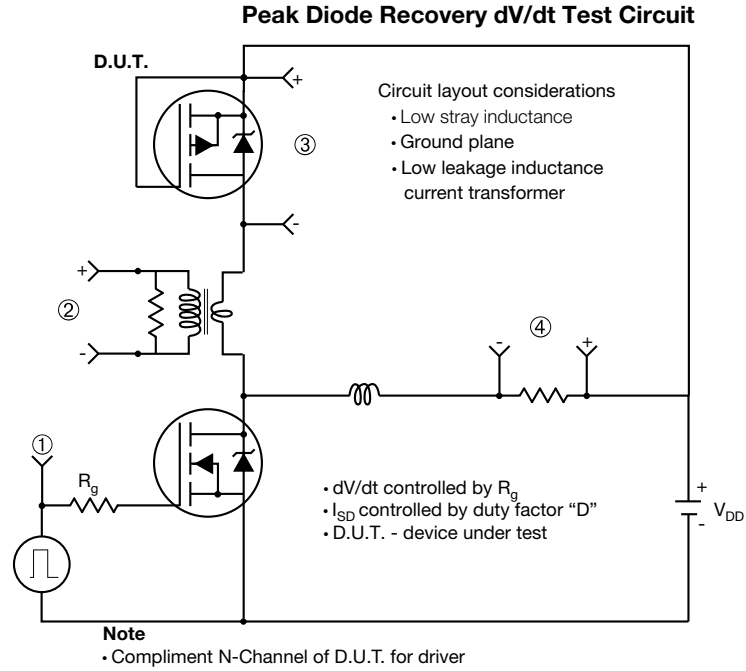
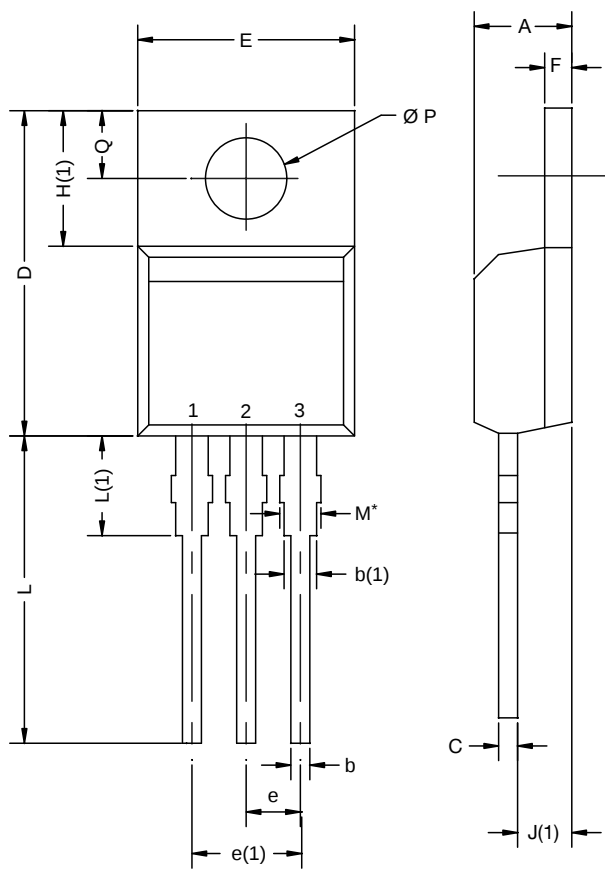


Fig. 14 - For P-Channel

TO-220AB



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
Ø P	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118
ECN: X12-0208-Rev. N, 08-Oct-12				
DWG: 5471				

Notes
* M = 1.32 mm to 1.62 mm (dimension including protrusion)
Heatsink hole for HVM

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