

# STP36NF06-VB Datasheet

## N-Channel 60 V (D-S) MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>a</sup>
60	0.024 at $V_{GS} = 10$ V	50
	0.028 at $V_{GS} = 4.5$ V	40

### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Surface Mount
- Available in Tape and Reel
- Dynamic dV/dt Rating
- Logic-Level Gate Drive
- Fast Switching
- Compliant to RoHS Directive 2002/95/EC



**RoHS\***  
COMPLIANT

TO-220AB



Top View



N-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ , unless otherwise noted)

PARAMETER				SYMBOL	LIMIT	UNIT
Drain-Source Voltage				$V_{DS}$	60	V
Gate-Source Voltage				$V_{GS}$	$\pm 20$	
Continuous Drain Current <sup>f</sup>	$V_{GS}$ at 10 V	$T_C = 25\text{ }^{\circ}\text{C}$	$I_D$	50	A	
Continuous Drain Current		$T_C = 100\text{ }^{\circ}\text{C}$		36		
Pulsed Drain Current <sup>a</sup>				$I_{DM}$	200	
Linear Derating Factor					1.0	W/ $^{\circ}\text{C}$
Linear Derating Factor (PCB Mount) <sup>e</sup>					0.025	
Single Pulse Avalanche Energy <sup>b</sup>				$E_{AS}$	400	mJ
Maximum Power Dissipation	$T_C = 25\text{ }^{\circ}\text{C}$			$P_D$	150	W
Maximum Power Dissipation (PCB Mount) <sup>e</sup>	$T_A = 25\text{ }^{\circ}\text{C}$				3.7	
Peak Diode Recovery $dV/dt^c$				$dV/dt$	4.5	V/ns
Operating Junction and Storage Temperature Range				$T_J, T_{stg}$	- 55 to + 175	$^{\circ}\text{C}$
Soldering Recommendations (Peak Temperature) <sup>d</sup>	for 10 s				300 <sup>d</sup>	

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25$  V, starting  $T_J = 25^\circ\text{C}$ ,  $L = 179$   $\mu\text{H}$ ,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 51$  A (see fig. 12).
- $I_{SD} \leq 51$  A,  $di/dt \leq 250$  A/ $\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 175^\circ\text{C}$ .
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).
- Current limited by the package, (die current = 51 A).

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Maximum Junction-to-Ambient (PCB Mount) <sup>a</sup>	$R_{thJA}$	-	40	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.0	

**Note**

a. When mounted on 1" square PCB (FR-4 or G-10 material).

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**SPECIFICATIONS** ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0, I <sub>D</sub> = 250 μA		60	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.070	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		1.0	-	2.5	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 10 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V		-	-	25	μA
		V <sub>DS</sub> = 48 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 150 °C		-	-	250	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 21 A <sup>b</sup>	-	0.024	-	Ω
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 15 A <sup>b</sup>	-	0.028	-	
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 25 V, I <sub>D</sub> = 21A <sup>b</sup>		23	-	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz, see fig. 5		-	190		pF
Output Capacitance	C <sub>oss</sub>			-	920	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	170	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 5.0 V	I <sub>D</sub> = 51 A, V <sub>DS</sub> = 48 V, see fig. 6 and 13 <sup>b</sup>	-	-	66	nC
Gate-Source Charge	Q <sub>gs</sub>			-	-	12	
Gate-Drain Charge	Q <sub>gd</sub>			-	-	43	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 51 A, R <sub>g</sub> = 4.6 Ω, R <sub>D</sub> = 0.56 Ω, see fig. 10 <sup>b</sup>		-	17	-	ns
Rise Time	t <sub>r</sub>			-	230	-	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	2	-	
Fall Time	t <sub>f</sub>			-	110	-	
Internal Drain Inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	L <sub>S</sub>			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		-	-	50°	A
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	200	
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 51 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	2.5	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 51 A, dI/dt = 100 A/μs <sup>b</sup>		-	130	180	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			-	0.84	1.3	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
 b. Pulse width  $\leq 300\ \mu\text{s}$ ; duty cycle  $\leq 2\%$ .  
 c. Current limited by the package, (Die Current = 51 A).

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics,  $T_C = 25^\circ\text{C}$** 

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 2 - Typical Output Characteristics,  $T_C = 150^\circ\text{C}$** 

**Fig. 4 - Normalized On-Resistance vs. Temperature**



Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



Fig. 7 - Typical Source-Drain Diode Forward Voltage



Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



Fig. 8 - Maximum Safe Operating Area



Fig. 9 - Maximum Drain Current vs. Case Temperature



Fig. 10a - Switching Time Test Circuit

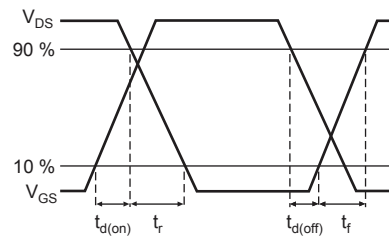


Fig. 10b - Switching Time Waveforms



Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



Fig. 12a - Unclamped Inductive Test Circuit



Fig. 12b - Unclamped Inductive Waveforms



Fig. 12c - Maximum Avalanche Energy vs. Drain Current

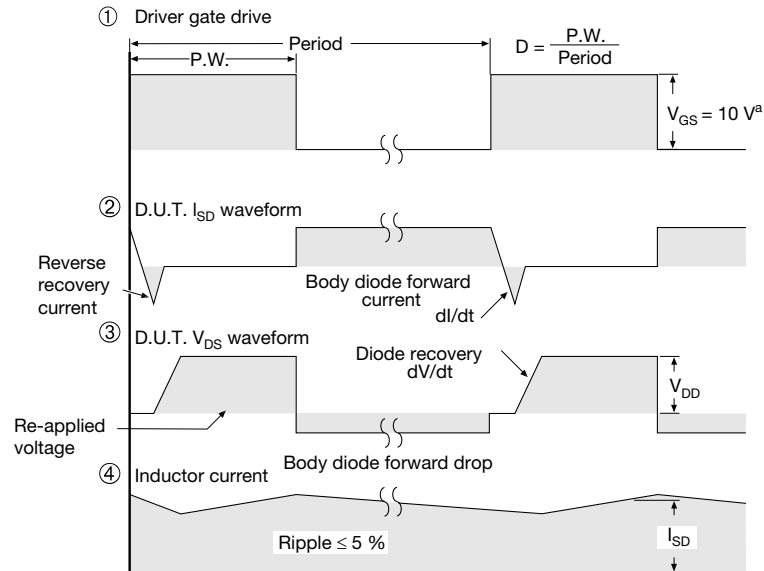
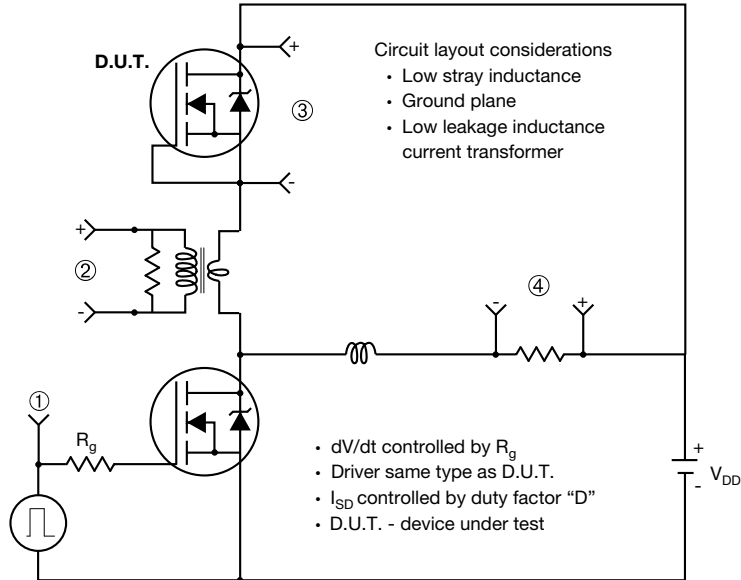


Fig. 13a - Basic Gate Charge Waveform



Fig. 13b - Gate Charge Test Circuit

### Peak Diode Recovery $dV/dt$ Test Circuit

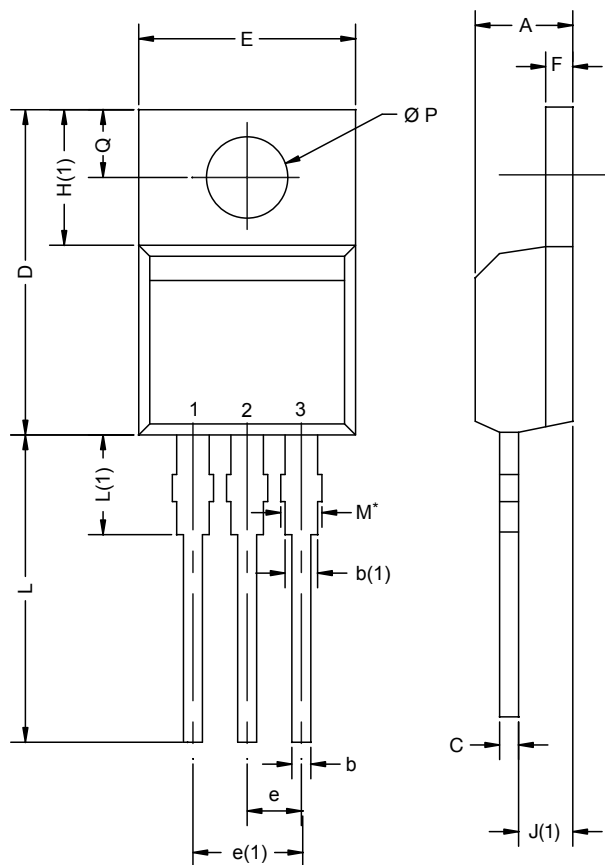


#### Note

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

# TO-220AB



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
$\varnothing P$	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118
ECN: X12-0208-Rev. N, 08-Oct-12 DWG: 5471				

**Notes**

\* M = 1.32 mm to 1.62 mm (dimension including protrusion)  
Heatsink hole for HVM



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