

PHP3N20E-VB Datasheet

N-Channel 200 V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	200				
R _{DS(on)} (Ω)	V _{GS} = 10 V 0. 91				
Q _g (Max.) (nC)	13				
Q _{gs} (nC)	3.0				
Q _{gd} (nC)	7.9				
Configuration	Single				

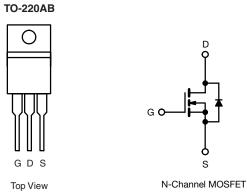
FEATURES

- Trench Power MOSFET ٠
- 175 °C Junction Temperature
- PWM Optimized •
- 100 % R_a Tested
- Compliant to RoHS Directive 2002/95/EC

APPLICATIONS

• Primary Side Switch





ABSOLUTE MAXIMUM RATINGS (T C	= 25 °C, unl	ess otherwis	se noted)			
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			V _{DS}	200	v	
Gate-Source Voltage			V _{GS}	± 20	v	
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C T _C = 100 °C	1	5.0		
		T _C = 100 °C	I _D	4.0	А	
Pulsed Drain Current ^a			I _{DM}	20		
Linear Derating Factor			0.33 0.020	0.33	W/°C	
Linear Derating Factor (PCB Mount) ^e				0.020		
Single Pulse Avalanche Energy ^b			E _{AS}	161	mJ	
Repetitive Avalanche Current ^a			I _{AR}	4.8	А	
Repetitive Avalanche Energy ^a			E _{AR}	4.2	mJ	
Maximum Power Dissipation	T _C = 25 °C		р	42	w	
Maximum Power Dissipation (PCB mount) ^e	T _A = 25 °C		P _D 2.5		v	
Peak Diode Recovery dV/dt ^c			dV/dt	5.0	V/ns	
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +150		
Soldering Recommendations (Peak temperature) ^d	for 10 s			260		

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11). b. $V_{DD} = 50 \text{ V}$, starting $T_J = 25 \text{ °C}$, L = 14 mH, $R_g = 25 \Omega$, $I_{AS} = 4.8 \text{ A}$ (see fig. 12). c. $I_{SD} \leq 5.2 \text{ A}$, dI/dt $\leq 95 \text{ A/}\mu$ s, $V_{DD} \leq V_{DS}$, $T_J \leq 150 \text{ °C}$.

d. 1.6 mm from case.

e. When mounted on 1" square PCB (FR-4 or G-10 material).



THERMAL RESISTANCE RAT	RMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R _{thJA}	-	-	110	
Maximum Junction-to-Ambient (PCB mount) ^a	R _{thJA}	-	-	50	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	-	-	3.0	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT	
Static		-					I
Drain-Source Breakdown Voltage	V _{DS}	V _{GS}	= 0 V, I _D = 250 μΑ	200	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference	ce to 25 °C, I _D = 1 mA	-	0.29	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} =	= V _{GS} , I _D = 250 μΑ	2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}		V _{GS} = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}		= 200 V, V _{GS} = 0 V /, V _{GS} = 0 V, T _J = 125 °C	-	-	25 250	μA
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 2.9 A ^b	-	0.91	-	Ω
Forward Transconductance	9 _{fs}	V _{DS} =	= 50 V, I _D = 2.9 A ^b	1.7	-	-	S
Dynamic		-					1
Input Capacitance	C _{iss}	$V_{GS} = 0 V,$		-	185	-	
Output Capacitance	C _{oss}		$V_{DS} = 25 V,$	-	100	-	pF
Reverse Transfer Capacitance	C _{rss}	f = 1.0 MHz, see fig. 5		-	30	-	
Total Gate Charge	Qg			-	-	13.0	
Gate-Source Charge	Q _{gs}	$V_{GS} = 10 V$	I _D = 4.8 A, V _{DS} = 160 V, see fig. 6 and 13 ^b	-	-	3.0	nC
Gate-Drain Charge	Q _{gd}		see lig. o and to	see fig. 6 and 13 b		1	
Turn-On Delay Time	t _{d(on)}			-	7.2	-	
Rise Time	t _r	V_{DD} = 100 V, I_D = 4.8 A, R_G = 18 $\Omega,~R_D$ = 20 $\Omega,$ see fig. 10 $^{\rm b}$		-	22	-	- ns
Turn-Off Delay Time	t _{d(off)}			-	19	-	
Fall Time	t _f			-	13	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from		-	4.5	-	nH
Internal Source Inductance	L _S	package and die contact	center of	D			
Drain-Source Body Diode Characteristic	s	•					•
Continuous Source-Drain Diode Current	I _S	showing the	MOSFET symbol showing the		-	4.8	^
Pulsed Diode Forward Current ^a	I _{SM}	integral revers p - n junction		-	-	19	A
Body Diode Voltage	V _{SD}	T _J = 25 °C	, $I_{S} = 4.8$ A, $V_{GS} = 0$ V ^b	-	-	1.8	V
Body Diode Reverse Recovery Time	t _{rr}	- T _J = 25 °C, I _F = 4.8 A, dl/dt = 100 A/μs ^b		-	150	300	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	0.91	1.8	μC
Forward Turn-On Time	t _{on}	Intrinsic tu	ırn-on time is negligible (turn	-on is dor	ninated b	y L _S and	L _D)

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11). b. Pulse width \leq 300 μ s; duty cycle \leq 2 %.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

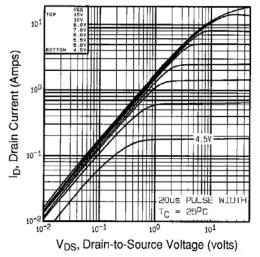


Fig. 1 - Typical Output Characteristics, $T_C = 25 \ ^{\circ}C$

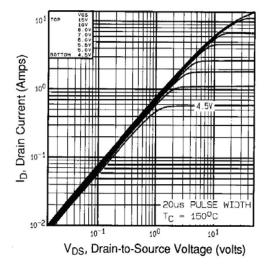


Fig. 2 - Typical Output Characteristics, T_C = 150 °C

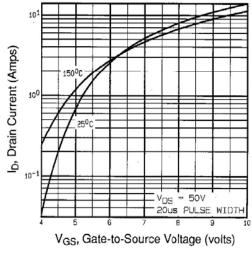


Fig. 3 - Typical Transfer Characteristics

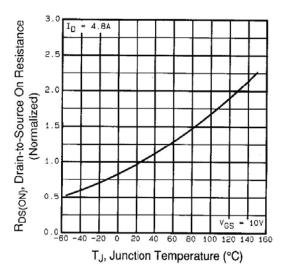


Fig. 4 - Normalized On-Resistance vs. Temperature



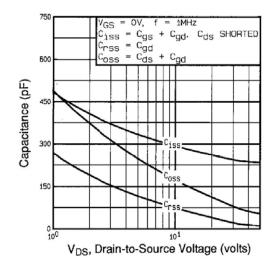


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

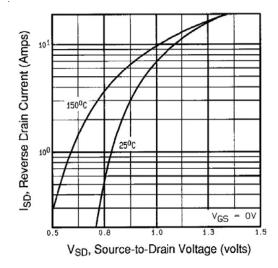


Fig. 7 - Typical Source-Drain Diode Forward Voltage

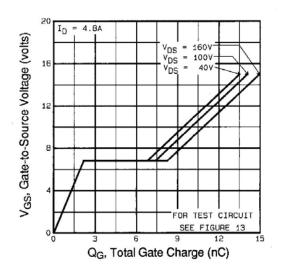


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

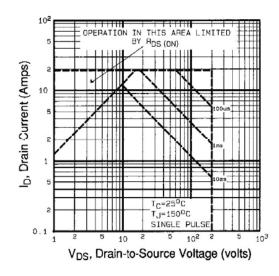


Fig. 8 - Maximum Safe Operating Area



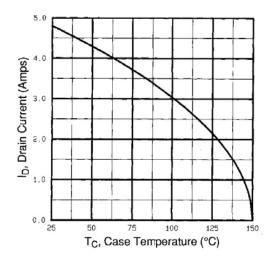


Fig. 9 - Maximum Drain Current vs. Case Temperature

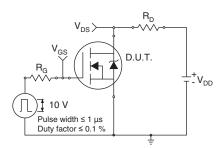


Fig. 10a - Switching Time Test Circuit

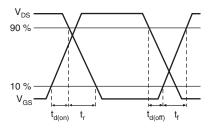


Fig. 10b - Switching Time Waveforms

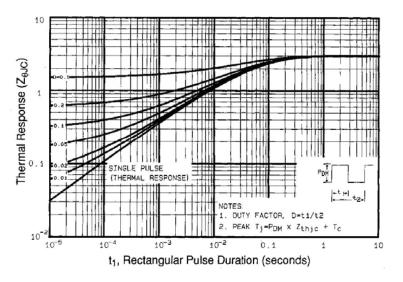


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



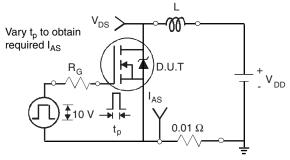


Fig. 12a - Unclamped Inductive Test Circuit

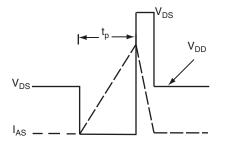


Fig. 12b - Unclamped Inductive Waveforms

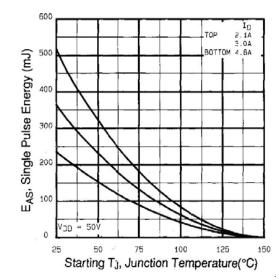


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

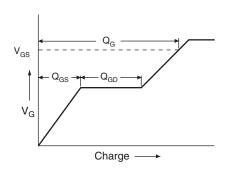


Fig. 13a - Basic Gate Charge Waveform

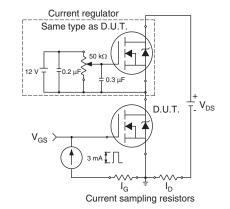
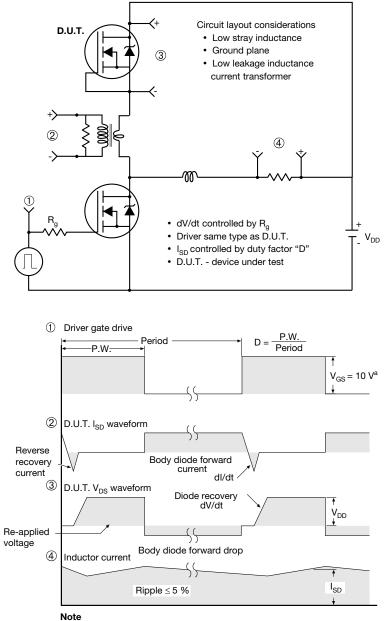


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit

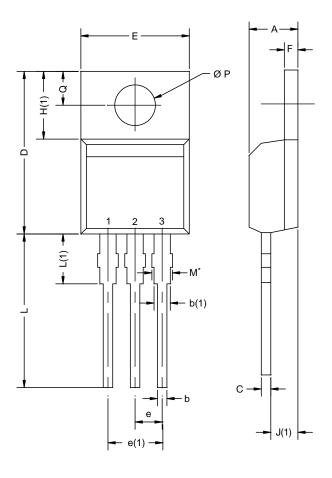


a. $V_{GS} = 5$ V for logic level devices

Fig. 14 - For N-Channel



TO-220AB



	MILLIN	IETERS	INC	HES
DIM.	MIN.	MAX.	MIN.	MAX.
А	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
С	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
Е	10.04	10.51	0.395	0.414
е	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
ØР	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118
ECN: X12- DWG: 547	0208-Rev. N, 1	08-Oct-12		

Notes

 * M = 1.32 mm to 1.62 mm (dimension including protrusion) Heatsink hole for HVM



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