

# FQP5N20L-VB Datasheet

## N-Channel 200 V (D-S) MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	200	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	0.91
$Q_g$ (Max.) (nC)	13	
$Q_{gs}$ (nC)	3.0	
$Q_{gd}$ (nC)	7.9	
Configuration	Single	

### FEATURES

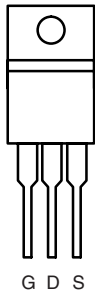
- Trench Power MOSFET
- 175 °C Junction Temperature
- PWM Optimized
- 100 %  $R_g$  Tested
- Compliant to RoHS Directive 2002/95/EC


**RoHS**  
 COMPLIANT

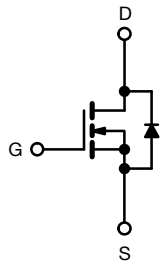
### APPLICATIONS

- Primary Side Switch

TO-220AB



Top View



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V <sub>DS</sub>	200	V
Gate-Source Voltage			V <sub>GS</sub>	± 20	
Continuous Drain Current	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	I <sub>D</sub>	5.0	A
		T <sub>C</sub> = 100 °C		4.0	
Pulsed Drain Current <sup>a</sup>			I <sub>DM</sub>	20	W/°C
Linear Derating Factor				0.33	
Linear Derating Factor (PCB Mount) <sup>e</sup>				0.020	
Single Pulse Avalanche Energy <sup>b</sup>			E <sub>AS</sub>	161	mJ
Repetitive Avalanche Current <sup>a</sup>			I <sub>AR</sub>	4.8	A
Repetitive Avalanche Energy <sup>a</sup>			E <sub>AR</sub>	4.2	mJ
Maximum Power Dissipation	T <sub>C</sub> = 25 °C		P <sub>D</sub>	42	W
Maximum Power Dissipation (PCB mount) <sup>e</sup>	T <sub>A</sub> = 25 °C			2.5	
Peak Diode Recovery dV/dt <sup>c</sup>			dV/dt	5.0	V/ns
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Soldering Recommendations (Peak temperature) <sup>d</sup>	for 10 s			260	

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 14\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 4.8\text{ A}$  (see fig. 12).
- $I_{SD} \leq 5.2\text{ A}$ ,  $dI/dt \leq 95\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	-	110	°C/W
Maximum Junction-to-Ambient (PCB mount) <sup>a</sup>	$R_{thJA}$	-	-	50	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	-	3.0	

**Note**

a. When mounted on 1" square PCB (FR-4 or G-10 material).

**SPECIFICATIONS** ( $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$		200	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^{\circ}\text{C}$ , $I_D = 1\text{ mA}$		-	0.29	-	V/ $^{\circ}\text{C}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 200\text{ V}$ , $V_{GS} = 0\text{ V}$		-	-	25	$\mu\text{A}$
		$V_{DS} = 160\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 125\text{ }^{\circ}\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 2.9\text{ A}^b$	-	0.91	-	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}$ , $I_D = 2.9\text{ A}^b$		1.7	-	-	S
Dynamic							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 25\text{ V}$ , $f = 1.0\text{ MHz}$ , see fig. 5		-	185	-	pF
Output Capacitance	$C_{oss}$			-	100	-	
Reverse Transfer Capacitance	$C_{rss}$			-	30	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 4.8\text{ A}$ , $V_{DS} = 160\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	13.0	nC
Gate-Source Charge	$Q_{gs}$			-	-	3.0	
Gate-Drain Charge	$Q_{gd}$			-	-	7.9	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 100\text{ V}$ , $I_D = 4.8\text{ A}$ , $R_G = 18\text{ }\Omega$ , $R_D = 20\text{ }\Omega$ , see fig. 10 <sup>b</sup>		-	7.2	-	ns
Rise Time	$t_r$			-	22	-	
Turn-Off Delay Time	$t_{d(off)}$			-	19	-	
Fall Time	$t_f$			-	13	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	$L_S$			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	4.8	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	19	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^{\circ}\text{C}$ , $I_S = 4.8\text{ A}$ , $V_{GS} = 0\text{ V}^b$		-	-	1.8	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^{\circ}\text{C}$ , $I_F = 4.8\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}^b$		-	150	300	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	0.91	1.8	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
 b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

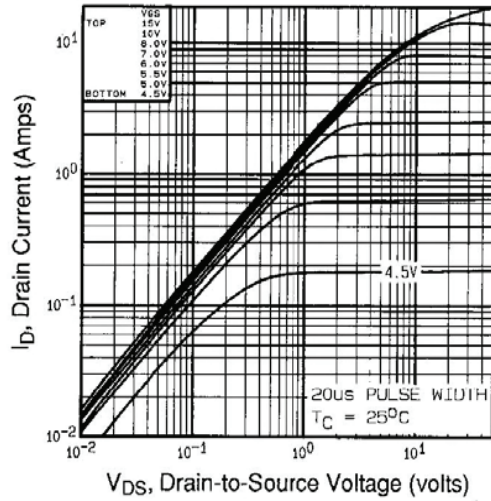


Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^{\circ}\text{C}$

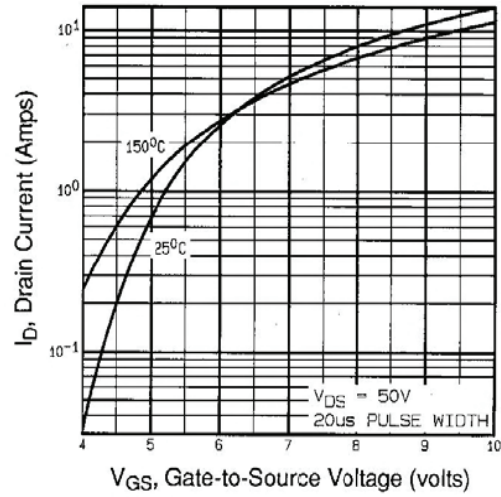


Fig. 3 - Typical Transfer Characteristics

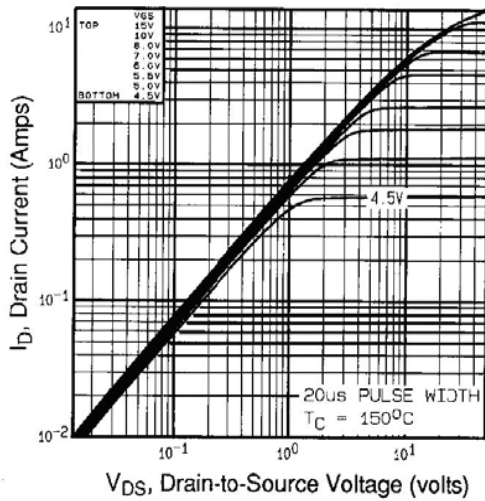


Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^{\circ}\text{C}$

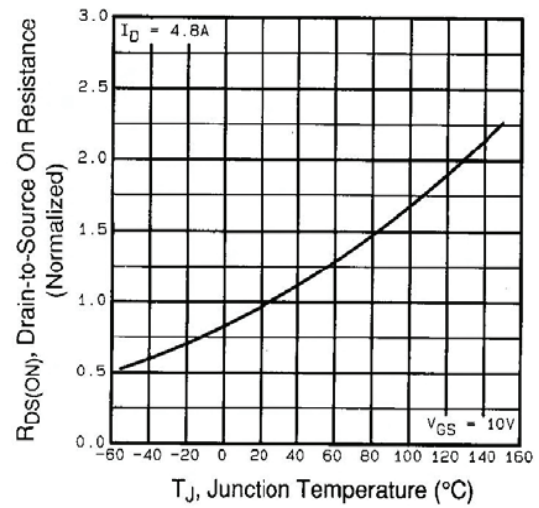


Fig. 4 - Normalized On-Resistance vs. Temperature

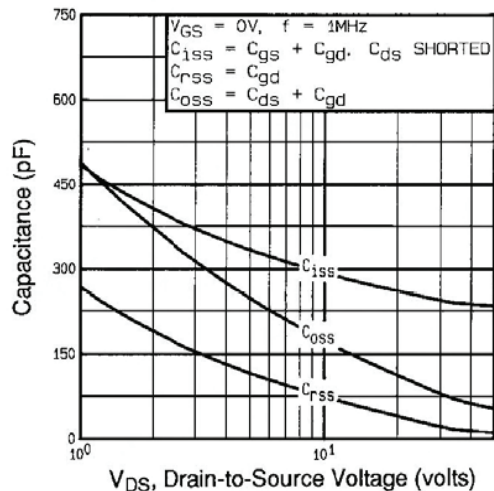


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

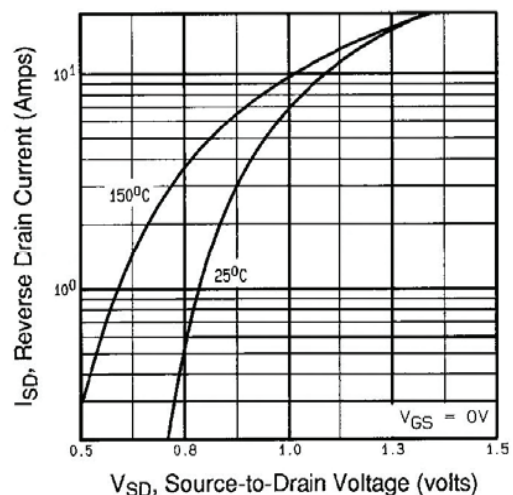


Fig. 7 - Typical Source-Drain Diode Forward Voltage

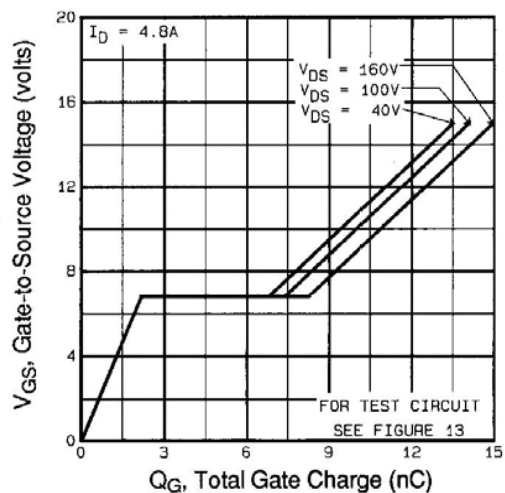


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

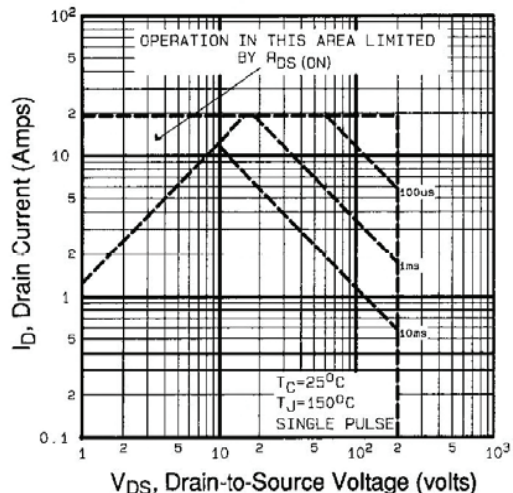


Fig. 8 - Maximum Safe Operating Area

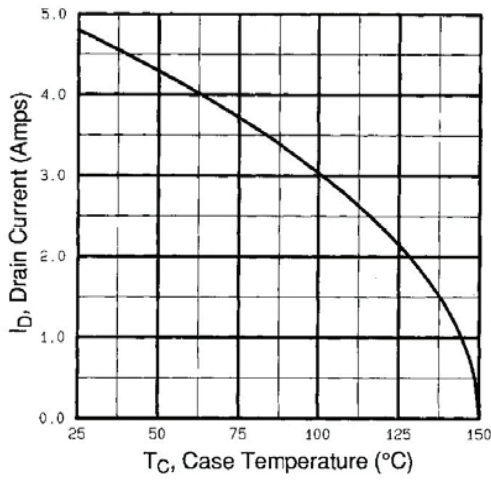


Fig. 9 - Maximum Drain Current vs. Case Temperature

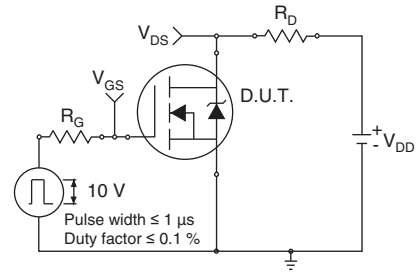


Fig. 10a - Switching Time Test Circuit

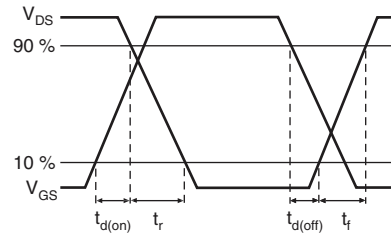


Fig. 10b - Switching Time Waveforms

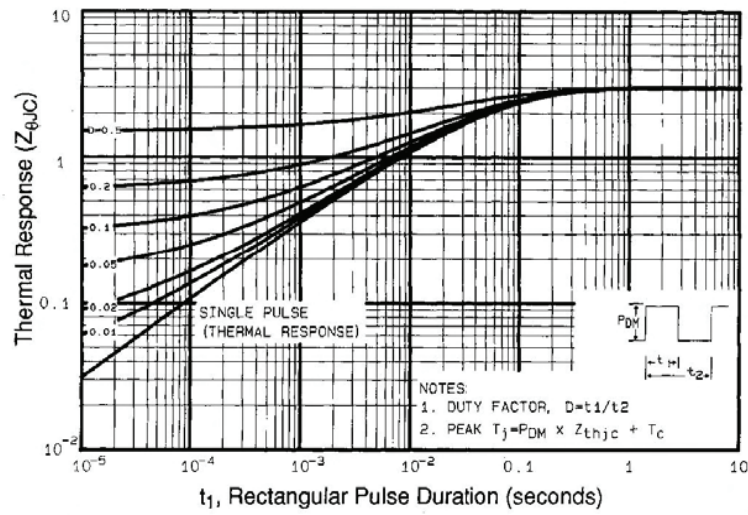


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

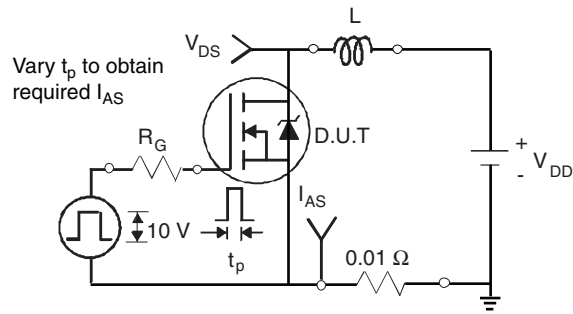


Fig. 12a - Unclamped Inductive Test Circuit

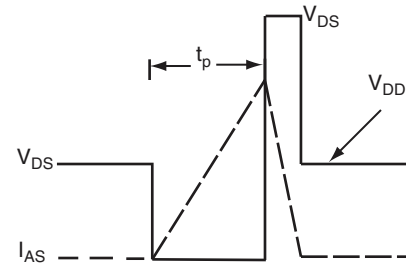


Fig. 12b - Unclamped Inductive Waveforms

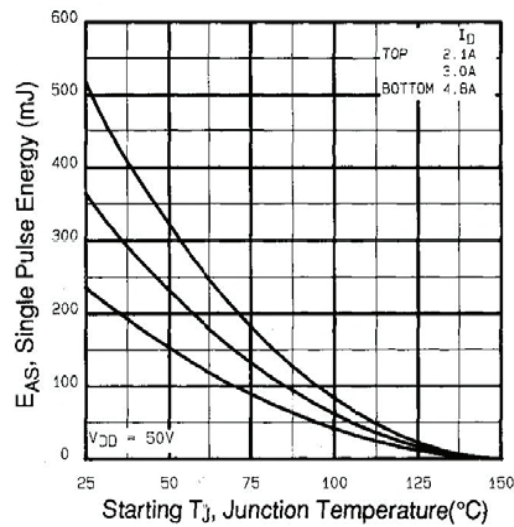


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

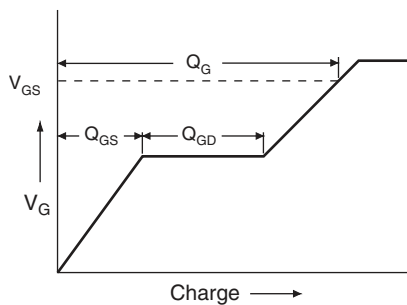


Fig. 13a - Basic Gate Charge Waveform

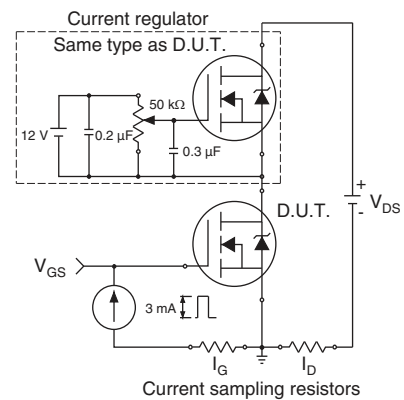
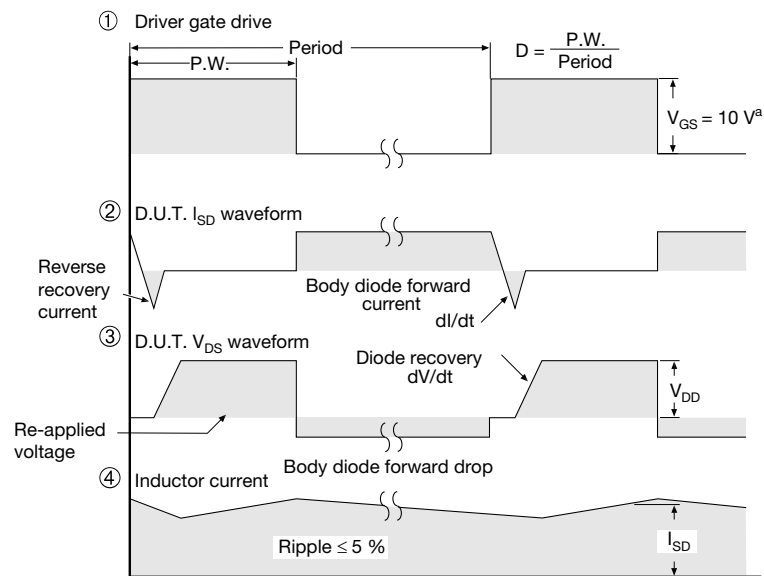
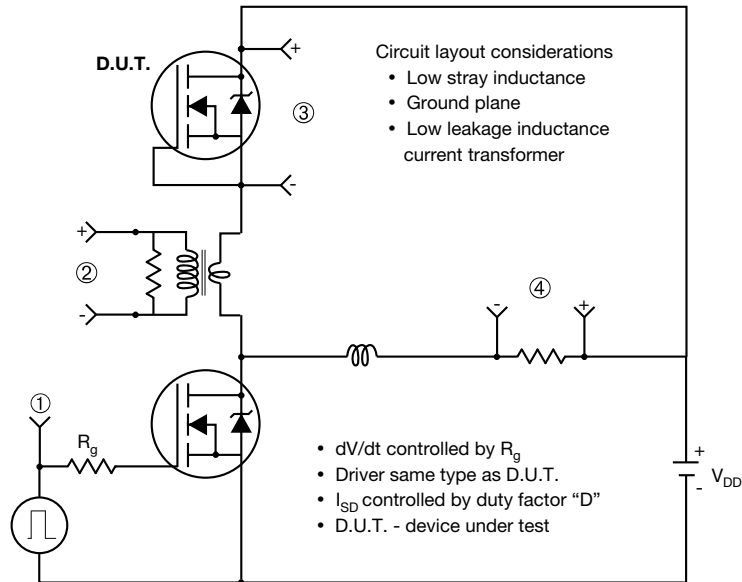


Fig. 13b - Gate Charge Test Circuit

### Peak Diode Recovery dV/dt Test Circuit

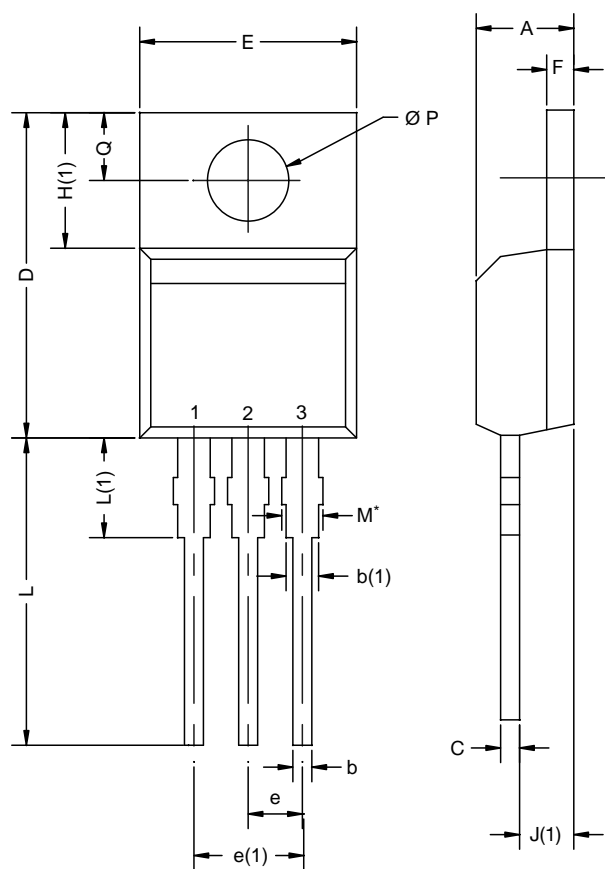


#### Note

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

## TO-220AB



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
Ø P	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118

ECN: X12-0208-Rev. N, 08-Oct-12

DWG: 5471

**Notes**

\* M = 1.32 mm to 1.62 mm (dimension including protrusion)  
Heatsink hole for HVM



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