

FIR60N06G-VB Datasheet

N-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY

| V_{DS} (V) | $R_{DS(on)}$ (Ω) | I_D (A) ^a |
|--------------|---------------------------|------------------------|
| 60 | 0.024 at $V_{GS} = 10$ V | 50 |
| | 0.028 at $V_{GS} = 4.5$ V | 40 |

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Surface Mount
- Available in Tape and Reel
- Dynamic dV/dt Rating
- Logic-Level Gate Drive
- Fast Switching
- Compliant to RoHS Directive 2002/95/EC


RoHS*
 COMPLIANT

TO-220AB



Top View



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

| PARAMETER | | | | SYMBOL | LIMIT | UNIT |
|---|------------------------------------|-------------------------------------|-------|----------------|------------------|------|
| Drain-Source Voltage | | | | V_{DS} | 60 | V |
| Gate-Source Voltage | | | | V_{GS} | ± 20 | |
| Continuous Drain Current ^f | V_{GS} at 10 V | $T_C = 25\text{ }^{\circ}\text{C}$ | I_D | 50 | A | |
| Continuous Drain Current | | $T_C = 100\text{ }^{\circ}\text{C}$ | | 36 | | |
| Pulsed Drain Current ^a | | | | I_{DM} | 200 | |
| Linear Derating Factor | | | | | 1.0 | W/°C |
| Linear Derating Factor (PCB Mount) ^e | | | | | 0.025 | |
| Single Pulse Avalanche Energy ^b | | | | E_{AS} | 400 | mJ |
| Maximum Power Dissipation | $T_C = 25\text{ }^{\circ}\text{C}$ | | | P_D | 150 | W |
| Maximum Power Dissipation (PCB Mount) ^e | $T_A = 25\text{ }^{\circ}\text{C}$ | | | | 3.7 | |
| Peak Diode Recovery dV/dt^c | | | | dV/dt | 4.5 | V/ns |
| Operating Junction and Storage Temperature Range | | | | T_J, T_{stg} | - 55 to + 175 | °C |
| Soldering Recommendations (Peak Temperature) ^d | for 10 s | | | | 300 ^d | |

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25$ V, starting $T_J = 25^\circ\text{C}$, $L = 179\ \mu\text{H}$, $R_g = 25\ \Omega$, $I_{AS} = 51$ A (see fig. 12).
- $I_{SD} \leq 51$ A, $di/dt \leq 250$ A/ μs , $V_{DD} \leq V_{DS}$, $T_J \leq 175^\circ\text{C}$.
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).
- Current limited by the package, (die current = 51 A).

THERMAL RESISTANCE RATINGS

| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
|--|------------|------|------|------|
| Maximum Junction-to-Ambient | R_{thJA} | - | 62 | °C/W |
| Maximum Junction-to-Ambient (PCB Mount) ^a | R_{thJA} | - | 40 | |
| Maximum Junction-to-Case (Drain) | R_{thJC} | - | 1.0 | |

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

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SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|----------------------------------|---|--|------|-------|-------|------|
| Static | | | | | | | |
| Drain-Source Breakdown Voltage | V _{DS} | V _{GS} = 0, I _D = 250 μA | | 60 | - | - | V |
| V _{DS} Temperature Coefficient | ΔV _{DS} /T _J | Reference to 25 °C, I _D = 1 mA | | - | 0.070 | - | V/°C |
| Gate-Source Threshold Voltage | V _{GS(th)} | V _{DS} = V _{GS} , I _D = 250 μA | | 1.0 | - | 2.5 | |
| Gate-Source Leakage | I _{GSS} | V _{GS} = ± 10 V | | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{DS} = 60 V, V _{GS} = 0 V | | - | - | 25 | μA |
| | | V _{DS} = 48 V, V _{GS} = 0 V, T _J = 150 °C | | - | - | 250 | |
| Drain-Source On-State Resistance | R _{DS(on)} | V _{GS} = 10 V | I _D = 21 A ^b | - | 0.024 | - | Ω |
| | | V _{GS} = 4.5 V | I _D = 15 A ^b | - | 0.028 | - | |
| Forward Transconductance | g _{fs} | V _{DS} = 25 V, I _D = 21A ^b | | 23 | - | - | S |
| Dynamic | | | | | | | |
| Input Capacitance | C _{iss} | V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5 | | - | 190 | | pF |
| Output Capacitance | C _{oss} | | | - | 920 | - | |
| Reverse Transfer Capacitance | C _{rss} | | | - | 170 | - | |
| Total Gate Charge | Q _g | V _{GS} = 5.0 V | I _D = 51 A, V _{DS} = 48 V, see fig. 6 and 13 ^b | - | - | 66 | nC |
| Gate-Source Charge | Q _{gs} | | | - | - | 12 | |
| Gate-Drain Charge | Q _{gd} | | | - | - | 43 | |
| Turn-On Delay Time | t _{d(on)} | V _{DD} = 30 V, I _D = 51 A, R _g = 4.6 Ω, R _D = 0.56 Ω, see fig. 10 ^b | | - | 17 | - | ns |
| Rise Time | t _r | | | - | 230 | - | |
| Turn-Off Delay Time | t _{d(off)} | | | - | 2 | - | |
| Fall Time | t _f | | | - | 110 | - | |
| Internal Drain Inductance | L _D | Between lead, 6 mm (0.25") from package and center of die contact | | - | 4.5 | - | nH |
| Internal Source Inductance | L _S | | | - | 7.5 | - | |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous Source-Drain Diode Current | I _S | MOSFET symbol showing the integral reverse p - n junction diode | | - | - | 50° | A |
| Pulsed Diode Forward Current ^a | I _{SM} | | | - | - | 200 | |
| Body Diode Voltage | V _{SD} | T _J = 25 °C, I _S = 51 A, V _{GS} = 0 V ^b | | - | - | 2.5 | V |
| Body Diode Reverse Recovery Time | t _{rr} | T _J = 25 °C, I _F = 51 A, dI/dt = 100 A/μs ^b | | - | 130 | 180 | ns |
| Body Diode Reverse Recovery Charge | Q _{rr} | | | - | 0.84 | 1.3 | μC |
| Forward Turn-On Time | t _{on} | Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D) | | | | | |

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
 b. Pulse width $\leq 300\ \mu\text{s}$; duty cycle $\leq 2\%$.
 c. Current limited by the package, (Die Current = 51 A).

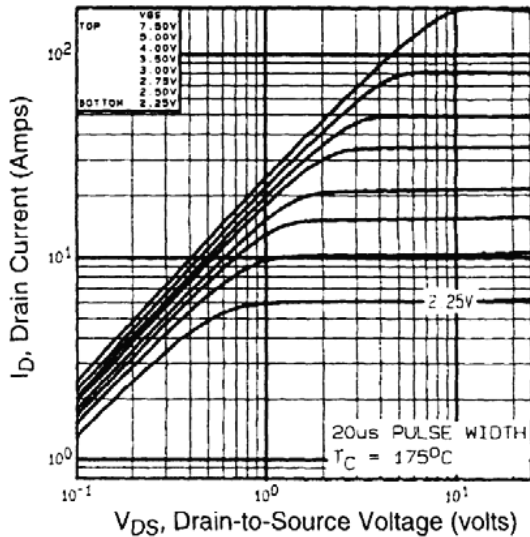
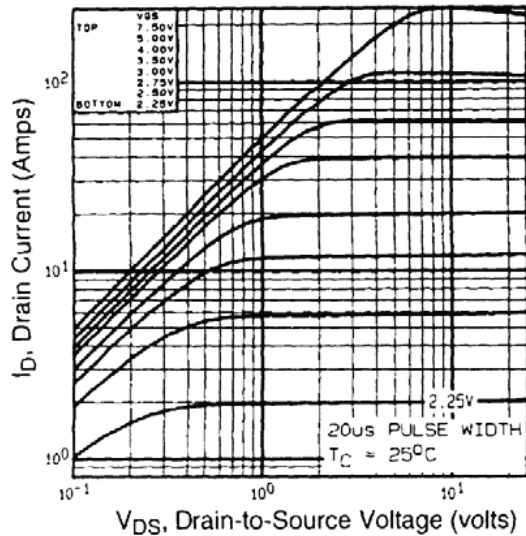
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)




Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



Fig. 7 - Typical Source-Drain Diode Forward Voltage



Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



Fig. 8 - Maximum Safe Operating Area



Fig. 9 - Maximum Drain Current vs. Case Temperature



Fig. 10a - Switching Time Test Circuit

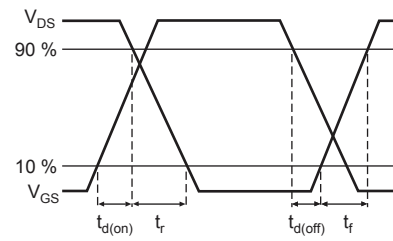


Fig. 10b - Switching Time Waveforms



Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



Fig. 12a - Unclamped Inductive Test Circuit



Fig. 12b - Unclamped Inductive Waveforms



Fig. 12c - Maximum Avalanche Energy vs. Drain Current

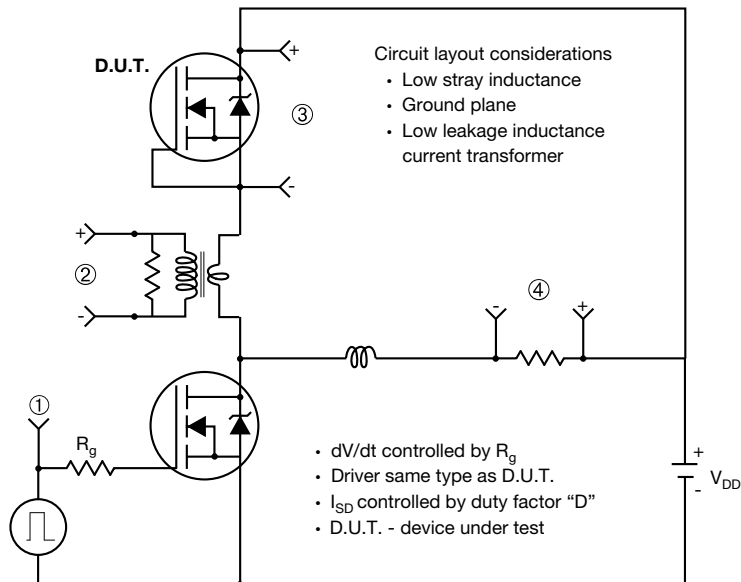


Fig. 13a - Basic Gate Charge Waveform



Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

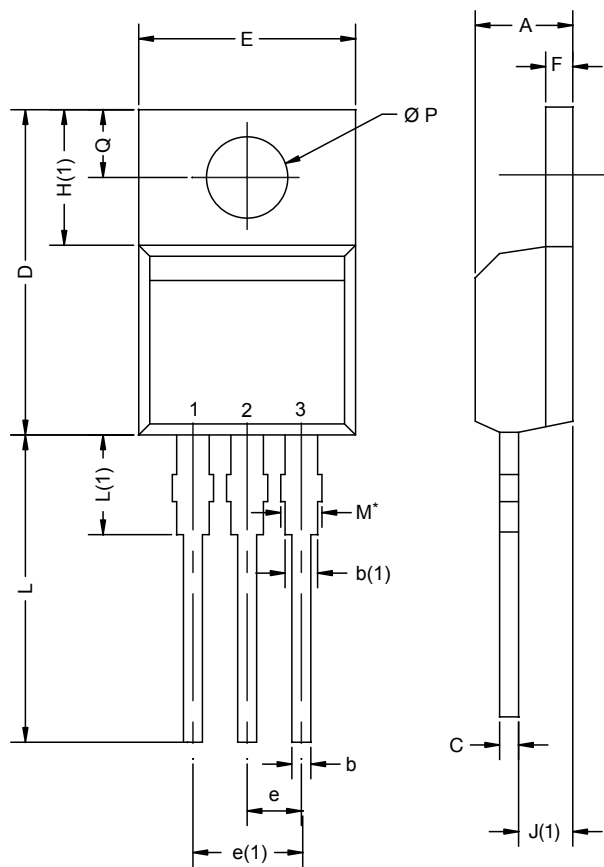


Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

TO-220AB



| DIM. | MILLIMETERS | | INCHES | |
|-----------------|-------------|-------|--------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 4.25 | 4.65 | 0.167 | 0.183 |
| b | 0.69 | 1.01 | 0.027 | 0.040 |
| b(1) | 1.20 | 1.73 | 0.047 | 0.068 |
| c | 0.36 | 0.61 | 0.014 | 0.024 |
| D | 14.85 | 15.49 | 0.585 | 0.610 |
| E | 10.04 | 10.51 | 0.395 | 0.414 |
| e | 2.41 | 2.67 | 0.095 | 0.105 |
| e(1) | 4.88 | 5.28 | 0.192 | 0.208 |
| F | 1.14 | 1.40 | 0.045 | 0.055 |
| H(1) | 6.09 | 6.48 | 0.240 | 0.255 |
| J(1) | 2.41 | 2.92 | 0.095 | 0.115 |
| L | 13.35 | 14.02 | 0.526 | 0.552 |
| L(1) | 3.32 | 3.82 | 0.131 | 0.150 |
| $\varnothing P$ | 3.54 | 3.94 | 0.139 | 0.155 |
| Q | 2.60 | 3.00 | 0.102 | 0.118 |

ECN: X12-0208-Rev. N, 08-Oct-12
DWG: 5471

Notes

* M = 1.32 mm to 1.62 mm (dimension including protrusion)
Heatsink hole for HVM

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