

# F640-VB Datasheet N-Channel 200 V (D-S) MOSFET

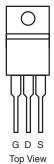
PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A)			
200	0.110 at V <sub>GS</sub> = 10 V	30			

### **FEATURES**

- Trench Power MOSFET
- 175 °C Junction Temperature
- PWM Optimized
- 100 % R<sub>g</sub> Tested
- Compliant to RoHS Directive 2002/95/EC



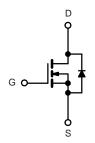
#### **TO-220AB**



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### **APPLICATIONS**

· Primary Side Switch



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)						
Parameter	Symbol	Limit	Unit			
Drain-Source Voltage	V <sub>DS</sub>	200	V			
Gate-Source Voltage	$V_{GS}$	± 20	<b> </b>			
Continuous Drain Courset /T 475 90\b	T <sub>C</sub> = 25 °C	I-	30			
Continuous Drain Current (T <sub>J</sub> = 175 °C) <sup>b</sup>	T <sub>C</sub> = 125 °C	l <sub>D</sub>	15			
Pulsed Drain Current	I <sub>DM</sub>	70	A			
Continuous Source Current (Diode Conduction)	I <sub>S</sub>	12				
Avalanche Current	I <sub>AS</sub>	12				
Single Pulse Avalanche Energy	L = 0.1 mH	E <sub>AS</sub>	20	mJ		
Maximum Dawar Dissination	T <sub>C</sub> = 25 °C	P <sub>D</sub>	126 <sup>b</sup>	10/		
Maximum Power Dissipation	T <sub>A</sub> = 25 °C		3 <sup>a</sup>	W		
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 175	°C			

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Typical	Maximum	Unit		
lunation to Ambiant	t ≤ 10 s	- R <sub>thJA</sub>	15	18	°C/W		
Junction-to-Ambient <sup>a</sup>	Steady State		40	50			
Junction-to-Case (Drain)	•	R <sub>thJC</sub>	0.85	1.1			

#### Notes:

- a. Surface mounted on 1" x 1" FR4 board.
- b. See SOA curve for voltage derating.



Parameter	Symbol	Test Conditions	Min.	Typ. <sup>a</sup>	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	200			V	
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1		3	V	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
		V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V			1		
Zero Gate Voltage Drain Current	$I_{DSS}$	V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C			50	μА	
		V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C			250		
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V	40			Α	
		$V_{GS} = 10 \text{ V}, I_D = 3 \text{ A}$		0.110	0.125	_ Ω	
Danie Course On Chata Besistance	R	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3 A, T <sub>J</sub> = 125 °C		0.120	0.140		
Drain-Source On-State Resistance <sup>b</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3 A, T <sub>J</sub> = 175 °C		0.130	0.150		
		$V_{GS} = 4.5 \text{ V}, I_D = 3 \text{ A}$		0.132	0.152		
Forward Transconductance <sup>b</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 3 A		35		S	
Dynamic <sup>a</sup>							
Input Capacitance	$C_{iss}$			1800		pF	
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 \text{ V}, V_{DS} = 25 \text{ V}, F = 1 \text{ MHz}$		180			
Reverse Transfer Capacitance	C <sub>rss</sub>			80			
Total Gate Charge <sup>c</sup>	$Q_g$			34	51		
Gate-Source Charge <sup>c</sup>	$Q_{gs}$	$V_{DS} = 100 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 3 \text{ A}$		8		nC	
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			12			
Gate Resistance	$R_g$		0.5		2.9	Ω	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			15	25		
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD} = 100 \text{ V}, R_{L} = 5.2 \Omega$		50	75	ns	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>	$I_D \cong 3 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 2.5 \Omega$		30	45	115	
Fall Time <sup>c</sup>	t <sub>f</sub>			60	90		
Source-Drain Diode Ratings and Char	acteristics (7	T <sub>C</sub> = 25 °C)					
Pulsed Current	I <sub>SM</sub>				30	Α	
Diode Forward Voltage <sup>b</sup>	$V_{SD}$	I <sub>F</sub> = 3 A, V <sub>GS</sub> = 0 V		0.9	1.5	V	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 3 A, dI/dt = 100 A/μs		180	250	ns	

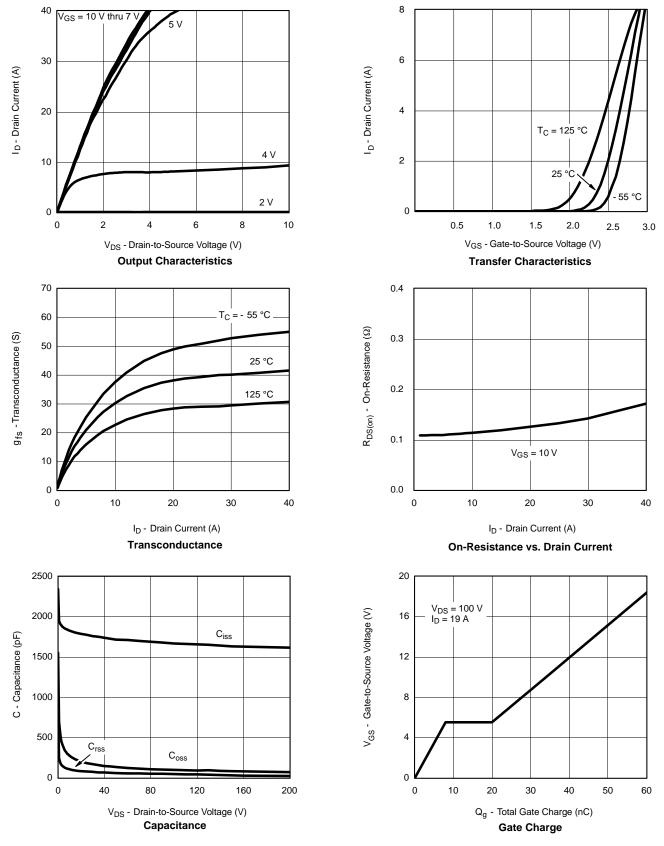
#### Notes:

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

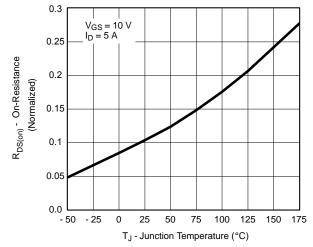


## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

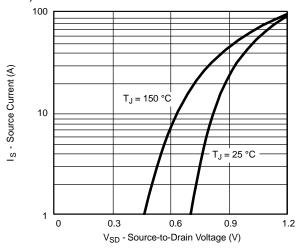




### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



On-Resistance vs. Junction Temperature

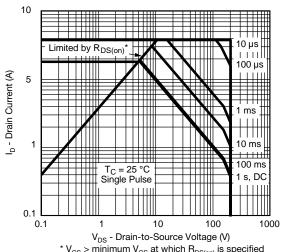


Source-Drain Diode Forward Voltage

### THERMAL RATINGS

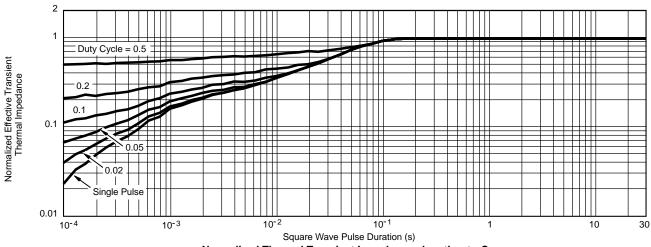


Maximum Avalanche Drain Current vs. Case Temperature



\* V<sub>GS</sub> > minimum V<sub>GS</sub> at which R<sub>DS(on)</sub> is specified

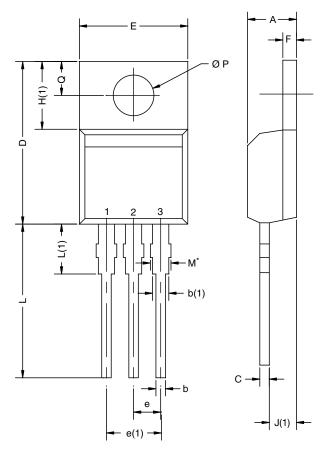
Safe Operating Area

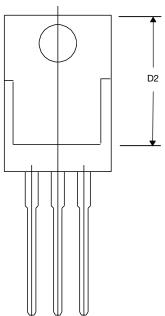


Normalized Thermal Transient Impedance, Junction-to-Case



## **TO-220AB**





	MILLIN	IETERS	INC	HES	
DIM.	MIN.	MAX.	MIN.	MAX.	
А	4.25	4.65	0.167	0.183	
b	0.69	1.01	0.027	0.040	
b(1)	1.20	1.73	0.047	0.068	
С	0.36	0.61	0.014	0.024	
D	14.85	15.49	0.585	0.610	
D2	12.19	12.70	0.480	0.500	
Е	10.04	10.51	0.395	0.414	
е	2.41	2.67	0.095	0.105	
e(1)	4.88	5.28	0.192	0.208	
F	1.14	1.40	0.045	0.055	
H(1)	6.09	6.48	0.240	0.255	
J(1)	2.41	2.92	0.095	0.115	
L	13.35	14.02	0.526	0.552	
L(1)	3.32	3.82	0.131	0.150	
ØΡ	3.54	3.94	0.139	0.155	
Q	2.60	3.00	0.102	0.118	
ECN: T14-0413-Rev. P, 16-Jun-14 DWG: 5471					

### Note

 $<sup>^{\</sup>star}$  M = 1.32 mm to 1.62 mm (dimension including protrusion) Heatsink hole for HVM



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