

# BUK9509-75A-VB Datasheet N-Channel 80 V (D-S) MOSFET

PRODUCT SUMMARY		
V <sub>DS</sub>	80	V
$R_{DS(on)} V_{GS} = 10 V$	7	mΩ
$R_{DS(on)}$ $V_{GS} = 4.5 \text{ V}$	9	mΩ
I <sub>D</sub>	100	Α
Configuration	Single	

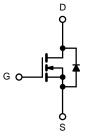
#### **FEATURES**

- Trench Power MOSFET
- $\bullet$  100 %  $R_g$  and UIS Tested



### **APPLICATIONS**

- Primary Side Switching
- Synchronous Rectification
- DC/AC Inverters
- LED Backlighting



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TO-220AB

	G C
Top View	S N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (	T <sub>A</sub> = 25 °C, unless	otherwise note	ed)	
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	80	V	
Gate-Source Voltage	V <sub>GS</sub>	± 20	<b>□</b>	
	T <sub>C</sub> = 25 °C		100a	
Continuous Dunin Comment /T 150 °C	T <sub>C</sub> = 70 °C	1 . 🗆	85 <sup>a</sup>	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>A</sub> = 25 °C	I <sub>D</sub>	28.6 <sup>b, c</sup>	
	T <sub>A</sub> = 70 °C		24.9 <sup>b, c</sup>	
Pulsed Drain Current (t = 100 μs)	I <sub>DM</sub>	350	Α Α	
Continuous Constant District Constant	T <sub>C</sub> = 25 °C		80 <sup>a</sup>	
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	l <sub>S</sub>	4.5 <sup>b, c</sup>	
Single Pulse Avalanche Current	. 0.1!!	I <sub>AS</sub>	30	
Single Pulse Avalanche Energy	L = 0.1 mH	E <sub>AS</sub>	45	mJ
Maximum Power Dissipation	T <sub>C</sub> = 25 °C		180	
	T <sub>C</sub> = 70 °C		120	,,,
	T <sub>A</sub> = 25 °C	P <sub>D</sub>	5 <sup>b, c</sup>	W
	T <sub>A</sub> = 70 °C		3.2 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C
Soldering Recommendations (Peak Temperature		260		

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient <sup>a</sup>	t ≤ 10 sec	R <sub>thJA</sub>	15	18		
	Steady State		40	50	°C/W	
Maximum Junction-to-Case	·	R <sub>thJC</sub>	0.85	1.1		

#### Notes

- a. Package limited.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 10 s.



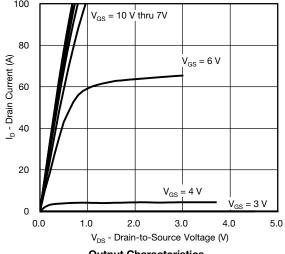
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static					l .		
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	80			V	
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>			37		1400	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA		- 6.1		mV/°C	
Gate-Source Threshold Voltage	V <sub>GS(th</sub> )	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2.0		3.5	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
	_	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$			1		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			10	μA	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	85			Α	
	. ,	$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$		7		+	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 6 \text{ V}, I_D = 15 \text{ A}$		7. 5		mΩ	
	, ,	$V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$		9			
Forward Transconductancea	9 <sub>fs</sub>	$V_{DS} = 10 \text{ V}, I_D = 20 \text{ A}$		60		S	
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>			3855			
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		1120		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>			376		1	
	Qg	$V_{DS} = 40 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$		35.5			
Total Gate Charge		$V_{DS} = 40 \text{ V}, V_{GS} = 6 \text{ V}, I_D = 10 \text{ A}$		22			
				18		nC	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 40 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$		5.3			
Gate-Drain Charge	$Q_{gd}$			7.3			
Output Charge	Q <sub>oss</sub>	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$		57	86		
Gate Resistance	$R_{g}$	f = 1 MHz	0.5	1.3	2	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			12	24		
Rise Time	t <sub>r</sub>	$V_{DD} = 40 \text{ V}, R_L = 4 \Omega$		8	16		
Turn-Off DelayTime	t <sub>d(off)</sub>	$I_D \cong 10^{\circ} \text{A}, V_{GEN} = 10^{\circ} \text{V}, R_g = 1^{\circ} \Omega$		32	64		
Fall Time	t <sub>f</sub>			7	14	1	
Turn-On Delay Time	t <sub>d(on)</sub>			14	28	ns	
Rise Time	t <sub>r</sub>	$V_{DD} = 40 \text{ V}, R_{L} = 4 \Omega$		11	22	1	
Turn-Off DelayTime	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 6.0 \text{ V}, R_g = 1 \Omega$		30	60		
Fall Time	t <sub>f</sub>			8	16		
Drain-Source Body Diode Characteristic	s						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			75	А	
Pulse Diode Forward Current (t = 100 μs)	I <sub>SM</sub>				150	^	
Body Diode Voltage	$V_{SD}$	I <sub>S</sub> = 5 A		0.76	1.1	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			38	75	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> = 10 A, dl/dt = 100 A/μs, T <sub>J</sub> = 25 °C		36	70	nC	
Reverse Recovery Fall Time	t <sub>a</sub>	$I_F = 10 \text{ A}$ , $\Omega I/\Omega I = 100 \text{ A}/\mu \text{S}$ , $I_J = 25 \text{ °C}$		19			
Reverse Recovery Rise Time	t <sub>b</sub>			19		ns	

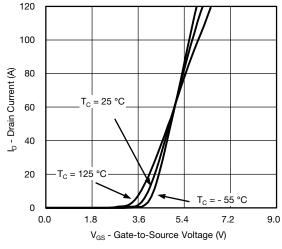
#### Notes

- a. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

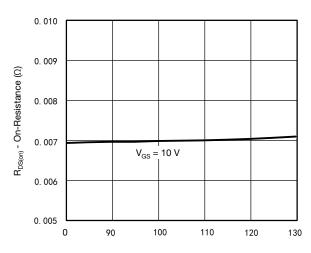


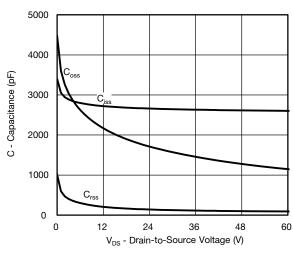






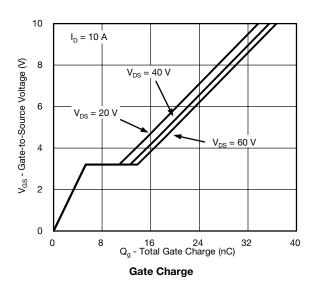


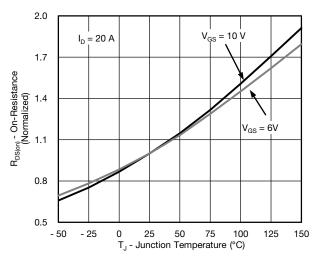




## On-Resistance vs. Drain Current

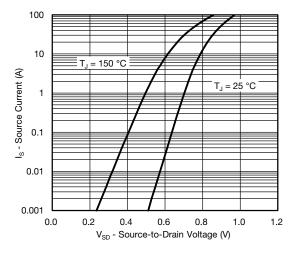
Capacitance



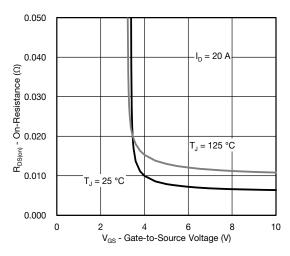


On-Resistance vs. Junction Temperature

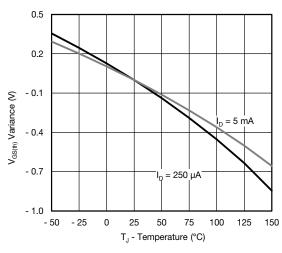




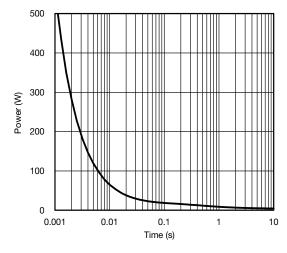
Source-Drain Diode Forward Voltage



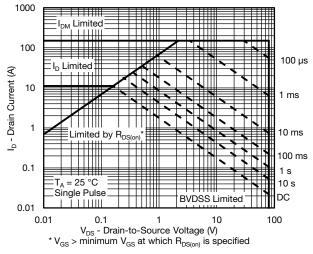
On-Resistance vs. Gate-to-Source Voltage



**Threshold Voltage** 

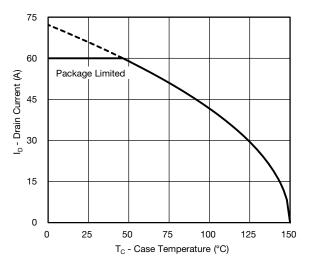


Single Pulse Power, Junction-to-Ambient

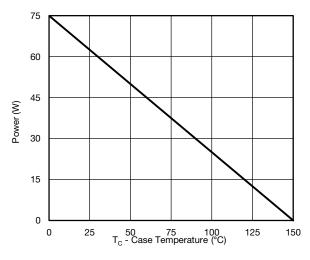


Safe Operating Area, Junction-to-Ambient

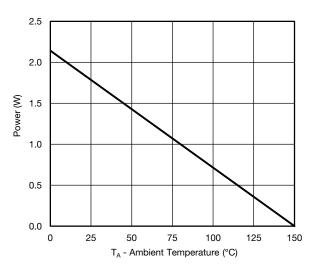




#### **Current Derating\***



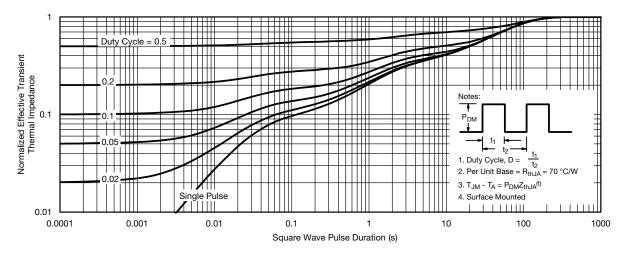




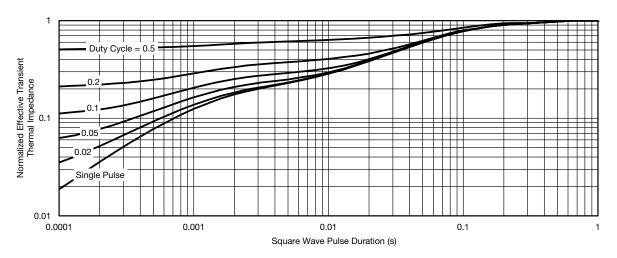
Power, Junction-to-Ambient

<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max.)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





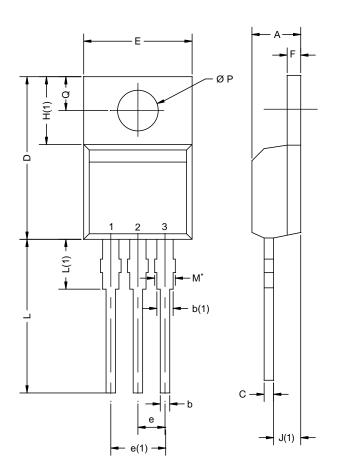
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case



## **TO-220AB**



	MILLIMETERS		INC	HES	
DIM.	MIN.	MAX.	MIN.	MAX.	
Α	4.25	4.65	0.167	0.183	
b	0.69	1.01	0.027	0.040	
b(1)	1.20	1.73	0.047	0.068	
С	0.36	0.61	0.014	0.024	
D	14.85	15.49	0.585	0.610	
Е	10.04	10.51	0.395	0.414	
е	2.41	2.67	0.095	0.105	
e(1)	4.88	5.28	0.192	0.208	
F	1.14	1.40	0.045	0.055	
H(1)	6.09	6.48	0.240	0.255	
J(1)	2.41	2.92	0.095	0.115	
L	13.35	14.02	0.526	0.552	
L(1)	3.32	3.82	0.131	0.150	
ØР	3.54	3.94	0.139	0.155	
Q	2.60	3.00	0.102	0.118	
ECN: X12-0208-Rev. N, 08-Oct-12 DWG: 5471					

#### Notes

 $<sup>^{\</sup>star}$  M = 1.32 mm to 1.62 mm (dimension including protrusion) Heatsink hole for HVM



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