

## MI3130-VB Datasheet

# N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY							
V <sub>DS</sub> (V)	$R_{DS(on)}$ ( $\Omega$ )	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)				
30	0.022 at V <sub>GS</sub> = 4.5 V	6.8	10 nC				
	0.030 at V <sub>GS</sub> = 2.5 V	6.0	TONC				

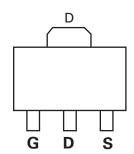
#### **FEATURES**

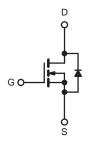
- Halogen-free
- Trench Power MOSFET



#### **APPLICATIONS**

· Load Switches for Portable Devices





N-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATIN</b>	IGS $T_A = 25  ^{\circ}C$ ,	unless othe	rwise noted	
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage		$V_{DS}$	30	V
Gate-Source Voltage		$V_{GS}$	± 20	V
	T <sub>C</sub> = 25 °C	-	6.8 <sup>a</sup>	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	$T_C = 70 ^{\circ}\text{C}$ $T_A = 25 ^{\circ}\text{C}$	- I <sub>D</sub> -	6.8 <sup>a, b, c</sup>	
	T <sub>A</sub> = 70 °C		6 <sup>a, b, c</sup>	A
Pulsed Drain Current		I <sub>DM</sub>	30	
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C	I <sub>S</sub>	5.2	
Commission Course Plant Pleas Carrent	T <sub>A</sub> = 25 °C	.3	2.1 <sup>b, c</sup>	
	T <sub>C</sub> = 25 °C	] [	6.3	
Maximum Power Dissipation	$T_C = 70  ^{\circ}C$	P <sub>D</sub>	4	w
Maximum i ower bissipation	T <sub>A</sub> = 25 °C	١ ٠ ١	2.5 <sup>b, c</sup>	**
	T <sub>A</sub> = 70 °C		1.6 <sup>b, c</sup>	
Operating Junction and Storage Temperature	e Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C
Soldering Recommendations (Peak Tempera	ature) <sup>e, f</sup>		260	

THERMAL RESISTANCE RATINGS								
Parameter	Symbol	Typical	Maximum	Unit				
Maximum Junction-to-Ambient <sup>a, c, d</sup>	t ≤ 5 s	R <sub>thJA</sub>	40	50	°C/W			
Maximum Junction-to-Foot (Drain)	Steady State	$R_{thJF}$	15	20	] 5/**			

- a. Package limited, T<sub>C</sub> = 25 °C.
  b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. Maximum under Steady State conditions is 95 °C/W.
- e. See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- f. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.



Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static					L		
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	J 250 A		25			
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250  \mu A$		- 4.0		mV/°C	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	0.6		1.5	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zana Oata Waltana Bush Oamaal		$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$			1		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			10	μA	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	30			Α	
_		$V_{GS} = 4.5 \text{ V}, I_D = 6.3 \text{ A}$		0.022		Ω	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 2.5 \text{ V}, I_D = 4.5 \text{ A}$		0.030			
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 6.3 A		45		S	
Dynamic <sup>b</sup>				l			
Input Capacitance	C <sub>iss</sub>			1200			
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		220		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>			100			
Tatal Oata Obanna		$V_{DS} = 10 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 6.3 \text{ A}$		22	33	nC	
Total Gate Charge	Qg			10	15		
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 6.3 \text{ A}$		2.5			
Gate-Drain Charge	$Q_{gd}$			1.7			
Gate Resistance	R <sub>g</sub>	f = 1 MHz		2.4		Ω	
Turn-on Delay Time	t <sub>d(on)</sub>			15	25		
Rise Time	t <sub>r</sub>	$V_{DD}$ = 10 V, $R_L$ = 1.5 $\Omega$		10	15		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D\cong 6.7$ A, $V_{GEN}$ = 4.5 V, $R_g$ = 1 $\Omega$		35	55		
Fall Time	t <sub>f</sub>			12	20		
Turn-on Delay Time	t <sub>d(on)</sub>			10	15	ns	
Rise Time	t <sub>r</sub>	$V_{DD}$ = 10 V, $R_L$ = 1.5 $\Omega$		12	20		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D\cong 6.7$ A, $V_{GEN}$ = 10 V, $R_g$ = 1 $\Omega$		25	40		
Fall Time	t <sub>f</sub>			10	15	1	
<b>Drain-Source Body Diode Characteristi</b>	cs					•	
Continuous Source-Drain Diode Current	I <sub>S</sub>	$T_C = 25  ^{\circ}C$			5.2	А	
Pulse Diode Forward Current	I <sub>SM</sub>				30	_ ^	
Body Diode Voltage	$V_{SD}$	I <sub>S</sub> = 6.7 A, V <sub>GS</sub> = 0 V		0.8	1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			20	40	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> = 6.7 A, dI/dt = 100 A/μs, T <sub>J</sub> = 25 °C		10	20	nC	
Reverse Recovery Fall Time	t <sub>a</sub>	i <sub>F</sub> = 0.7 A, αίναι = 100 Ανμ5, 1 <sub>J</sub> = 25 °C		10			
Reverse Recovery Rise Time	t <sub>b</sub>	t <sub>b</sub>		10		ns	

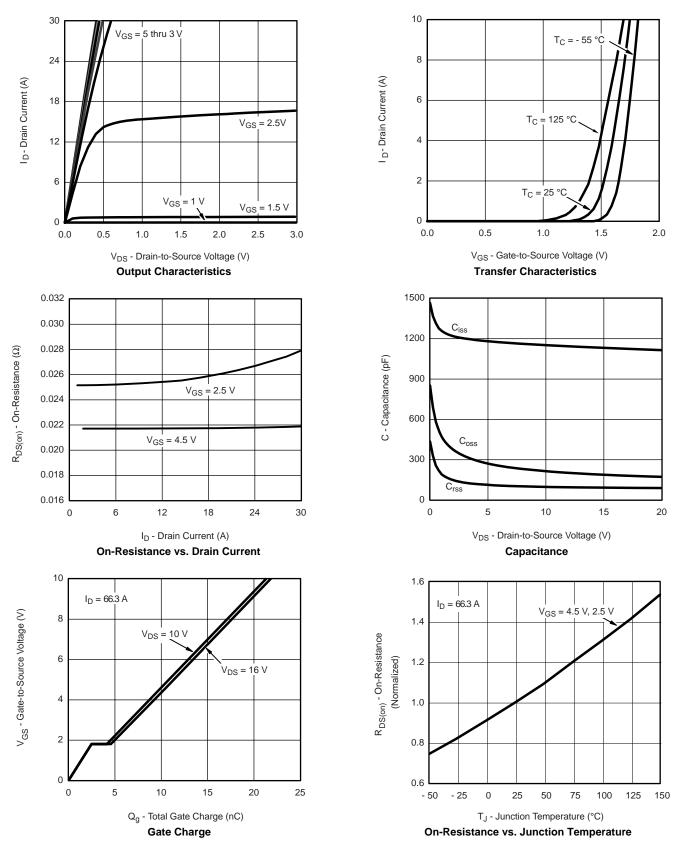
#### Notes:

- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%$
- b. Guaranteed by design, not subject to production testing.

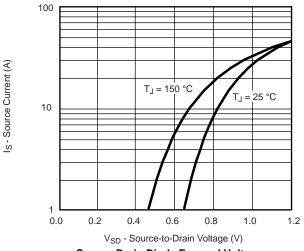
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

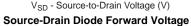
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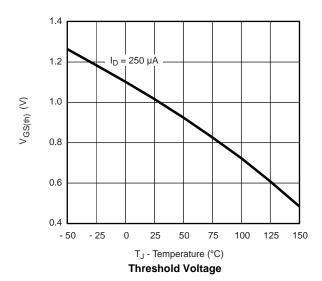


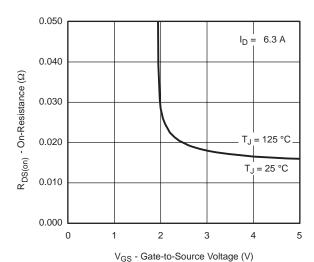




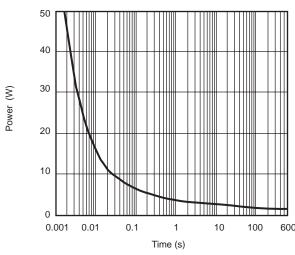




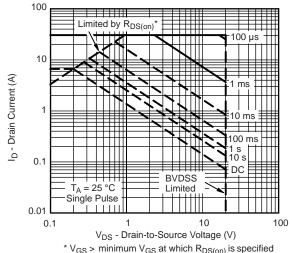




On-Resistance vs. Gate-to-Source Voltage



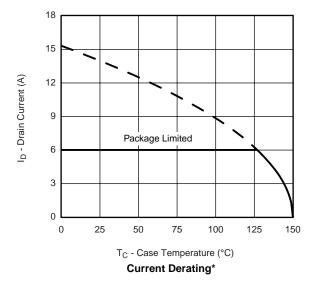
Single Pulse Power

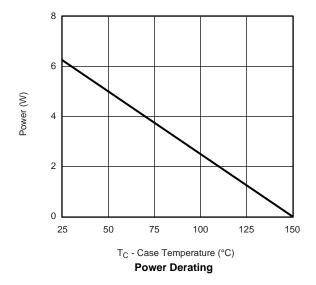


\*  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

Safe Operating Area, Junction-to-Ambient



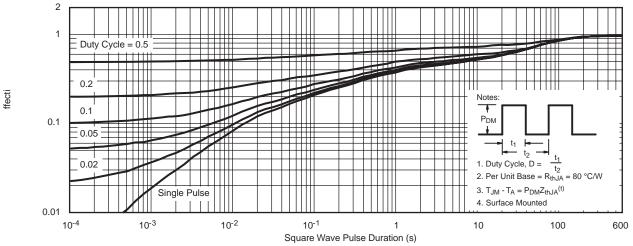




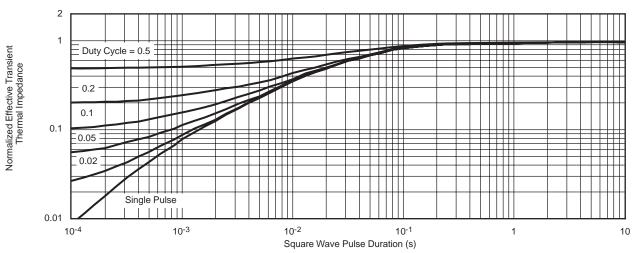
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<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





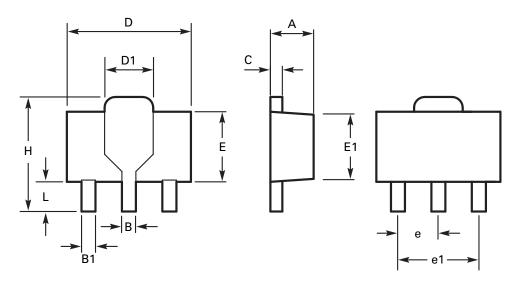
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot



## Package outline - SOT89



DIM	Millin	neters	Inc	Inches DIM Millimeters Inches		Millimeters		hes	
	Min	Max	Min	Max		Min	Max	Min	Max
Α	1.40	1.60	0.550	0.630	Е	2.29	2.60	0.090	0.102
В	0.44	0.56	0.017	0.022	E1	2.13	2.29	0.084	0.090
B1	0.36	0.48	0.014	0.019	е	1.50 BSC		0.059 BSC	
С	0.35	0.44	0.014	0.017	e1	3.00 BSC		0.118 BSC	
D	4.40	4.60	0.173	0.181	Н	3.94	4.25	0.155	0.167
D1	1.62	1.83	0.064	0.072	L	0.89	1.20	0.035	0.047

Note: Controlling dimensions are in millimeters. Approximate dimensions are provided in inches

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