

## SI3446DV-T1-GE3-VB Datasheet N-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY						
V <sub>DS</sub> (V)	$R_{DS(on)}\left(\Omega\right)$	I <sub>D</sub> (A) <sup>a, e</sup>	Q <sub>g</sub> (Typ.)			
30	0.023 at V <sub>GS</sub> = 10 V	6	4.2 nC			
30	0.027 at V <sub>GS</sub> = 4.5 V	6	4.2110			

# TSOP-6 D 1 6 D D 2 5 D G 3 4 S Top View

#### **FEATURES**

- Halogen-free According to IEC 61249-2-21 Definition
- Trench Power MOSFET
- Low On-Resistance
- 100 % R<sub>g</sub> Tested
- Compliant to RoHS Directive 2002/95/EC



#### **APPLICATIONS**

• DC/DC Converters, High Speed Switching

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage		V <sub>DS</sub>	30	V
Gate-Source Voltage		V <sub>GS</sub>	± 20	
	T <sub>C</sub> = 25 °C		6 <sup>e</sup>	
Continuous Proin Current /T 450 °C)	T <sub>C</sub> = 70 °C	,	6 <sup>e</sup>	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>A</sub> = 25 °C	- I <sub>D</sub>	5.5 <sup>b, c</sup>	
	T <sub>A</sub> = 70 °C		4.4 <sup>b, c</sup>	А
Pulsed Drain Current (t = 300 μs)		I <sub>DM</sub> 25		
0 0 0	T <sub>C</sub> = 25 °C		2.1	
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	ls —	1.1 <sup>b, c</sup>	
	T <sub>C</sub> = 25 °C		2.5	
Manine de Deves Dissination	T <sub>C</sub> = 70 °C		1.6	w
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	1.3 <sup>b, c</sup>	VV
	T <sub>A</sub> = 70 °C		0.8 <sup>b, c</sup>	
Operating Junction and Storage Temperature	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	90	
Soldering Recommendations (Peak Tempera		260	°C	

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	Typical	Maximum	Unit			
Maximum Junction-to-Ambient <sup>b, d</sup>	t ≤ 5 s	R <sub>thJA</sub>	75	100	°C/W		
Maximum Junction-to-Foot (Drain)	Steady State	R <sub>thJF</sub>	40	50	C/ VV		

#### Notes:

- a. Based on  $T_C = 25$  °C.
- b. Surface mounted on 1" x 1" FR4 board.
- c t = 5 s
- d. Maximum under steady state conditions is 166 °C/W.
- e. Package limited.

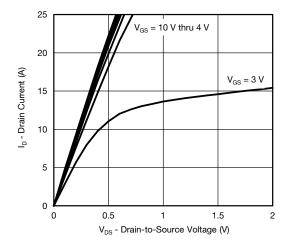


Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static					•	
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V, I}_{D} = 250 \mu\text{A}$	30			V
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = 250 μA		30		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA		- 4.8		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	0.5		1.5	V
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zara Oata Valta va Basis Oamast	I <sub>DSS</sub>	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
Zero Gate Voltage Drain Current		$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 70 ^{\circ}\text{C}$			10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \le 5 \text{ V}, V_{GS} = 10 \text{ V}$	20			А
		$V_{GS} = 10 \text{ V}, I_D = 5.5 \text{ A}$		0.023		
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 5 A		0.027		Ω
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 5.5 A		24		S
Dynamic <sup>b</sup>					l	
Input Capacitance	C <sub>iss</sub>			424		pF
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		100		
Reverse Transfer Capacitance	C <sub>rss</sub>			42		
· ·	Qg	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 5.5 \text{ A}$		8.2	13	nC
Total Gate Charge				4.2	7	
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 5.5 \text{ A}$		1.4		
Gate-Drain Charge	Q <sub>gd</sub>			1.4		
Gate Resistance	$R_{g}$	f = 1 MHz	2.5	12.6	25.2	Ω
Turn-On Delay Time	t <sub>d(on)</sub>			6	12	
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 3.4 $\Omega$		20	30	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 4.4 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		14	21	
Fall Time	t <sub>f</sub>			10	20	
Turn-On Delay Time	t <sub>d(on)</sub>			3	6	ns
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 3.4 $\Omega$		11	20	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 4.4 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		20	30	
Fall Time	t <sub>f</sub>			7	14	
<b>Drain-Source Body Diode Characteristic</b>	s			L		
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			2.1	^
Pulse Diode Forward Current	I <sub>SM</sub>				25	A
Body Diode Voltage	V <sub>SD</sub>	$I_S = 4.4 \text{ A}, V_{GS} = 0 \text{ V}$		0.82	1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>			13	20	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	1 444 dil/dt 400 A/v- T 05 00		6	12	nC
Reverse Recovery Fall Time	t <sub>a</sub>	$I_F = 4.4 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$		8		
Reverse Recovery Rise Time	t <sub>b</sub>			5		ns

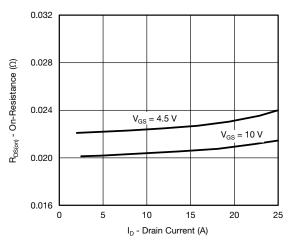
- a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %. b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

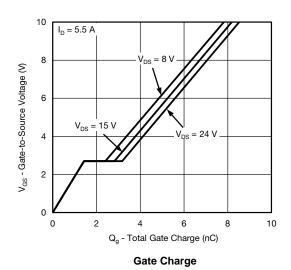




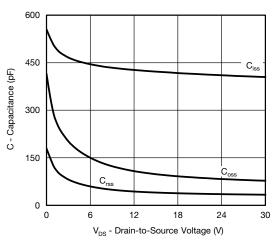
#### **Output Characteristics**



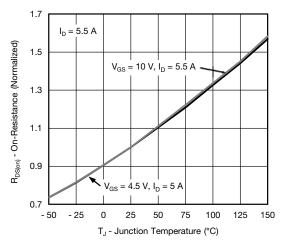
On-Resistance vs. Drain Current and Gate Voltage



**Transfer Characteristics** 

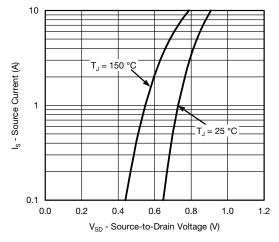


Capacitance

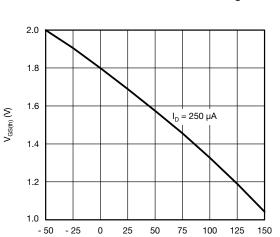


On-Resistance vs. Junction Temperature



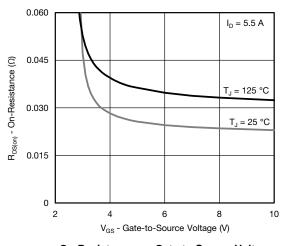


#### Source-Drain Diode Forward Voltage

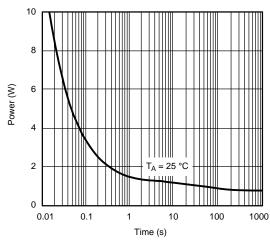


T<sub>J</sub> - Temperature (°C)

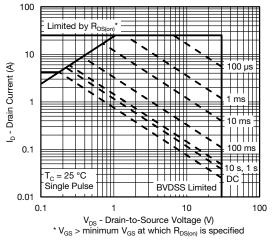
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage

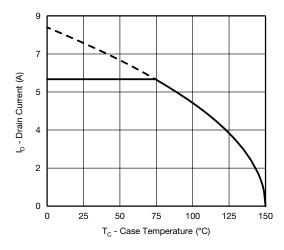


Single Pulse Power (Junction-to-Ambient)

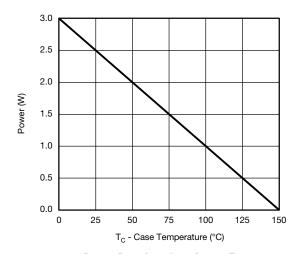


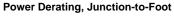
Safe Operating Area, Junction-to-Ambient

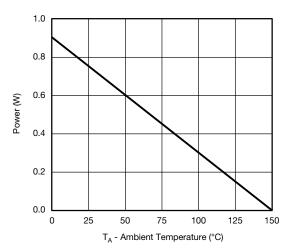




#### **Current Derating\***



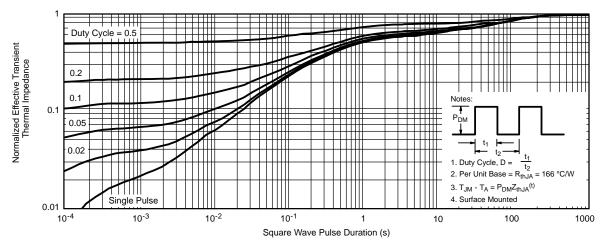




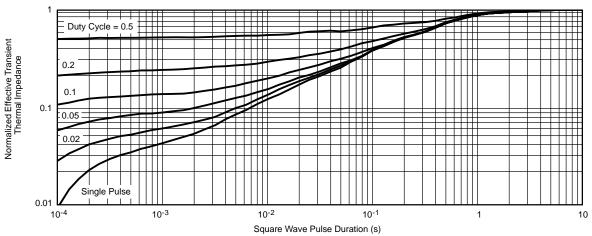
Power Derating, Junction-to-Ambient

<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max.)}$  = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot



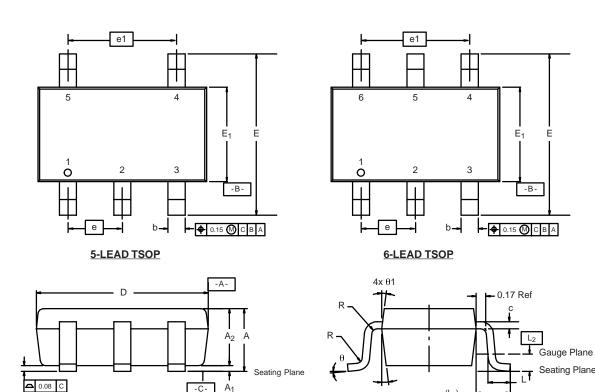
Seating Plane

(L<sub>1</sub>) -

4x θ1

TSOP: 5/6-LEAD

**JEDEC Part Number: MO-193C** 

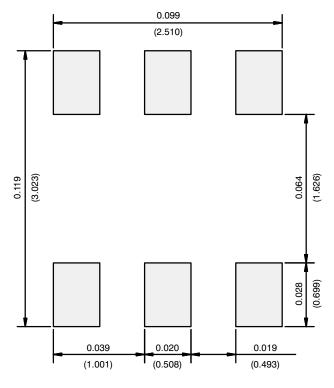


-C- A<sub>1</sub>

	MIL	LIMETER	RS	INCHES			
Dim	Min	Nom	Max	Min	Nom	Max	
Α	0.91	-	1.10	0.036	-	0.043	
A <sub>1</sub>	0.01	-	0.10	0.0004	-	0.004	
A <sub>2</sub>	0.90	-	1.00	0.035	0.038	0.039	
b	0.30	0.32	0.45	0.012	0.013	0.018	
С	0.10	0.15	0.20	0.004	0.006	0.008	
D	2.95	3.05	3.10	0.116	0.120	0.122	
Е	2.70	2.85	2.98	0.106	0.112	0.117	
E <sub>1</sub>	1.55	1.65	1.70	0.061	0.065	0.067	
е	0.95 BSC			0.0374 BSC			
e <sub>1</sub>	1.80	1.90	2.00	0.071	0.075	0.079	
L	0.32	-	0.50	0.012	-	0.020	
L <sub>1</sub>	0.60 Ref			0.024 Ref			
L <sub>2</sub>	0.25 BSC			0.010 BSC			
R	0.10	-	-	0.004	-	-	
θ	0°	4°	8°	0°	4°	8°	
$\theta_1$	7° Nom			7° Nom			
ECN: C-06593-Rev. I, 18-Dec-06 DWG: 5540							



#### **RECOMMENDED MINIMUM PADS FOR TSOP-6**



Recommended Minimum Pads Dimensions in Inches/(mm)



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