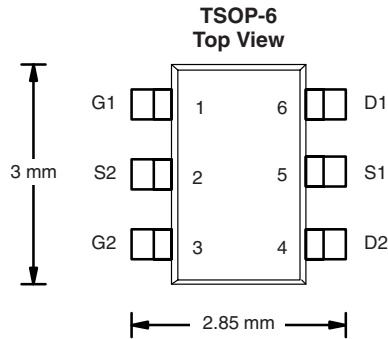


FDC8602-VB Datasheet

Dual N-Channel 100 V (D-S) MOSFET

MOSFET PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
100	0.140 at $V_{GS} = 10$ V	2.0	2.9 nC
	0.160 at $V_{GS} = 6$ V	1.8	
	0.180 at $V_{GS} = 4.5$ V	1.7	



FEATURES

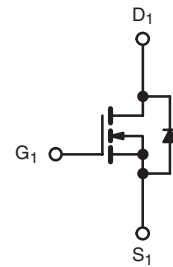
- Halogen-free According to IEC 61249-2-21 Definition
- Trench Power MOSFET
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



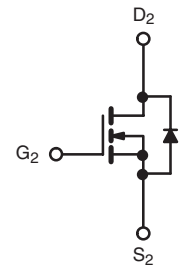
RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- CCFL Inverter
- DC/DC Converter
- HDD



N-Channel MOSFET



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	2
		$T_C = 70$ °C	1.8
		$T_A = 25$ °C	1.6 ^{b, c}
		$T_A = 70$ °C	1.3 ^{b, c}
Pulsed Drain Current ($t = 300$ μ s)	I_{DM}	7	A
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C	2.1
		$T_A = 25$ °C	1.0 ^{b, c}
Single Pulse Avalanche Current	I_{AS}	5	A
Single Pulse Avalanche Energy	E_{AS}	1.25	mJ
Maximum Power Dissipation	P_D	$T_C = 25$ °C	2.5
		$T_C = 70$ °C	1.6
		$T_A = 25$ °C	1.25 ^{b, c}
		$T_A = 70$ °C	0.8 ^{b, c}
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	R_{thJA}	75	100	°C/W
Maximum Junction-to-Foot (Drain)	R_{thJF}	40	50	°C/W

Notes:

- Based on $T_C = 25$ °C.
- Surface mounted on 1" x 1" FR4 board.
- $t = 5$ s.
- Maximum under steady state conditions is 166 °C/W.

MOSFET SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{DS} = 0 V, I _D = 250 μA	100			V	
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		105		mV/°C	
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 5.2			
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.2		2.8	V	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V			- 1	μA	
		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 55 °C			- 10		
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 4.5 V	5			A	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 1.5 A		0.140		Ω	
		V _{GS} = 6 V, I _D = 1 A		0.160			
		V _{GS} = 4.5 V, I _D = 0.5 A		0.180			
Forward Transconductance ^a	g _{fs}	V _{DS} = 20 V, I _D = 1.5 A		2.0		S	
Dynamic ^b							
Input Capacitance	C _{iss}	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz		190		pF	
Output Capacitance	C _{oss}			22			
Reverse Transfer Capacitance	C _{rss}			13			
Total Gate Charge	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 1.6 A		5.2	10.4	nC	
Gate-Source Charge	Q _{gs}	V _{DS} = 50 V, V _{GS} = 4.5 V, I _D = 1.6 A		2.9	5.8		
Gate-Drain Charge	Q _{gd}			0.75			
Gate Resistance	R _g			1.4			
Turn-On Delay Time	t _{d(on)}	f = 1 MHz	0.3	1.4	2.8	Ω	
Rise Time	t _r		V _{DD} = 50 V, R _L = 39 Ω I _D = 1.3 A, V _{GEN} = 4.5 V, R _g = 1 Ω		30		45
Turn-Off Delay Time	t _{d(off)}				26		39
Fall Time	t _f				17		26
Turn-On Delay Time	t _{d(on)}	V _{DD} = 50 V, R _L = 39 Ω I _D = 1.3 A, V _{GEN} = 10 V, R _g = 1 Ω			12		20
Rise Time	t _r			6	12		
Turn-Off Delay Time	t _{d(off)}			10	20		
Fall Time	t _f			10	20		
Fall Time	t _f			6	12		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			- 2.1		A
Pulse Diode Forward Current ^a	I _{SM}				- 20		
Body Diode Voltage	V _{SD}	I _S = 1.3 A		- 0.8	- 1.2		V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 1.3 A, dI/dt = 100 A/μs, T _J = 25 °C		22	33	ns	
Body Diode Reverse Recovery Charge	Q _{rr}			21	32	nC	
Reverse Recovery Fall Time	t _a			16		ns	
Reverse Recovery Rise Time	t _b			6			

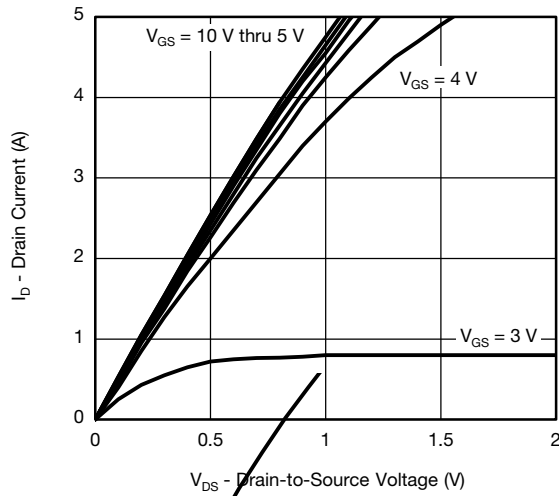
Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

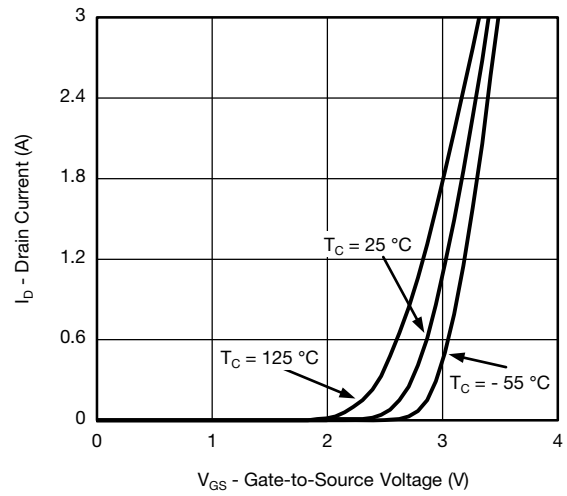
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

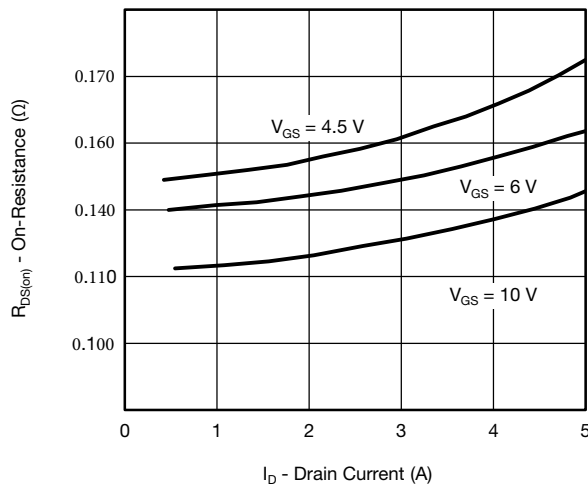
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



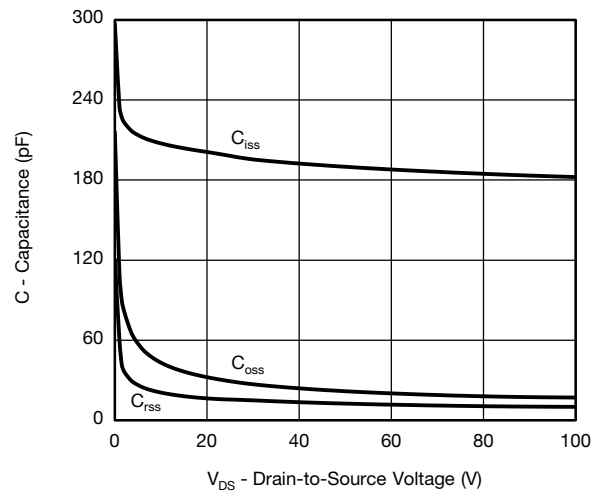
Output Characteristics



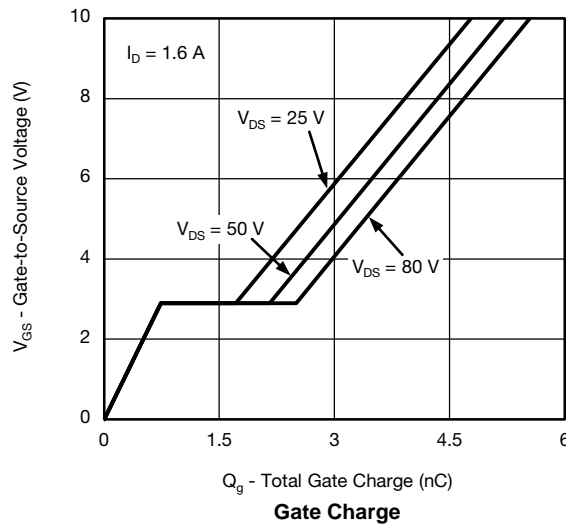
Transfer Characteristics



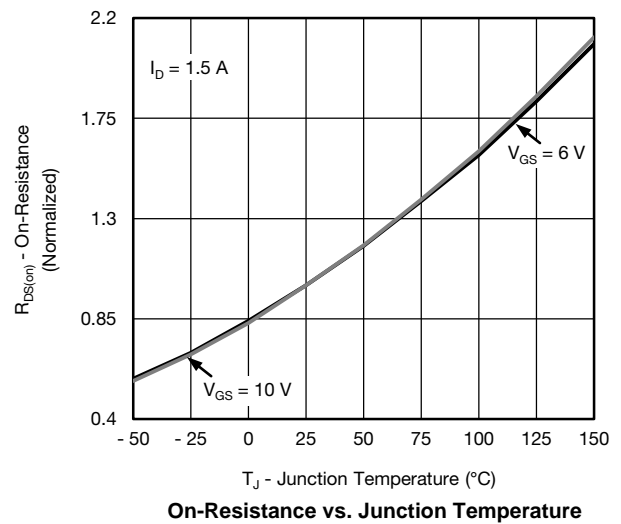
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

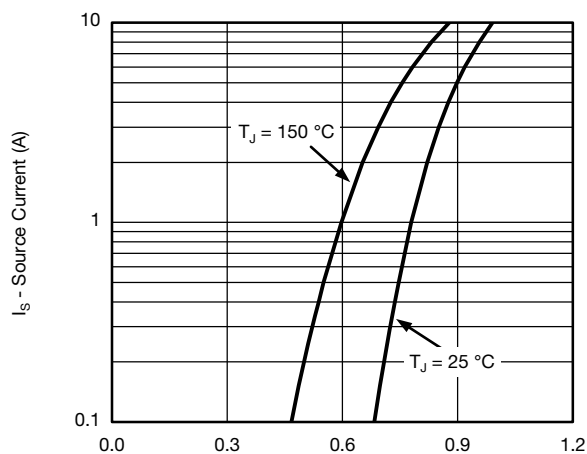


Gate Charge

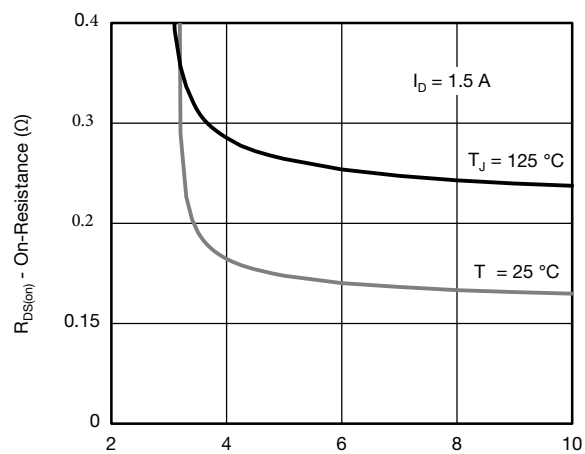


On-Resistance vs. Junction Temperature

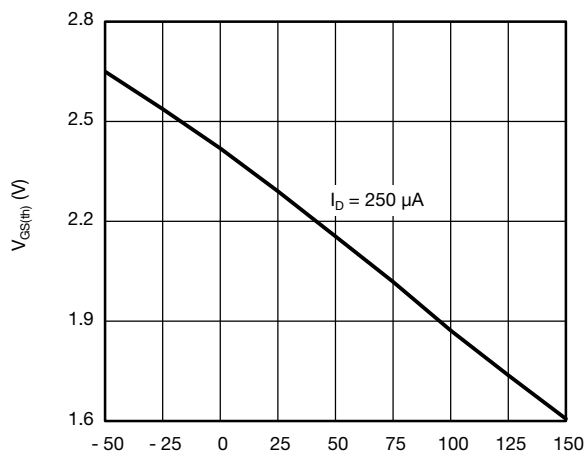
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



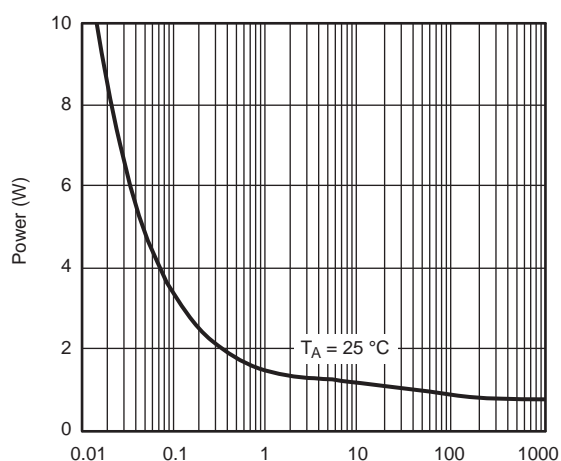
Source-Drain Diode Forward Voltage



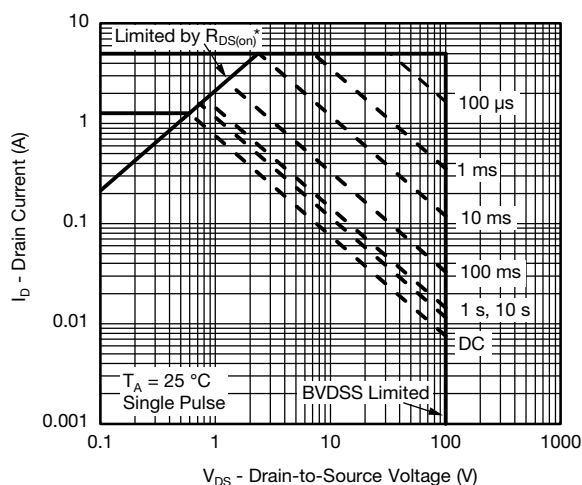
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

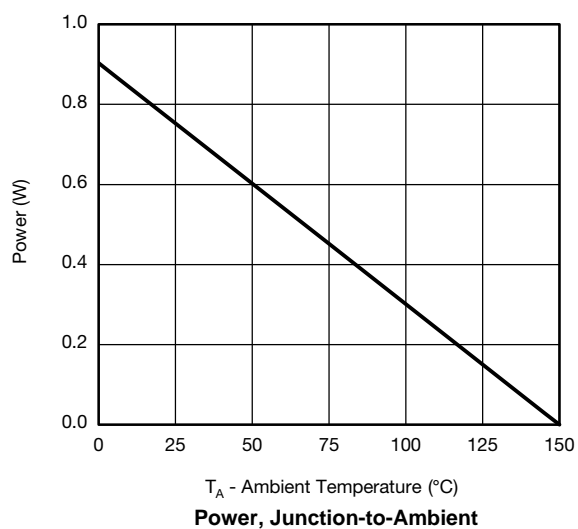
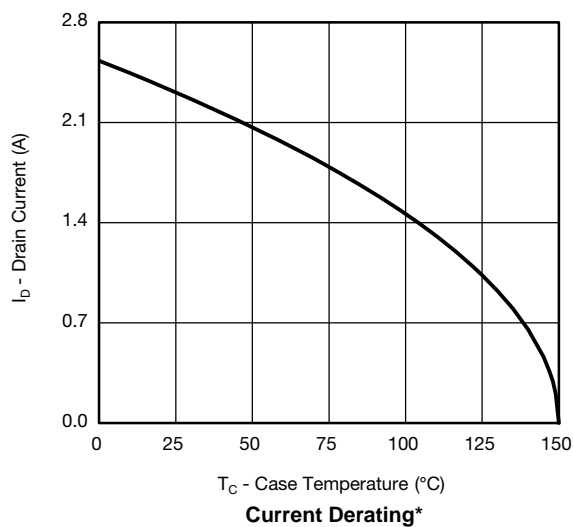


Single Pulse Power

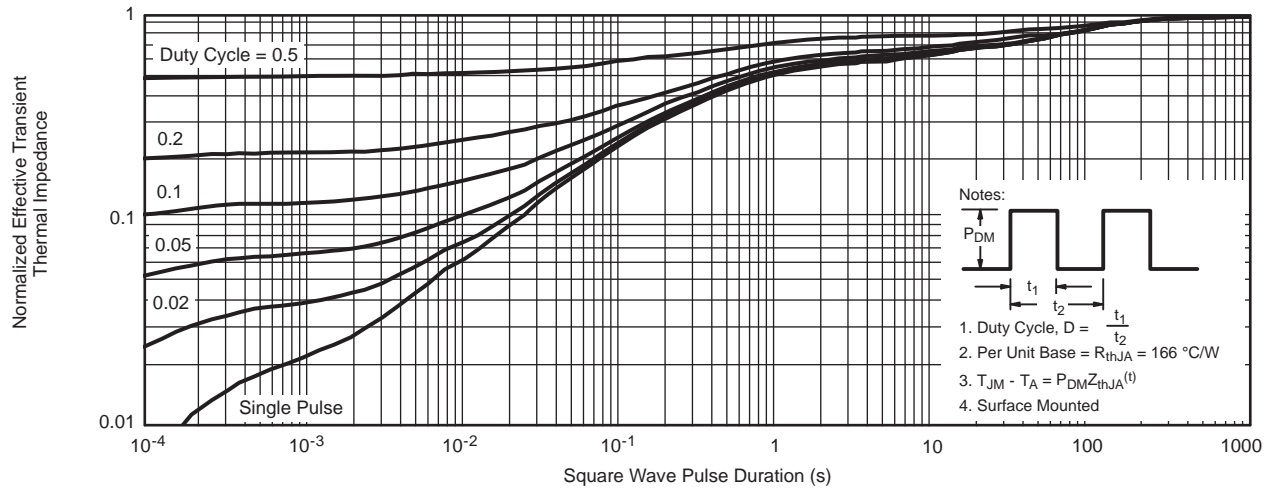
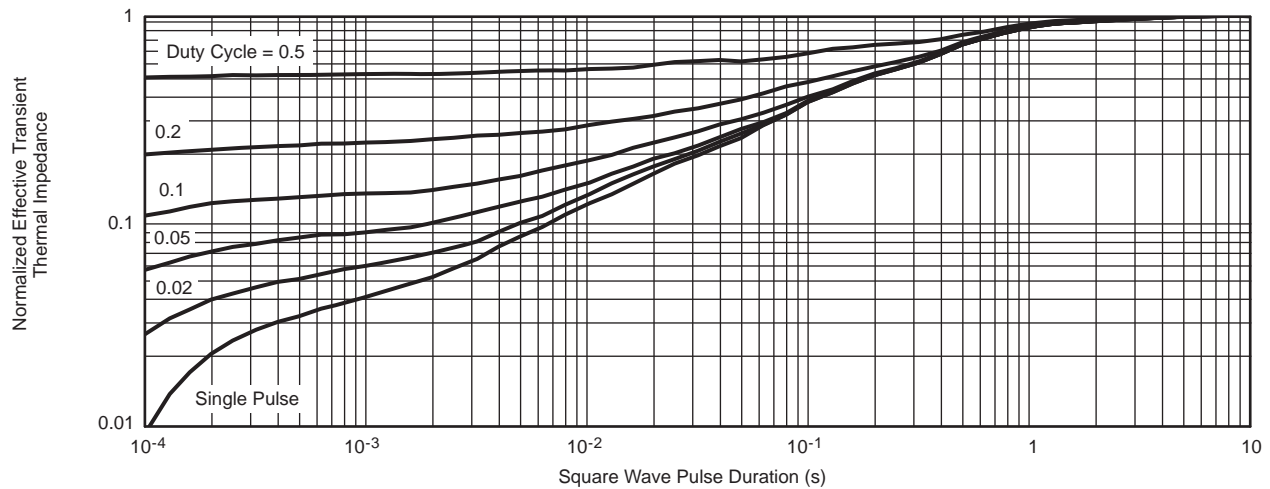


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


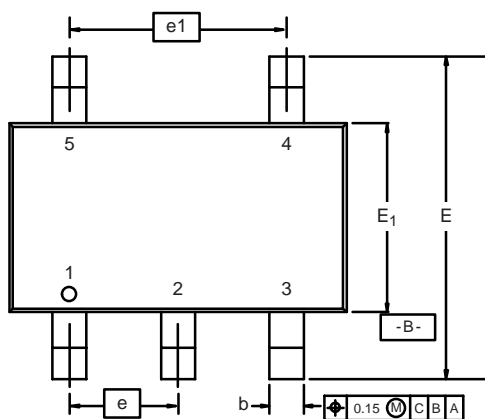
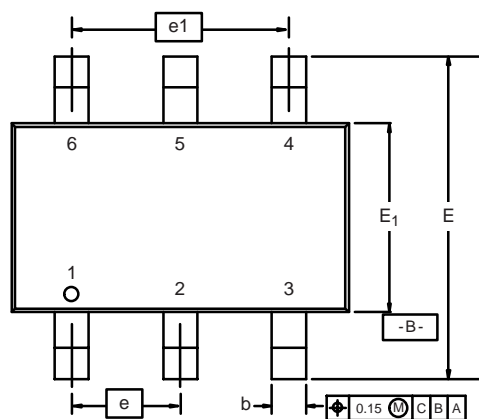
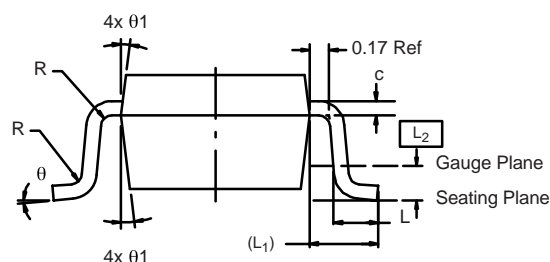
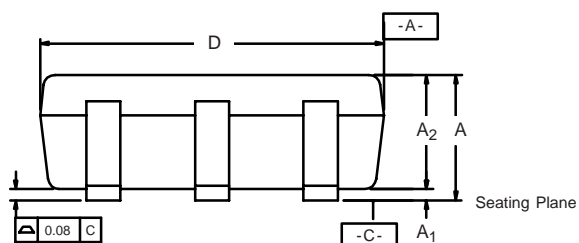
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Foot
Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Foot ($25\text{ }^{\circ}\text{C}$)
- are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

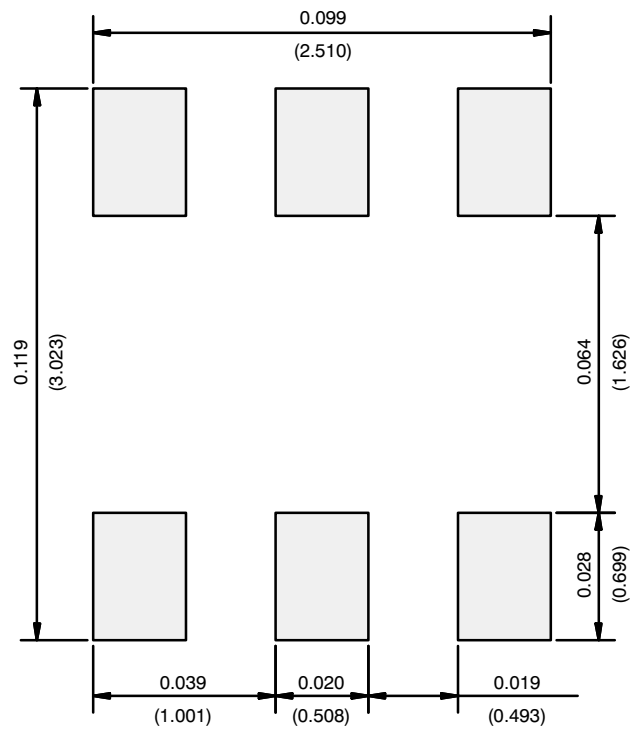
TSOP: 5/6-LEAD

JEDEC Part Number: MO-193C

**5-LEAD TSOP****6-LEAD TSOP**

	MILLIMETERS			INCHES		
Dim	Min	Nom	Max	Min	Nom	Max
A	0.91	-	1.10	0.036	-	0.043
A ₁	0.01	-	0.10	0.0004	-	0.004
A ₂	0.90	-	1.00	0.035	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E ₁	1.55	1.65	1.70	0.061	0.065	0.067
e	0.95 BSC			0.0374 BSC		
e ₁	1.80	1.90	2.00	0.071	0.075	0.079
L	0.32	-	0.50	0.012	-	0.020
L ₁	0.60 Ref			0.024 Ref		
L ₂	0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-
θ	0°	4°	8°	0°	4°	8°
θ ₁	7° Nom			7° Nom		
ECN: C-06593-Rev. I, 18-Dec-06						
DWG: 5540						

RECOMMENDED MINIMUM PADS FOR TSOP-6



Recommended Minimum Pads
Dimensions in Inches/(mm)

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