

CML3055-VB Datasheet

N-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (A) ^a	Q _g (Typ.)		
00	0.076 at V _{GS} = 10 V	4.5	10 nC		
60	0.085 at V _{GS} = 4.5 V	3.5	10110		

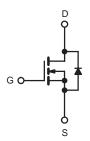
FEATURES

- Halogen-free
- Trench Power MOSFET



APPLICATIONS

· Load Switches for Portable Devices



N-Channel MOSFET

90	T_2	22_2
30	1-24	23-3



Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	60	V	
Gate-Source Voltage		V _{GS}	± 20	V	
	T _C = 25 °C		4.5		
Continuous Drain Current (T _{.I} = 150 °C)	T _C = 70 °C	I _D	3.2 ^a		
Continuous Diam Current (1) = 150 °C)	T _A = 25 °C	'D	2.7		
	T _A = 70 °C		2.3	A	
Pulsed Drain Current		I _{DM}	20		
Continuous Source-Drain Diode Current	T _C = 25 °C	- I _S	3.2		
Continuous Source-Diam Diode Current	T _A = 25 °C	'S	2.1 ^{b, c}		
	T _C = 25 °C		4.0		
Maximum Power Dissipation	T _C = 70 °C	P _D	3.0	w	
Maximum Power Dissipation	T _A = 25 °C	' D	2.5 ^{b, c}	VV	
	T _A = 70 °C		1.6 ^{b, c}		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Tempera		260			

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{a, c, d}	t ≤ 5 s	R _{thJA}	40	50	°C/W	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	15	20	0/11	

- a. Package limited, T_C = 25 °C.
 b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. Maximum under Steady State conditions is 95 °C/W.
- e. See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- f. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.



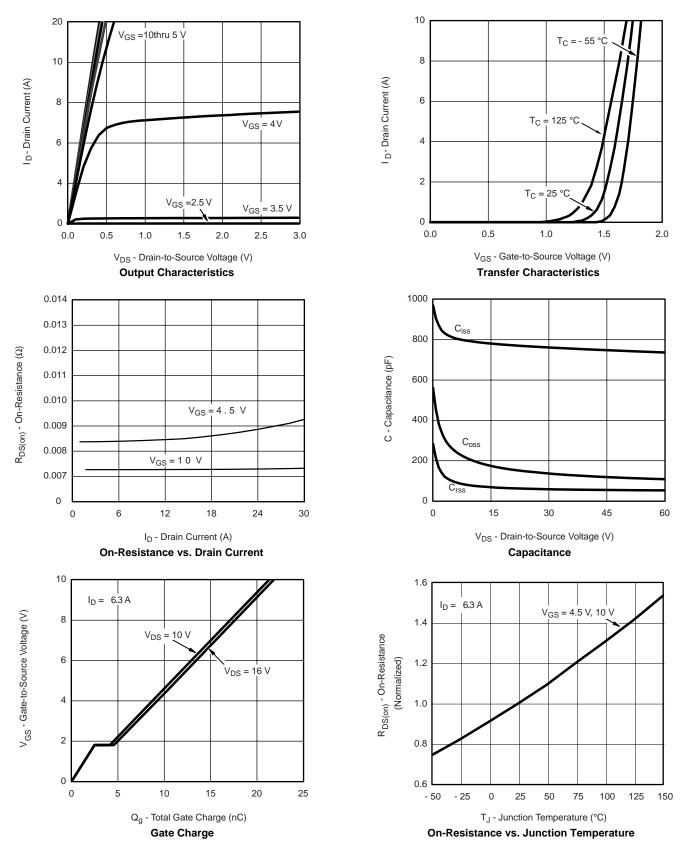
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static	<u> </u>			1		
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	60			V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	L = 250 uA		25		
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_{D} = 250 \mu A$		- 4.0		mV/°C
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	1.0		2.5	V
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 100	nA
Zana Cata Valtana Duain Comunit	1.	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$			1	
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 60 V, V _{GS} = 0 V, T _J = 55 °C			10	μΑ
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	30			Α
_		V _{GS} = 10 V , I _D = 4.0 A		0.076		Ω
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 V$, $I_D = 3.0 A$		0.085		
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 4.0 A		45		S
Dynamic ^b	· · · · ·					I
Input Capacitance	C _{iss}			810		
Output Capacitance	C _{oss}	$V_{DS} = 30V$, $V_{GS} = 0$ V, $f = 1$ MHz		120		pF
Reverse Transfer Capacitance	C _{rss}			100		
Tatal Cata Observe	Qg	V _{DS} = 30 V, V _{GS} = 10 V, I _D = 4.0 A		22	33	nC
Total Gate Charge				10	15	
Gate-Source Charge	Q _{gs}	$V_{DS} = 30 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 3.0 \text{ A}$		2.5		
Gate-Drain Charge	Q_{gd}			1.7		
Gate Resistance	R_g	f = 1 MHz	1 MHz			Ω
Turn-on Delay Time	t _{d(on)}			15	25	
Rise Time	t _r	V_{DD} =30V, , R_L = 1.5 Ω		10	15	
Turn-Off Delay Time	t _{d(off)}	$I_D\cong 4.0$ A, $V_{GEN}=4.5$ V, $R_g=1$ Ω		35	55	
Fall Time	t _f			12	20	
Turn-on Delay Time	t _{d(on)}			10	15	ns
Rise Time	t _r	V_{DD} = 30V , R_L = 1.5 Ω		12	20	1
Turn-Off Delay Time	t _{d(off)}	$I_D\cong 4.0$ A, V_{GEN} = 10 V, R_g = 1 Ω		25	40	
Fall Time	t _f			10	15	1
Drain-Source Body Diode Characteristi	cs					
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			7.2	Α
Pulse Diode Forward Current	I _{SM}				30	^
Body Diode Voltage	V_{SD}	$I_S = 4.0 \text{ A}, V_{GS} = 0 \text{ V}$ 0.8		0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}			20	40	ns
Body Diode Reverse Recovery Charge	Q _{rr}	I _F = 4.0 A, dl/dt = 100 A/µs, T _J = 25 °C		10	20	nC
Reverse Recovery Fall Time	t _a	1 _F = 4.0 Λ, αι/αι = 100 Λ/μ5, 1 _J = 25 C		10		20
Reverse Recovery Rise Time	t _b			10		ns

Notes:

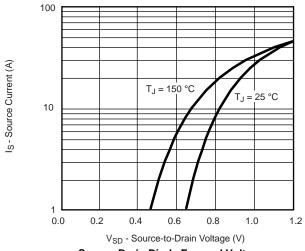
- a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

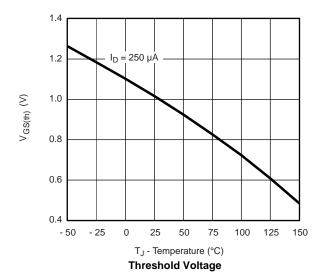


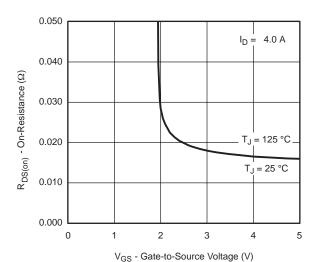




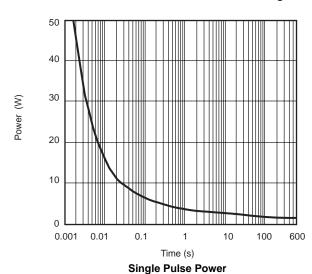


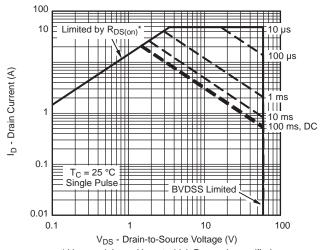
Source-Drain Diode Forward Voltage





On-Resistance vs. Gate-to-Source Voltage

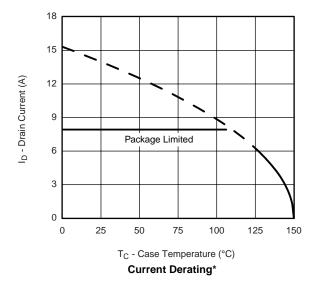


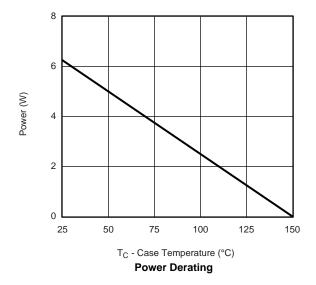


* $V_{\mbox{\footnotesize{GS}}}$ > minimum $V_{\mbox{\footnotesize{GS}}}$ at which $R_{\mbox{\footnotesize{DS(on)}}}$ is specified

Single Pulse Power, Junction-to-Case

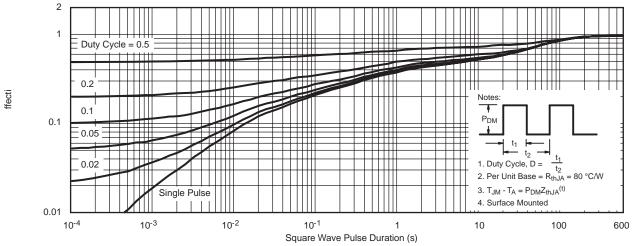




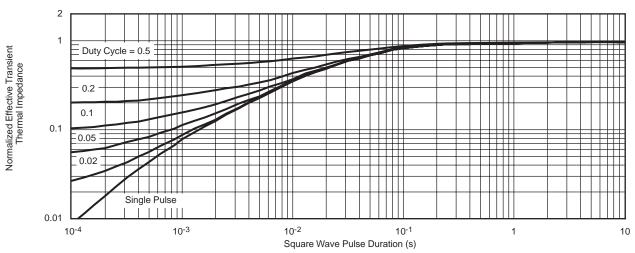


^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





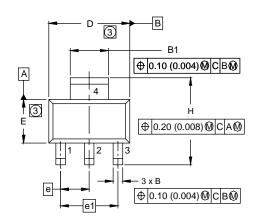
Normalized Thermal Transient Impedance, Junction-to-Ambient

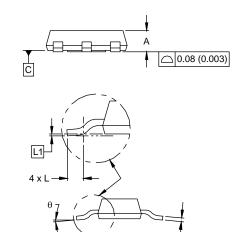


Normalized Thermal Transient Impedance, Junction-to-Foot



SOT-223 (HIGH VOLTAGE)





DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
Α	1.55	1.80	0.061	0.071
В	0.65	0.85	0.026	0.033
B1	2.95	3.15	0.116	0.124
С	0.25	0.35	0.010	0.014
D	6.30	6.70	0.248	0.264
E	3.30	3.70	0.130	0.146
е	2.30 BSC		0.0905 BSC	
e1	4.60 BSC		0.181 BSC	
Н	6.71	7.29	0.264	0.287
L	0.91	-	0.036	-
L1	0.061 BSC		0.0024 BSC	
θ	-	10'	-	10'

ECN: S-82109-Rev. A, 15-Sep-08

DWG: 5969

Notes

- 1. Dimensioning and tolerancing per ASME Y14.5M-1994.
- 2. Dimensions are shown in millimeters (inches).
- 3. Dimension do not include mold flash.
- 4. Outline conforms to JEDEC outline TO-261AA.



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