

## A2N70K-VB Datasheet

### Power MOSFET

#### PRODUCT SUMMARY

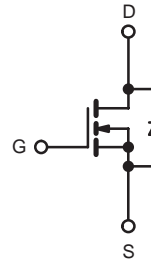
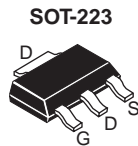
$V_{DS}$ (V)	650	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	8.4
$Q_g$ (Max.) (nC)	18	
$Q_{gs}$ (nC)	3.0	
$Q_{gd}$ (nC)	8.9	
Configuration	Single	

#### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Dynamic  $dV/dt$  Rating
- Repetitive Avalanche Rated
- Available in Tape and Reel
- Fast Switching
- Ease of Paralleling
- Compliant to RoHS Directive 2002/95/EC



Available  
**RoHS\***  
 COMPLIANT  
 HALOGEN  
**FREE**  
 Available



N-Channel MOSFET

#### ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V <sub>DS</sub>	650	V
Gate-Source Voltage			V <sub>GS</sub>	± 20	
Continuous Drain Current	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	I <sub>D</sub>	1.2	A
		T <sub>C</sub> = 100 °C		0.8	
Pulsed Drain Current <sup>a</sup>			I <sub>DM</sub>	4.8	W/°C
Linear Derating Factor				0.33	
Linear Derating Factor (PCB Mount) <sup>e</sup>				0.020	
Single Pulse Avalanche Energy <sup>b</sup>			E <sub>AS</sub>	74	mJ
Repetitive Avalanche Current <sup>a</sup>			I <sub>AR</sub>	2.0	A
Repetitive Avalanche Energy <sup>a</sup>			E <sub>AR</sub>	4.2	mJ
Maximum Power Dissipation	T <sub>C</sub> = 25 °C		P <sub>D</sub>	3	W
Maximum Power Dissipation (PCB Mount) <sup>e</sup>	T <sub>A</sub> = 25 °C			0.02	
Peak Diode Recovery dV/dt <sup>c</sup>			dV/dt	3.0	V/ns
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			260 <sup>d</sup>	

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 37\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 2.0\text{ A}$  (see fig. 12).
- $I_{SD} \leq 2.0\text{ A}$ ,  $dI/dt \leq 40\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).

\* Pb containing terminations are not RoHS compliant, exemptions may apply

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	-	110	°C/W
Maximum Junction-to-Ambient (PCB Mount) <sup>a</sup>	$R_{thJA}$	-	-	50	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	-	3.0	

**Note**

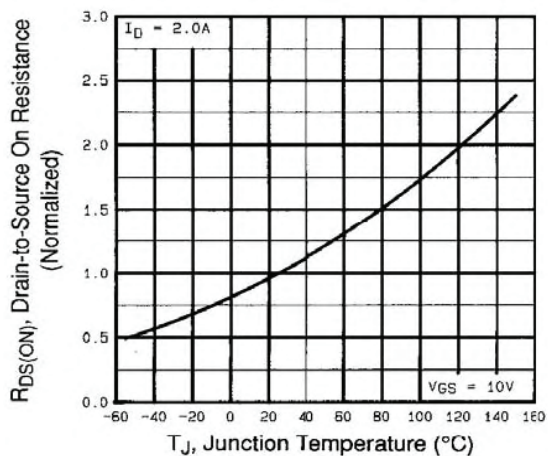
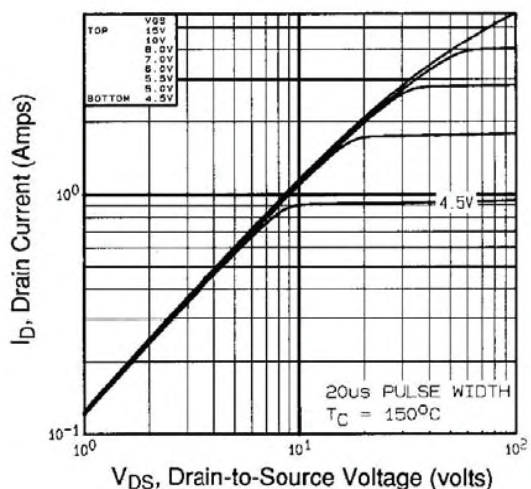
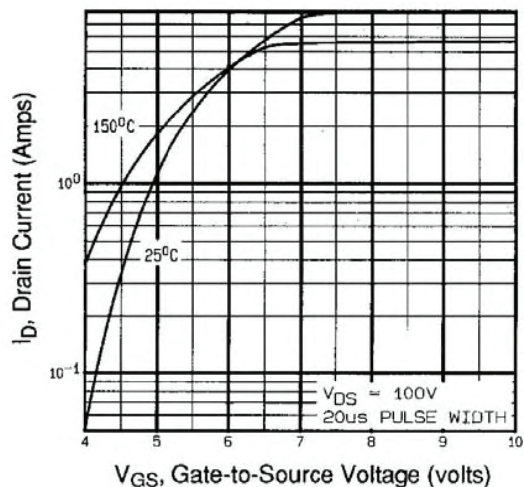
a. When mounted on 1" square PCB (FR-4 or G-10 material).

**SPECIFICATIONS**  $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		650	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.88	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V		-	-	100	μA
		V <sub>DS</sub> = 480 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	500	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 1.2 A <sup>b</sup>	-	8.4	-	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 1.2 A		1.4	-	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = - 25 V, f = 1.0 MHz, see fig. 5		-	350	-	pF
Output Capacitance	C <sub>oss</sub>			-	48	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	8.6	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 2.0 A, V <sub>DS</sub> = 360 V, see fig. 6 and 13 <sup>b</sup>	-	-	18	nC
Gate-Source Charge	Q <sub>gs</sub>			-	-	3.0	
Gate-Drain Charge	Q <sub>gd</sub>			-	-	8.9	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 2.0 A, R <sub>g</sub> = 18 Ω, R <sub>D</sub> = 135 Ω, see fig. 10 <sup>b</sup>		-	10	-	ns
Rise Time	t <sub>r</sub>			-	23	-	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	30	-	
Fall Time	t <sub>f</sub>			-	25	-	
Internal Drain Inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	L <sub>S</sub>			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		-	-	2.0	A
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	8.0	
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 2.0 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	1.6	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 2.0 A, dI/dt = 100 A/μs <sup>b</sup>		-	290	580	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			-	0.67	1.3	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
 b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted


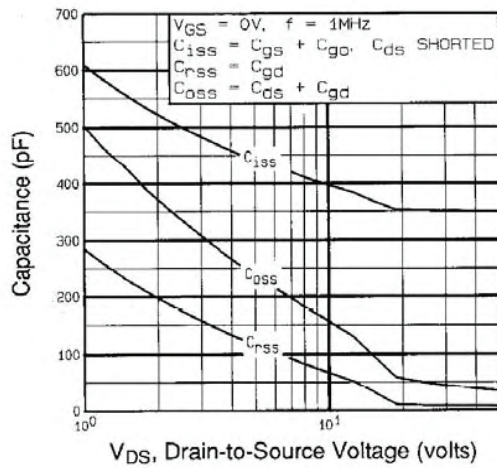


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

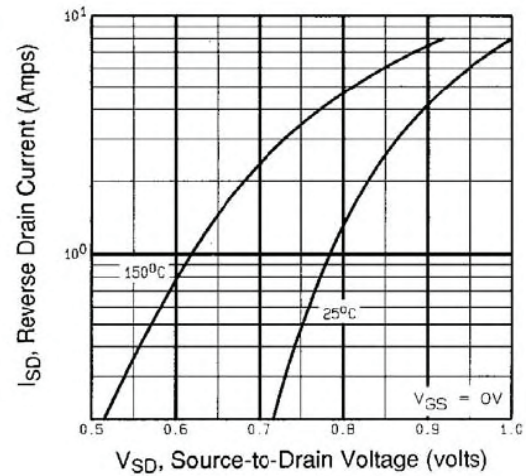


Fig. 7 - Typical Source-Drain Diode Forward Voltage

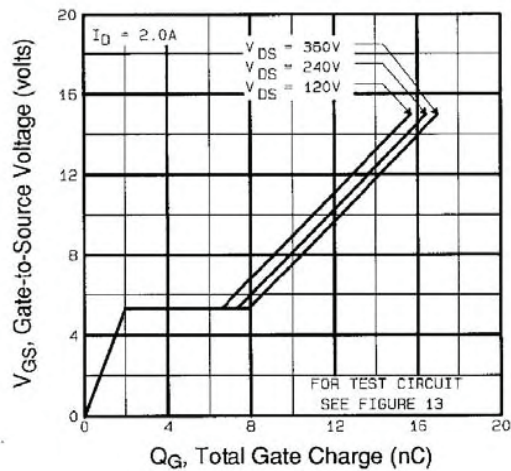


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

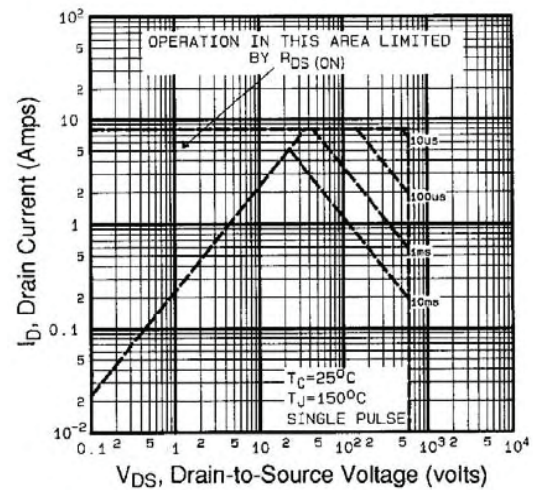


Fig. 8 - Maximum Safe Operating Area

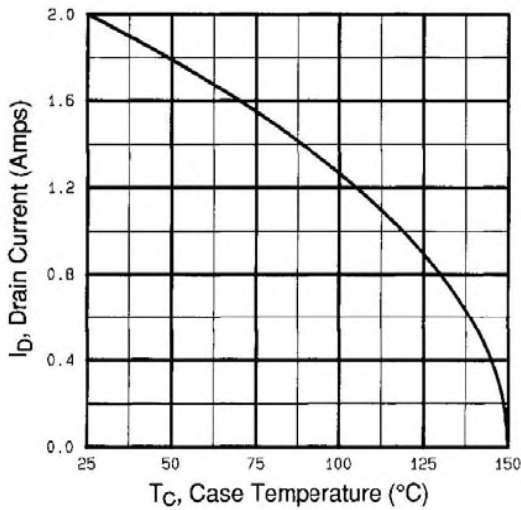


Fig. 9 - Maximum Drain Current vs. Case Temperature

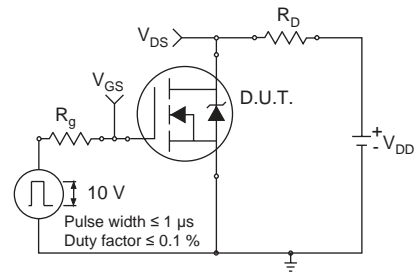


Fig. 10a - Switching Time Test Circuit

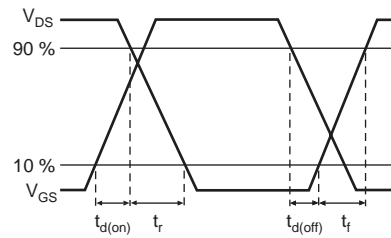


Fig. 10b - Switching Time Waveforms

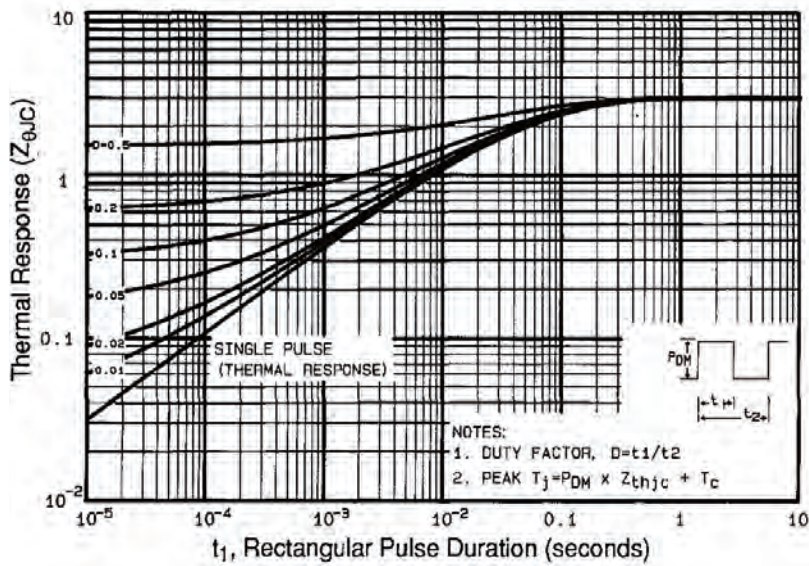


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



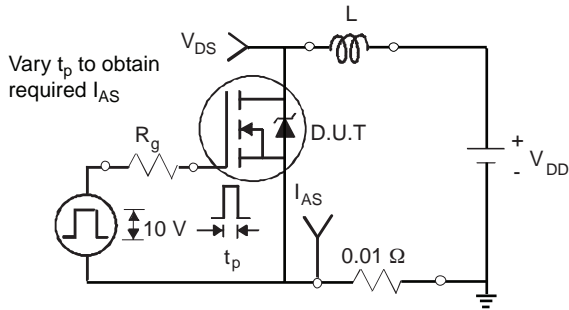


Fig. 12a - Unclamped Inductive Test Circuit

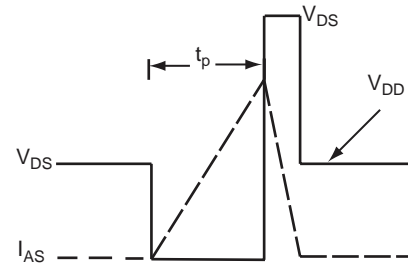


Fig. 12b - Unclamped Inductive Waveforms

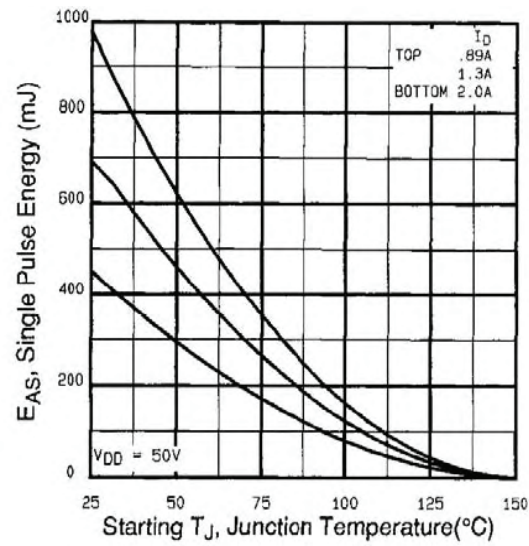


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

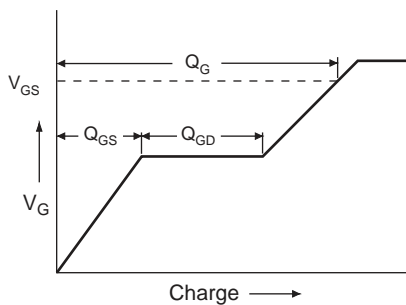


Fig. 13a - Basic Gate Charge Waveform

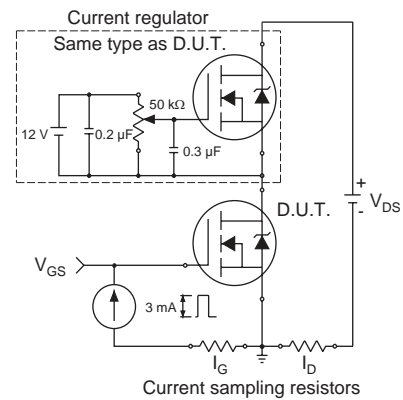
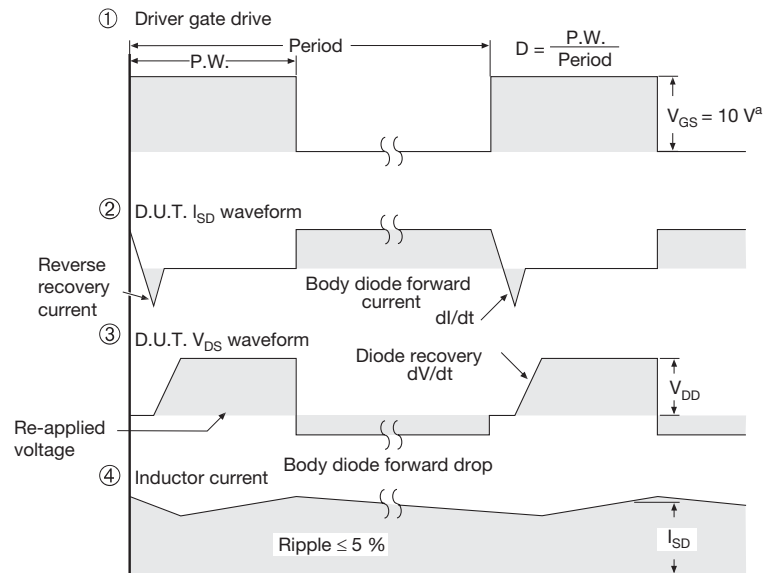
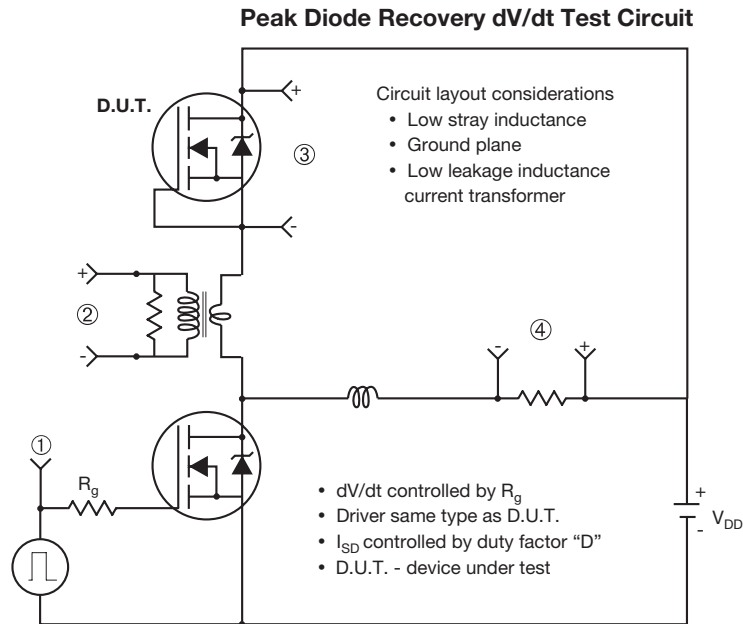


Fig. 13b - Gate Charge Test Circuit

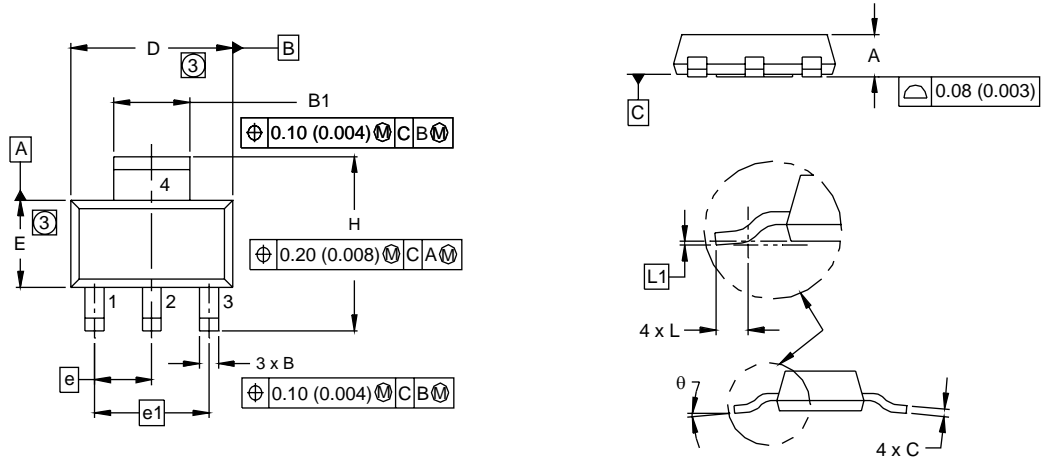


**Note**

a.  $V_{GS} = 5V$  for logic level devices

**Fig. 14 - For N-Channel**

**SOT-223 (HIGH VOLTAGE)**



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.55	1.80	0.061	0.071
B	0.65	0.85	0.026	0.033
B1	2.95	3.15	0.116	0.124
C	0.25	0.35	0.010	0.014
D	6.30	6.70	0.248	0.264
E	3.30	3.70	0.130	0.146
e	2.30 BSC		0.0905 BSC	
e1	4.60 BSC		0.181 BSC	
H	6.71	7.29	0.264	0.287
L	0.91	-	0.036	-
L1	0.061 BSC		0.0024 BSC	
$\theta$	-	10°	-	10°
ECN: S-82109-Rev. A, 15-Sep-08 DWG: 5969				

**Notes**

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension do not include mold flash.
4. Outline conforms to JEDEC outline TO-261AA.



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