

SSG4841P-VB Datasheet

P-Channel 40 V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A) ^a	Q _g (Typ.)			
- 40	0.010 at V _{GS} = - 10 V	- 16.1	33 nC			
- 40	0.014 at V _{GS} = - 4.5 V	- 13.3	33 110			

FEATURES

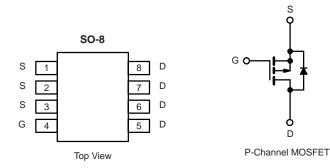
- Halogen-free According to IEC 61249-2-21 Definition
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC



COMPLIANT HALOGEN FREE

APPLICATIONS

- Load Switch
- POL



Parameter	Symbol	Limit	Unit		
Drain-Source Voltage Gate-Source Voltage		V _{DS}	- 40	V	
		V _{GS}	± 20		
	T _C = 25 °C		- 16.1		
Continuous Proin Current /T 150 °C	T _C = 70 °C	1 ,	- 12.9		
Continuous Drain Current (T _J = 150 °C)	T _A = 25 °C	I _D	- 10.2 ^{b, c}		
	T _A = 70 °C		- 8.2 ^{b, c}		
Pulsed Drain Current		I _{DM}	- 50	A	
Continous Source-Drain Diode Current	T _C = 25 °C		- 5.3		
Continous Source-Drain Diode Current	T _A = 25 °C	l _s	- 2.1 ^{b, c}		
Single Pulse Avalanche Current	1 0411	I _{AS}	- 28		
Single Pulse Avalanche Energy	L = 0.1 mH	E _{AS}	39	mJ	
	T _C = 25 °C		6.3		
Mayimum Dawar Dissination	T _C = 70 °C		4	w	
Maximum Power Dissipation	T _A = 25 °C	P _D	2.5 ^{b, c}	VV	
	T _A = 70 °C		1.6 ^{b, c}		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	Typical	Maximum	Unit			
Maximum Junction-to-Ambient ^{b, d}	t ≤ 10 s	R _{thJA}	37	50	°C/W		
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	16	20	C/VV		

Notes:

- a. Based on T_C = 25 °C.
 b. Surface mounted on 1" x 1" FR4 board.
- d. Maximum under steady state conditions is 85 °C/W.



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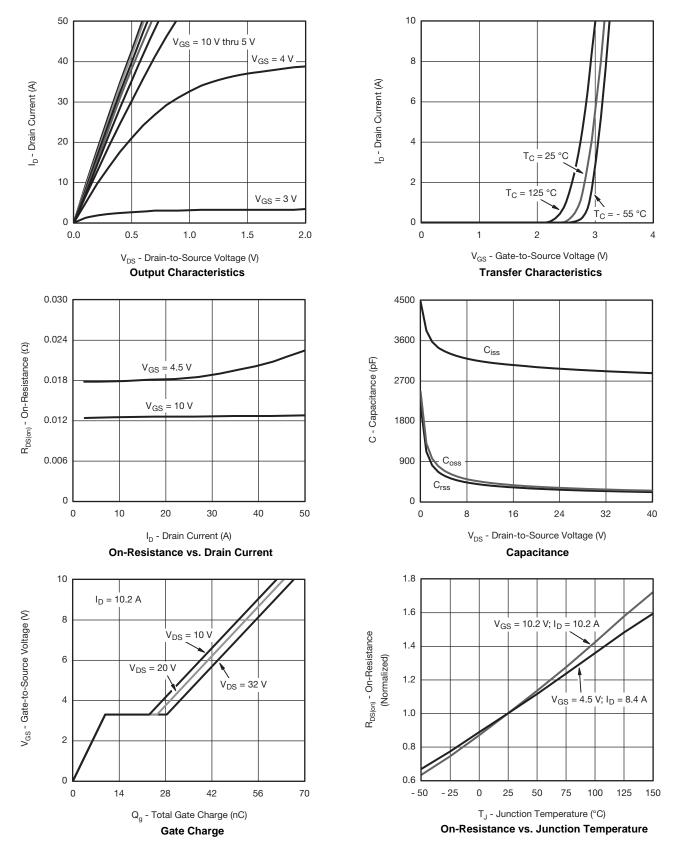
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static	-				L		
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V, } I_D = -250 \mu\text{A}$	- 40			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I - 250 uA		- 36		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_{J}$	I _D = - 250 μA		5			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = -250 \mu A$	- 1.2		- 2.5	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zana Oata Valtana Busis Osumast		V _{DS} = - 40 V, V _{GS} = 0 V			- 1		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 40 V, V _{GS} = 0 V, T _J = 55 °C			- 5	μA	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \le -5 \text{ V}, V_{GS} = -10 \text{ V}$	- 25			Α	
Drain Course On State Desigtance	D	V _{GS} = - 10 V, I _D = - 10.2 A		0.010		Ω	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 8.4 A		0.014			
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 15 V, I _D = - 10.2 A		37		S	
Dynamic ^b	•						
Input Capacitance	C _{iss}			3007		pF	
Output Capacitance	C _{oss}	$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		335			
Reverse Transfer Capacitance	C _{rss}			291			
Total Gate Charge	0	Q_g $V_{DS} = -20 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -10.2 \text{ A}$		64	95	nC	
Total Gate Griange	· ·			33	50		
Gate-Source Charge	Q_{gs}	$V_{DS} = -20 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -10.2 \text{ A}$		9.8			
Gate-Drain Charge	Q_{gd}			15.7			
Gate Resistance	R _g	f = 1 MHz	0.4	2	4	Ω	
Turn-On Delay Time	t _{d(on)}			57	86		
Rise Time	t _r	V_{DD} = - 20 V, R_L = 2.4 Ω		50	75	ns	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong$ - 8.2 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		40	60		
Fall Time	t _f			17	26		
Turn-On Delay Time	t _{d(on)}			13	20		
Rise Time	t _r	V_{DD} = - 20 V, R_L = 2.4 Ω		11	20		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong$ - 8.2 A, V_{GEN} = - 10 V, R_g = 1 Ω		45	68		
Fall Time	t _f			9	18		
Drain-Source Body Diode Characteristi	cs						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			- 5.3	Α	
Pulse Diode Forward Current	I _{SM}				- 50		
Body Diode Voltage	V _{SD}	I _S = -8.2 A, V _{GS} = 0 V		- 0.8	- 1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			36	54	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	I _F = - 8.2 A, dl/dt = 100 A/μs, T _{.I} = 25 °C		41	62	nC	
Reverse Recovery Fall Time	t _a	I _F = - 8.2 A, αl/αl = 100 A/μs, 1 _J = 25 C		20		200	
Reverse Recovery Rise Time	t _b			16	_	ns	

Notes:

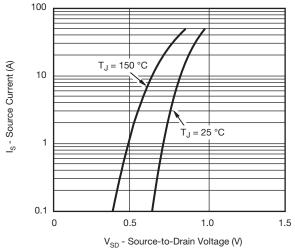
- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

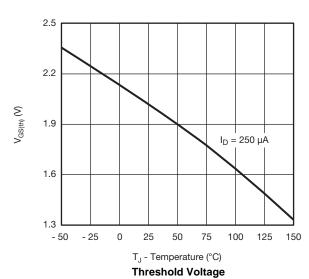






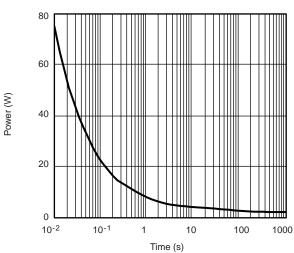




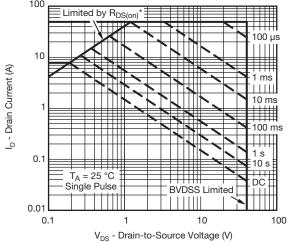


0.05 0.04 0.03 0.02 0.01 $T_{J} = 125 \, ^{\circ}\text{C}$ $T_{J} = 25 \, ^{\circ}\text{C}$ 0.01 V_{GS} - Gate-to-Source Voltage (V)

On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power (Junction-to-Ambient)

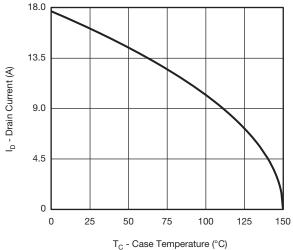


 $^{*}V_{GS}$ > minimum V_{GS} at which $R_{DS(on)}$ is specified

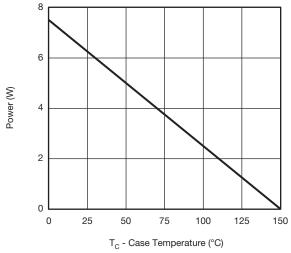
Safe Operating Area, Junction-to-Ambient

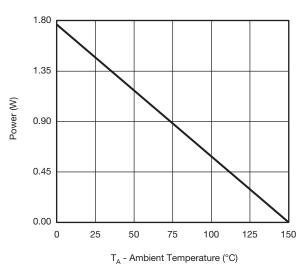
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Current Derating*



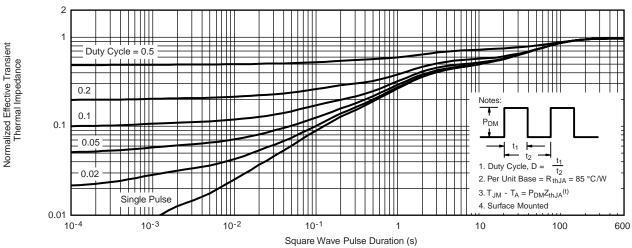


Power, Junction-to-Foot

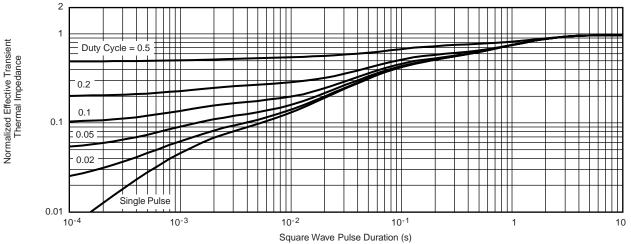
Power, Junction-to-Ambient

 $^{^*}$ The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Ambient

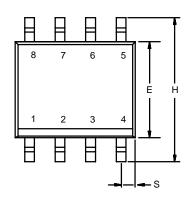


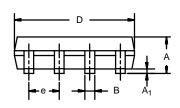
Normalized Thermal Transient Impedance, Junction-to-Foot

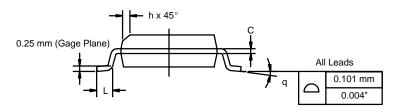
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SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012





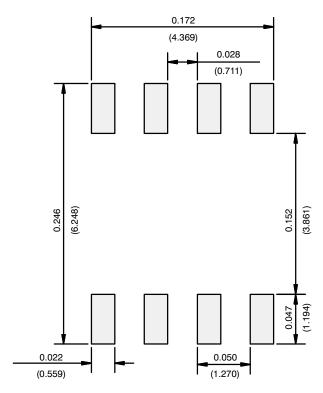


	MILLIMETERS		INC	HES	
DIM	Min	Max	Min	Max	
Α	1.35	1.75	0.053	0.069	
A ₁	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
Е	3.80	4.00	0.150	0.157	
е	1.27 BSC		0.050 BSC		
Н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
FCN: C-06527-Rev 11-Sen-06					

ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)



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