

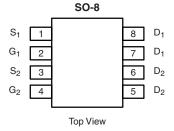
SSF9926-VB Datasheet **Dual N-Channel 20-V (D-S) MOSFET**

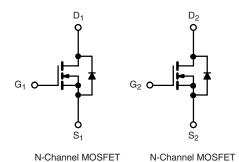
PRODUCT SUMMARY				
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)		
20	0.019 at $V_{GS} = 4.5 \text{ V}$	7.1		
20	0.026 at V _{GS} = 2.5 V	6.0		

FEATURES

- Halogen-free According to IEC 61249-2-21 **Definition**
- Trench Power MOSFET
- 100 % R_g Tested
 Compliant to RoHS Directive 2002/95/EC







Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	20	V	
Gate-Source Voltage		V _{GS}	± 12	V	
Out 1 150 00\3	T _A = 25 °C	. I _D	7.1		
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 70 °C		5.7	1	
Pulsed Drain Current (10 μs Pulse Width)		I _{DM}	40	Α	
Continuous Source Current (Diode Conduction) ^a		I _S	1.7		
Mariana Barra Biratina di	T _A = 25 °C	P _D	2	w	
Maximum Power Dissipation ^a	T _A = 70 °C	'D	1.3	1 w	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Limit	Unit		
Maximum Junction-to-Ambient ^a	R _{thJA}	62.5	°C/W		

a. Surface Mounted on FR4 board, $t \le 10 \text{ s.}$

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SPECIFICATIONS T _J = 25 °C, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	0.6		1.5	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 100	nA	
Zava Cata Valtana Drain Current	,	V _{DS} = 20 V, V _{GS} = 0 V		1			
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			5	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	20			Α	
	В	$V_{GS} = 4.5 \text{ V}, I_D = 7.1 \text{ A}$		0.019			
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 2.5 V, I _D = 6.0 A		0.026		Ω	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 10 V, I _D = 7.1 A		27		S	
Diode Forward Voltage ^a	V_{SD}	I _S = 1.7 A, V _{GS} = 0 V			1.2	V	
Dynamic ^b							
Total Gate Charge	Q_g			9.5			
Gate-Source Charge	Q_{gs}	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 7.1 \text{ A}$		1.5		nC	
Gate-Drain Charge	Q_{gd}			2.5			
Gate Resistance	R_{g}	f = 1 MHz		1.6	2.7	Ω	
Turn-On Delay Time	t _{d(on)}			10			
Rise Time	t _r	V_{DD} = 10 V, R_L = 10 Ω		15			
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 1 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 10 \Omega$		38		ns	
Fall Time	t _f			25			
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 1.7 A, dI/dt = 100 A/μs		26			

Notes:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

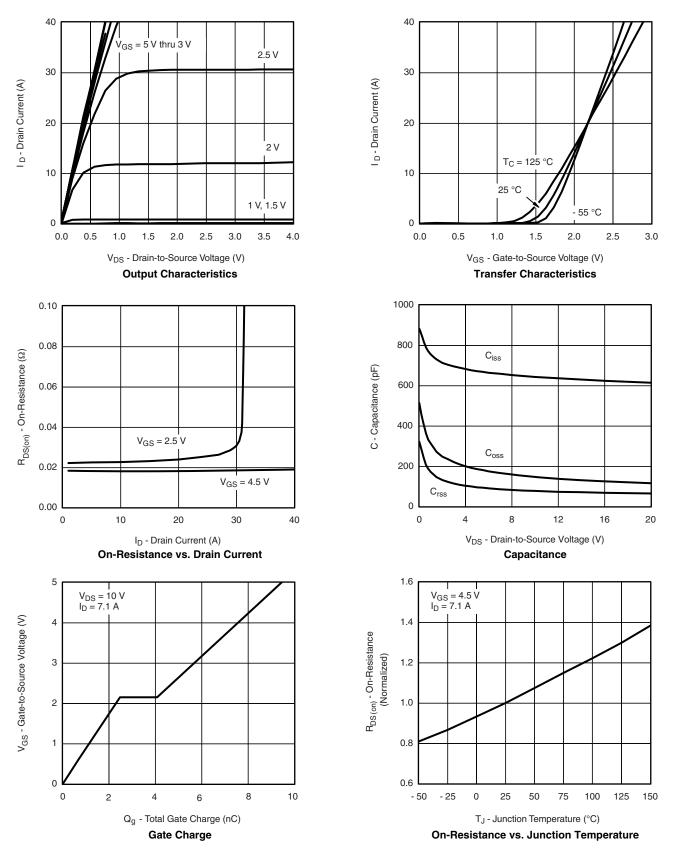
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a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

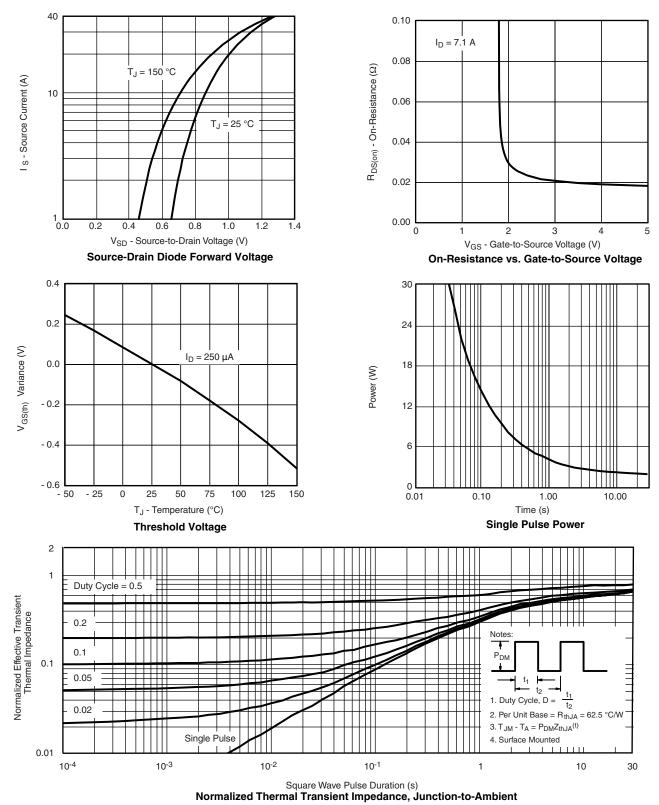


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





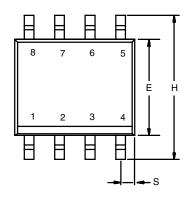
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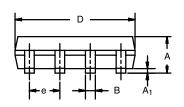


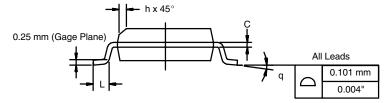
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SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







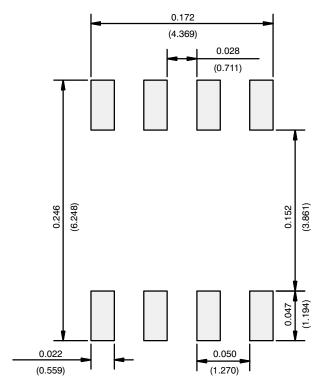
	MILLIM	IETERS	INCHES		
DIM	Min	Max	Min	Max	
Α	1.35	1.75	0.053	0.069	
A ₁	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
Е	3.80	4.00	0.150	0.157	
е	1.27 BSC		0.050 BSC		
Н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
ECN: C-06527-Rev. J. 11-Sep-06					

DWG: 5498

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RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)

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