

## SI9424ADY-T1-E3-VB Datasheet P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}$ ( $\Omega$ )	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)		
	$0.015$ at $V_{GS} = -4.5 \text{ V}$	- 13 <sup>a</sup>			
- 20	$0.021$ at $V_{GS} = -2.5 \text{ V}$	- 10 <sup>a</sup>	20 nC		
	0.040 at V <sub>GS</sub> = - 1.8 V	- 8			

#### **FEATURES**

- Halogen-free According to IEC 61249-2-21 Definition

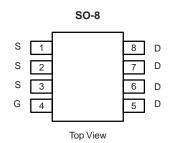
- Trench Power MOSFET 100 %  $R_{\rm g}$  Tested Compliant to RoHS Directive 2002/95/EC

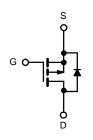


**FREE** 



- Portable Devices
- Load Switch
- Battery Switch
- Charger Switch





P-Channel MOSFET

Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	$V_{DS}$	- 20	V		
Gate-Source Voltage	$V_{GS}$	± 12			
Continuous Drain Current (T <sub>J</sub> = 150 °C)	$T_{C} = 25 ^{\circ}\text{C}$ $T_{C} = 70 ^{\circ}\text{C}$ $T_{A} = 25 ^{\circ}\text{C}$ $T_{A} = 70 ^{\circ}\text{C}$	I <sub>D</sub>	- 13 <sup>a</sup> - 10 <sup>a</sup> - 8 <sup>b, c</sup> - 7.1 <sup>b, c</sup>	A	
Pulsed Drain Current	I <sub>DM</sub>	- 50			
Continuous Source-Drain Diode Current	$T_C = 25 ^{\circ}\text{C}$ $T_A = 25 ^{\circ}\text{C}$	I <sub>S</sub>	- 6 <sup>a</sup> - 2.9 <sup>b, c</sup>		
Maximum Power Dissipation	$T_{C} = 25 ^{\circ}\text{C}$ $T_{C} = 70 ^{\circ}\text{C}$ $T_{A} = 25 ^{\circ}\text{C}$ $T_{A} = 70 ^{\circ}\text{C}$	P <sub>D</sub>	19 12 3.5 <sup>b, c</sup> 2.2 <sup>b, c</sup>	w	
Operating Junction and Storage Temperature Ra	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C		
Soldering Recommendations (Peak Temperature		260			

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>b, e</sup>	t ≤ 5 s	R <sub>thJA</sub>	28	36	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	$R_{thJC}$	5.3	6.5	O/ VV	

#### Notes:

- a. Package limited.
- b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 5 s.
- d. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- e. Maximum under Steady State conditions is 80 °C/W.

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static				•	l .	l .	
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	- 20			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = - 250 μA		- 12		mV/°C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	i <sub>D</sub> = - 250 μA		3			
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = -250 \mu\text{A}$	- 0.5		- 1.2	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 20	± 20	
		$V_{DS} = 0 \text{ V}, V_{GS} = \pm 4.5 \text{ V}$			± 0.5	^	
Zero Gate Voltage Drain Current		$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}$			- 1	μΑ	
Zero Gate voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 \text{ °C}$			- 10		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \le -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	- 20			Α	
		V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 5.6 A		0.015		Ω	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 2.5 V, I <sub>D</sub> = - 5.3 A		0.021			
		V <sub>GS</sub> = - 1.8 V, I <sub>D</sub> = - 2.5 A		0.040			
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = - 10 V, I <sub>D</sub> = - 5.6 A		35		S	
Dynamic <sup>b</sup>				•	l .		
Total Gate Charge	0	V <sub>DS</sub> = - 10 V, V <sub>GS</sub> = - 8 V, I <sub>D</sub> = - 5 A		50	75		
Cata Causa Chausa	$Q_g$			20	30	nC	
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -5 \text{ A}$		3.3			
Gate-Drain Charge	$Q_{gd}$			8.4			
Gate Resistance	$R_g$	f = 1 MHz	0.2	1	2	kΩ	
Turn-On Delay Time	t <sub>d(on)</sub>			0.71	1.1		
Rise Time	t <sub>r</sub>	$V_{DD} = -10 \text{ V}, R_L = 1 \Omega$		1.7	2.6		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong -5 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_g = 1$		6	9		
Fall Time	t <sub>f</sub>	Ω		3.2	5	l	
Turn-On Delay Time	t <sub>d(on)</sub>			0.3	0.45	us	
Rise Time	t <sub>r</sub>	$V_{DD}$ = - 10 V, $R_L$ = 1 $\Omega$		0.6	0.9		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong -5 \text{ A}, V_{GEN} = -10 \text{ V}, R_g = 1$		10	15		
Fall Time	t <sub>f</sub>	Ω		3.5	5.5		
<b>Drain-Source Body Diode Characterist</b>	ics						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			- 6	Α	
Pulse Diode Forward Current	I <sub>SM</sub>				- 50		
Body Diode Voltage	$V_{SD}$	I <sub>S</sub> = - 5 A, V <sub>GS</sub> = 0 V		- 0.85	- 1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			30	60	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> = 6 A, dI/dt = 100 A/μs, T <sub>.1</sub> = 25 °C		20	40	nC	
Reverse Recovery Fall Time	t <sub>a</sub>	$_{iF}$ – 0 A, divut = 100 A/ $\mu$ s, $_{ij}$ = 25 $^{\circ}$ C		13		ne	
Reverse Recovery Rise Time	t <sub>b</sub>			17		ns	

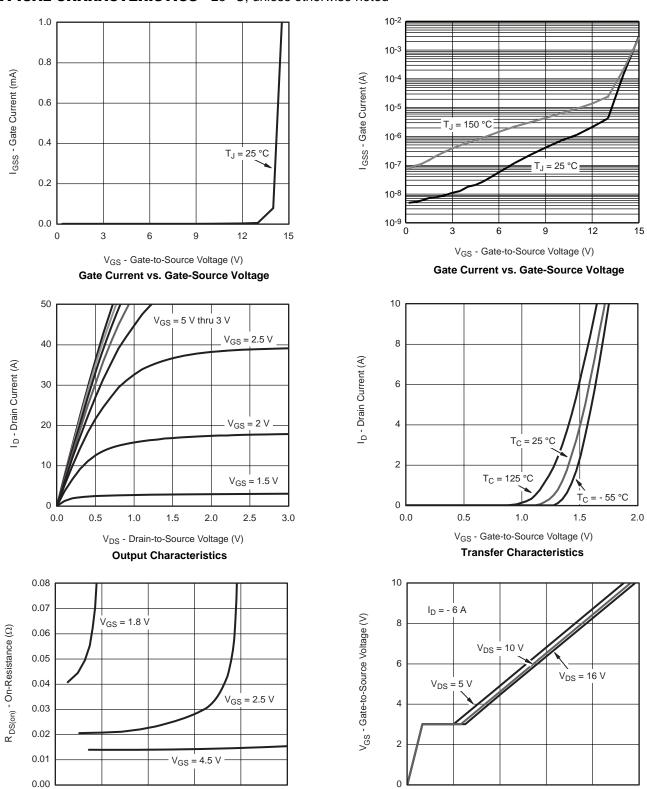
#### Notes:

- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$  b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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10

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Q<sub>q</sub> - Total Gate Charge (nC)

**Gate Charge** 

0

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0

10

30

I<sub>D</sub> - Drain Current (A)

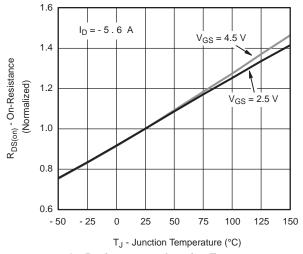
On-Resistance vs. Drain Current

40

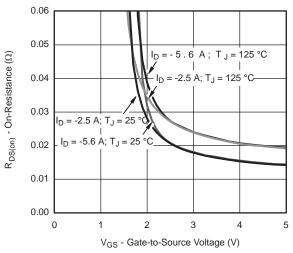
50

50

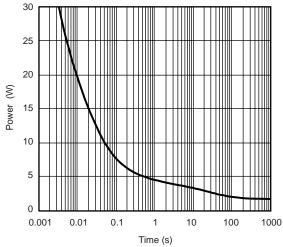




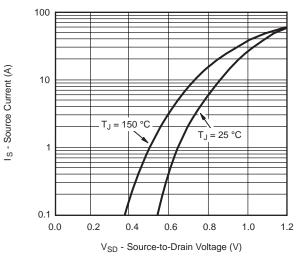
#### On-Resistance vs. Junction Temperature



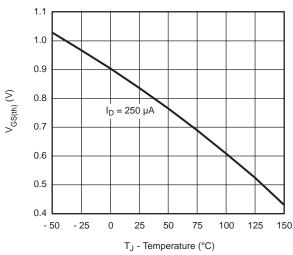
On-Resistance vs. Gate-to-Source Voltage



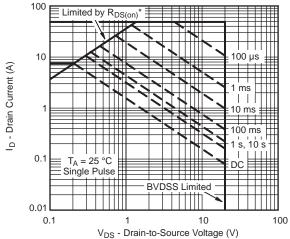
Single Pulse Power, Junction-to-Ambient



#### Soure-Drain Diode Forward Voltage



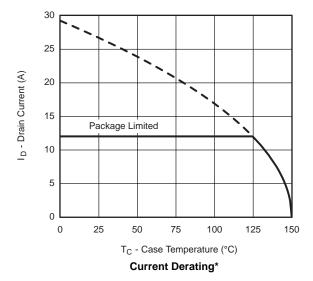
#### Threshold Voltage

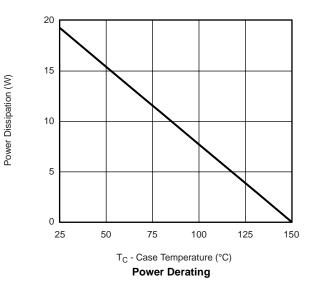


\* V<sub>GS</sub> > minimum V<sub>GS</sub> at which R<sub>DS(on)</sub> is specified

Safe Operating Area, Junction-to-Ambient



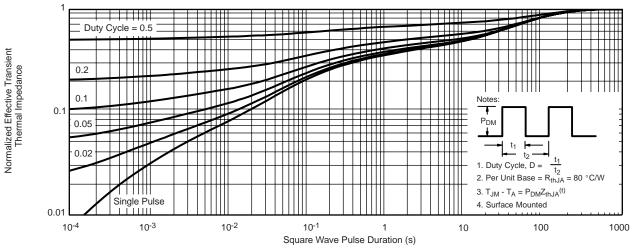




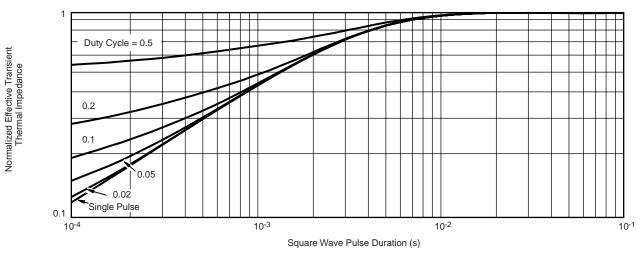
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<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case



**SOIC (NARROW): 8-LEAD**JEDEC Part Number: MS-012







	MILLIM	IETERS	INC	HES	
DIM	Min	Max	Min	Max	
Α	1.35	1.75	0.053	0.069	
A <sub>1</sub>	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
E	3.80	4.00	0.150	0.157	
е	1.27 BSC		0.050 BSC		
Н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
FCN: C-06527-Rev I 11-Sen-06					

ECN: C-06527-Rev. I, 11-Sep-06

DWG: 5498

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#### **RECOMMENDED MINIMUM PADS FOR SO-8**



Recommended Minimum Pads Dimensions in Inches/(mm)



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