

SH8M41TB-VB Datasheet

N-and P-Channel 80-V (D-S) MOSFET

PRODUCT SUMMARY

	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
N-Channel	80	0.046 at V _{GS} = 10 V	5.3	6 nC
		0.059 at V _{GS} = 4.5 V	4.7	
P-Channel	- 80	0.100 at V _{GS} = - 10 V	- 3.9	8 nC
		0.126 at V _{GS} = - 4.5 V	- 3.5	

FEATURES

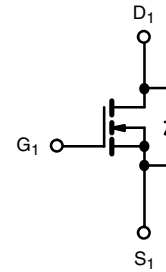
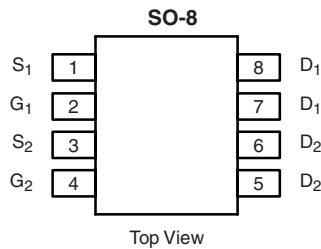
- Halogen-free According to IEC 61249-2-21 Available
- Trench Power MOSFET
- 100 % R_g and UIS Tested

APPLICATIONS

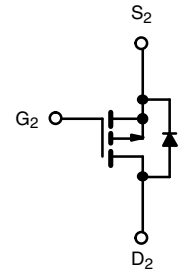
- CCFL Inverter



RoHS
COMPLIANT
HALOGEN
FREE
Available



N-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V _{DS}	60	- 60	V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	I _D	5.3	- 3.9	A
	T _C = 70 °C		4.3	- 3.2	
	T _A = 25 °C		4.3 ^{b, c}	- 3.0 ^{b, c}	
	T _A = 70 °C		3.4 ^{b, c}	- 2.4 ^{b, c}	
Pulsed Drain Current (10 μs Pulse Width)		I _{DM}	20	- 25	
Source Drain Current Diode Current	T _C = 25 °C	I _S	2.6	- 2.8	
	T _A = 25 °C		1.7 ^{b, c}	- 1.7 ^{b, c}	
Pulsed Source-Drain Current		I _{SM}	20	- 25	
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	11	15	mJ
Single Pulse Avalanche Energy		E _{AS}	6.1	11	
Maximum Power Dissipation	T _C = 25 °C	P _D	3.1	3.4	W
	T _C = 70 °C		2	2.2	
	T _A = 25 °C		2 ^{b, c}	2 ^{b, c}	
	T _A = 70 °C		1.3 ^{b, c}	1.3 ^{b, c}	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS

Parameter		Symbol	N-Channel		P-Channel		Unit
			Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient ^{b, d}	t ≤ 10 s	R _{thJA}	55	62.5	53	62.5	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	33	40	30	37	

Notes:

a. Based on T_C = 25 °C.

b. Surface Mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. Maximum under Steady State conditions is 110 °C/W for N-Channel and P-Channel.

SPECIFICATIONS T _J = 25 °C, unless otherwise noted								
Parameter	Symbol	Test Conditions		Min.	Typ. ^a	Max.	Unit	
Static								
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	N-Ch	60			V	
		V _{GS} = 0 V, I _D = - 250 μA	P-Ch	- 60				
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA	N-Ch		55		mV	
		I _D = - 250 μA	P-Ch		- 50			
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	N-Ch		- 6			
		I _D = - 250 μA	P-Ch		4			
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	1		3	V	
		V _{DS} = V _{GS} , I _D = - 250 μA	P-Ch	- 1		- 3		
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	N-Ch P-Ch			100 - 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V	N-Ch			1	μA	
		V _{DS} = - 60 V, V _{GS} = 0 V	P-Ch			- 1		
		V _{DS} = 60 V, V _{GS} = 0 V, T _J = 55 °C	N-Ch			10		
		V _{DS} = - 60 V, V _{GS} = 0 V, T _J = 55 °C	P-Ch			- 10		
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	N-Ch	20			A	
		V _{DS} ≤ - 5 V, V _{GS} = - 10 V	P-Ch	- 25				
Drain-Source On-State Resistance ^b	R _{DS(on)}	V _{GS} = 10 V, I _D = 4.3 A	N-Ch		0.046		Ω	
		V _{GS} = - 10 V, I _D = - 3.1 A	P-Ch		0.100			
		V _{GS} = 4.5 V, I _D = 3.9 A	N-Ch		0.059			
		V _{GS} = - 4.5 V, I _D = - 0.2 A	P-Ch		0.126			
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 4.3 A	N-Ch		15		S	
		V _{DS} = - 15 V, I _D = - 3.1 A	P-Ch		8.5			
Dynamic ^a								
Input Capacitance	C _{iss}	N-Channel V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	N-Ch P-Ch		665 650		pF	
Output Capacitance	C _{oss}		N-Ch P-Ch		75 95			
Reverse Transfer Capacitance	C _{rss}	P-Channel V _{DS} = - 15 V, V _{GS} = 0 V, f = 1 MHz	N-Ch P-Ch		40 60			
Total Gate Charge	Q _g	V _{DS} = 30 V, V _{GS} = 10 V, I _D = 4.3 A	N-Ch		13	20	nC	
		V _{DS} = - 30 V, V _{GS} = - 10 V, I _D = - 3.1 A	P-Ch		14.5	22		
Gate-Source Charge	Q _{gs}	N-Channel V _{DS} = 30 V, V _{GS} = 4.5 V, I _D = 4.3 A	N-Ch P-Ch		6 8	9 12		
			N-Ch P-Ch		2.3 2.2			
Gate-Drain Charge	Q _{gd}	P-Channel V _{DS} = - 30 V, V _{GS} = - 4.5 V, I _D = - 3.1 A	N-Ch P-Ch		2.6 3.7			
Gate Resistance	R _g	f = 1 MHz	N-Ch P-Ch		2 14	3 20		Ω

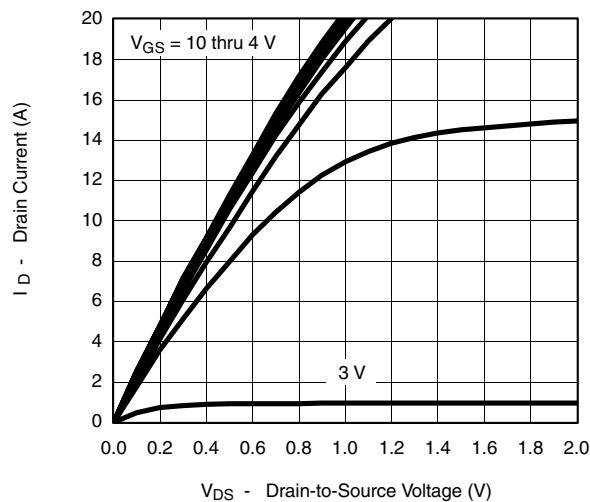
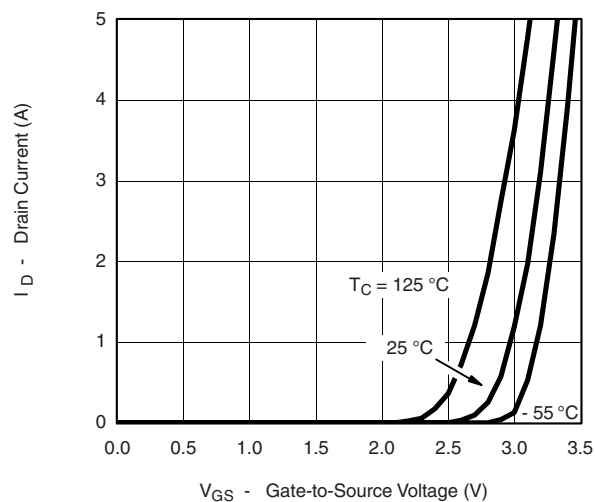
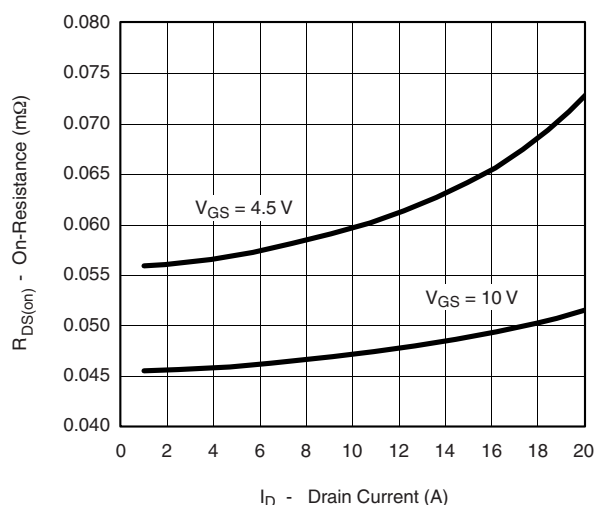
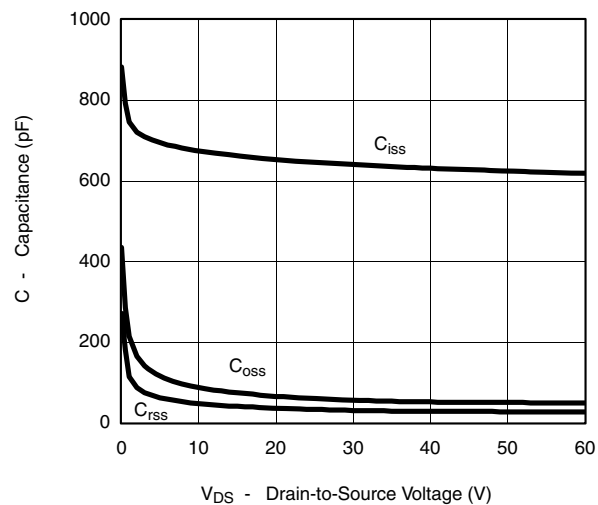
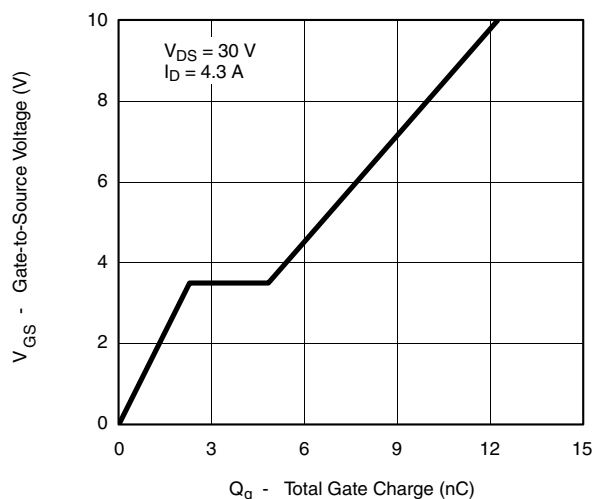
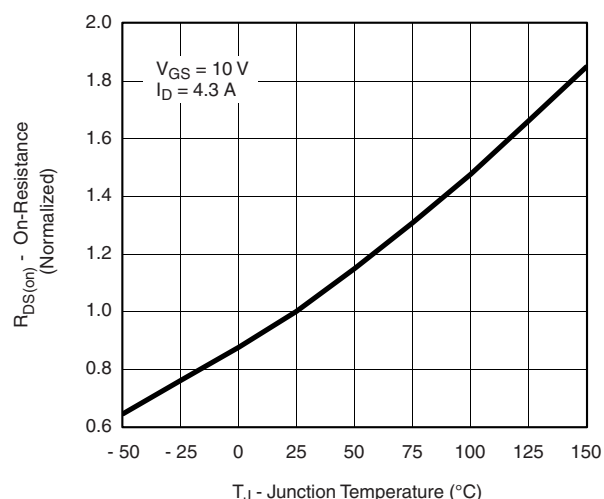
SPECIFICATIONS T _J = 25 °C, unless otherwise noted								
Parameter	Symbol	Test Conditions		Min.	Typ. ^a	Max.	Unit	
Dynamic ^a								
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 30 V, R _L = 8.8 Ω I _D ≅ 3.4 A, V _{GEN} = 4.5 V, R _g = 1 Ω	N-Ch		15	25	ns	
			P-Ch		30	45		
Rise Time	t _r		N-Ch		65	100		
			P-Ch		70	105		
Turn-Off Delay Time	t _{d(off)}	P-Channel V _{DD} = - 30 V, R _L = 12.5 Ω I _D ≅ - 2.4 A, V _{GEN} = - 4.5 V, R _g = 1 Ω	N-Ch		15	25		
			P-Ch		40	60		
Fall Time	t _f		N-Ch		10	15		
			P-Ch		30	45		
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 30 V, R _L = 8.8 Ω I _D ≅ 3.4 A, V _{GEN} = 10 V, R _g = 1 Ω	N-Ch		10	15		
			P-Ch		10	15		
Rise Time	t _r		N-Ch		15	25		
			P-Ch		13	20		
Turn-Off Delay Time	t _{d(off)}	P-Channel V _{DD} = - 30 V, R _L = 12.5 Ω I _D ≅ - 2.4 A, V _{GEN} = - 10 V, R _g = 1 Ω	N-Ch		20	30		
			P-Ch		35	55		
Fall Time	t _f		N-Ch		10	15		
			P-Ch		30	45		
Drain-Source Body Diode Characteristics								
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	N-Ch			2.6	A	
			P-Ch			- 2.8		
Pulse Diode Forward Current ^a	I _{SM}		N-Ch			20		
			P-Ch			- 25		
Body Diode Voltage	V _{SD}	I _S = 1.7 A	N-Ch		0.8	1.2	V	
		I _S = - 2 A	P-Ch		- 0.8	- 1.2		
Body Diode Reverse Recovery Time	t _{rr}	N-Channel I _F = 1.7 A, dI/dt = 100 A/μs, T _J = 25 °C	N-Ch		30	60	ns	
			P-Ch		30	50		
Body Diode Reverse Recovery Charge	Q _{rr}		P-Channel I _F = - 2 A, dI/dt = - 100 A/μs, T _J = 25 °C	N-Ch		32	50	nC
				P-Ch		35	60	
Reverse Recovery Fall Time	t _a			N-Ch		25		ns
				P-Ch		16		
Reverse Recovery Rise Time	t _b		N-Ch		5			
			P-Ch		14			

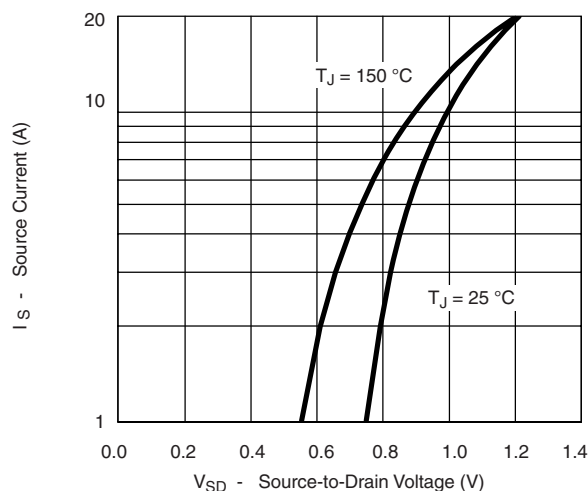
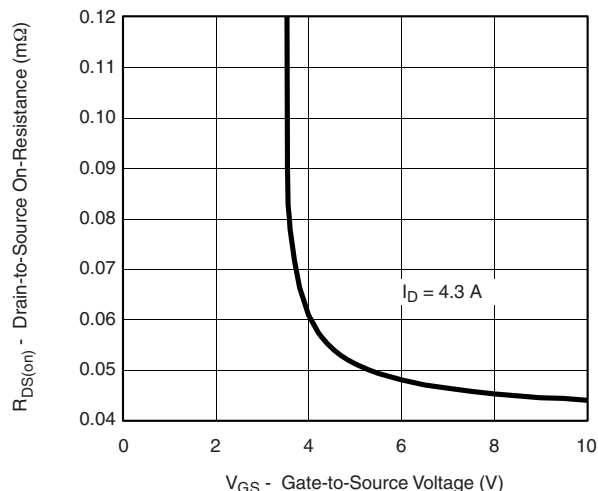
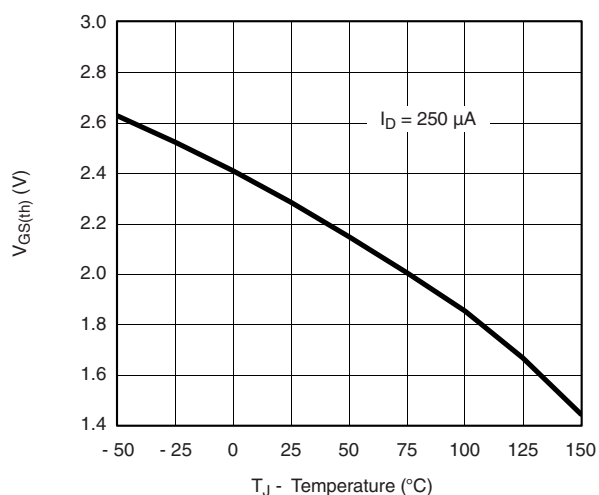
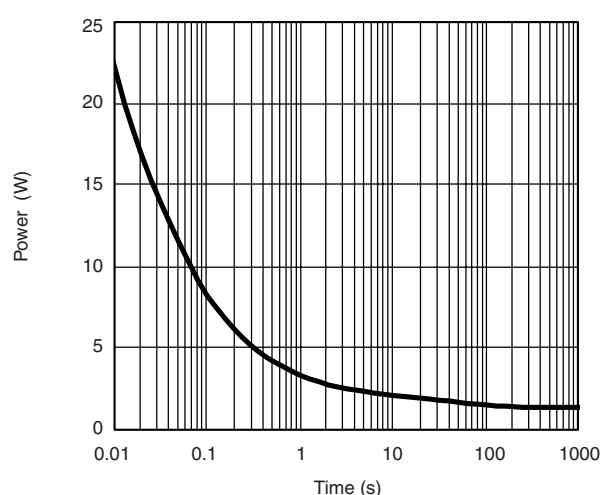
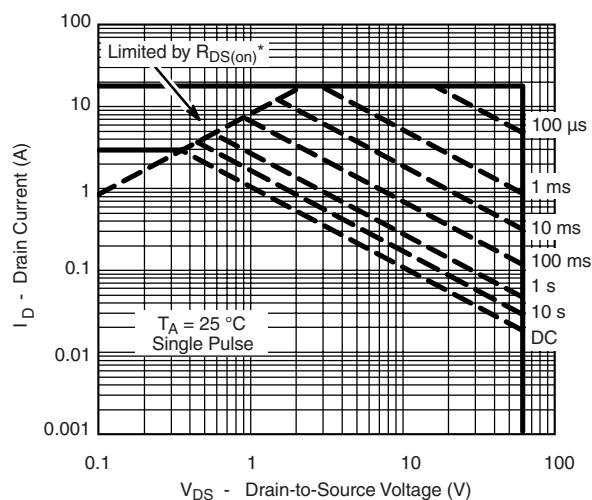
Notes:

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

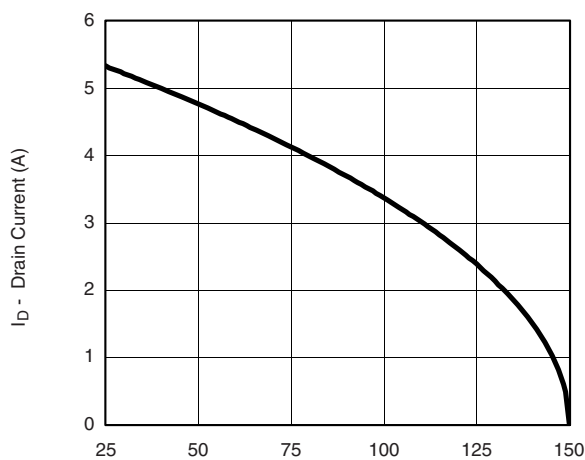
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

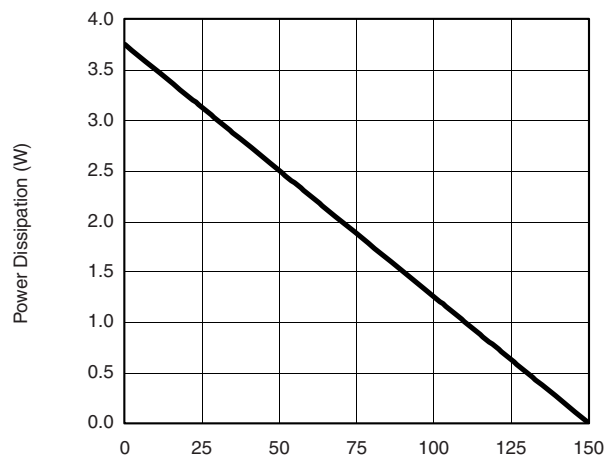
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

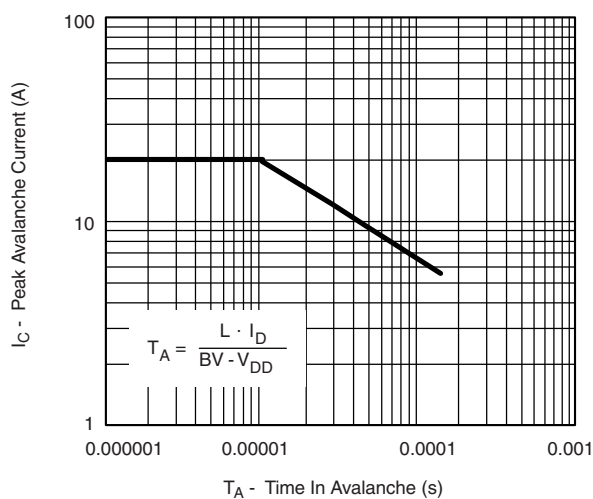
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Single Pulse Power, Junction-to-Ambient


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area

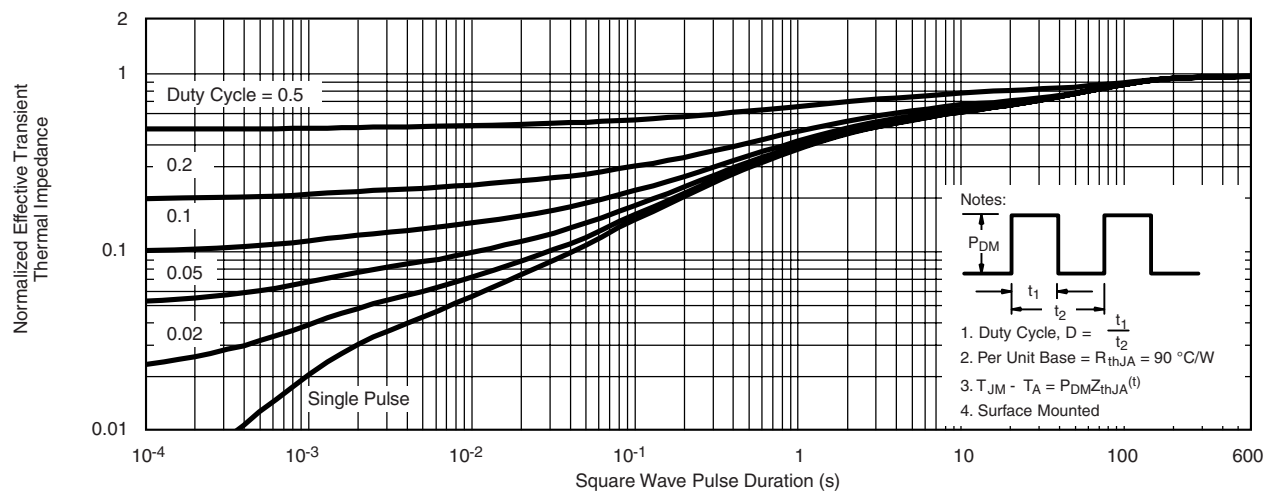
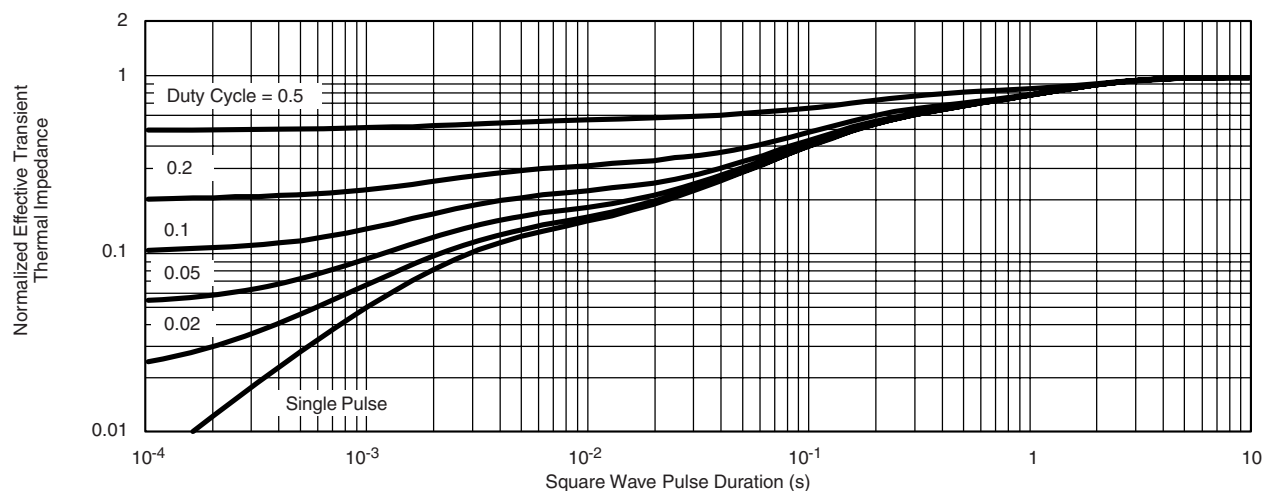
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

 T_C - Case Temperature (°C)

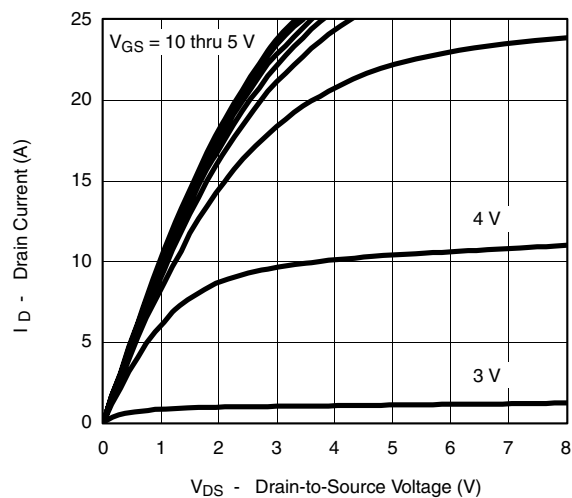
Current Derating*

 T_C - Case Temperature (°C)

Power Derating

 T_A - Time In Avalanche (s)

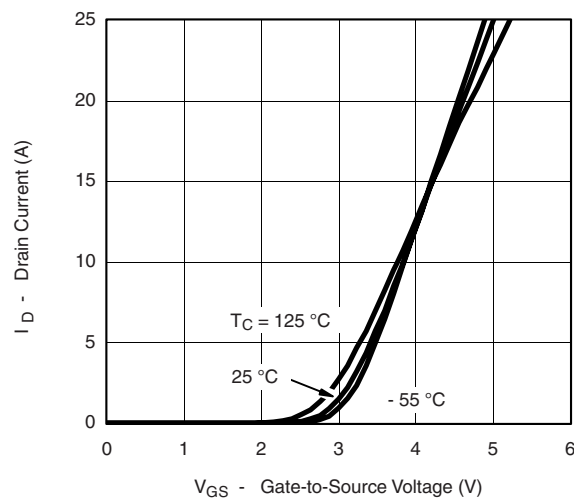
Single Pulse Avalanche Capability

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

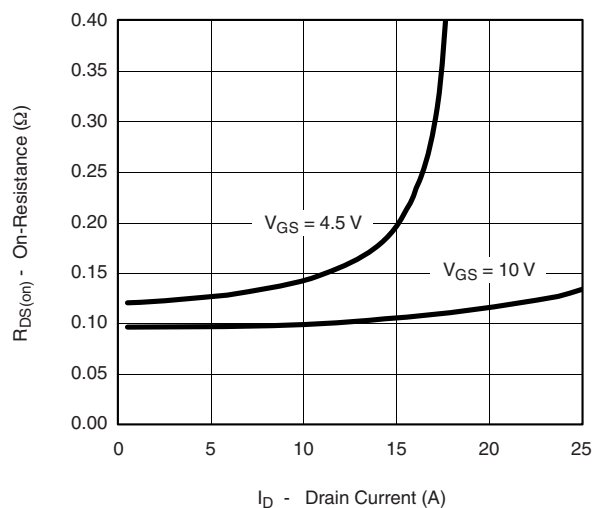
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Case

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


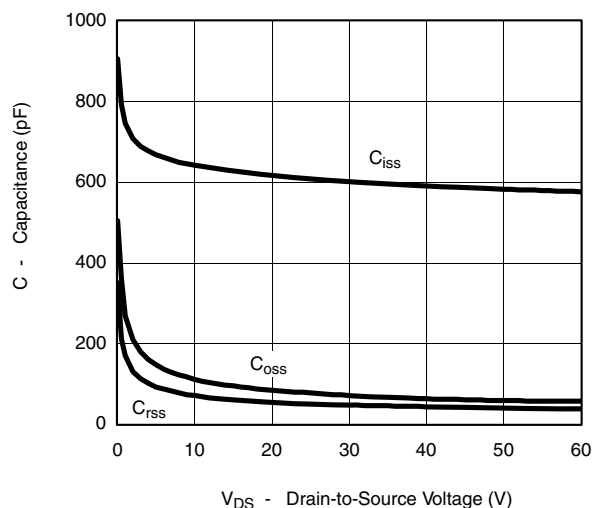
Output Characteristics



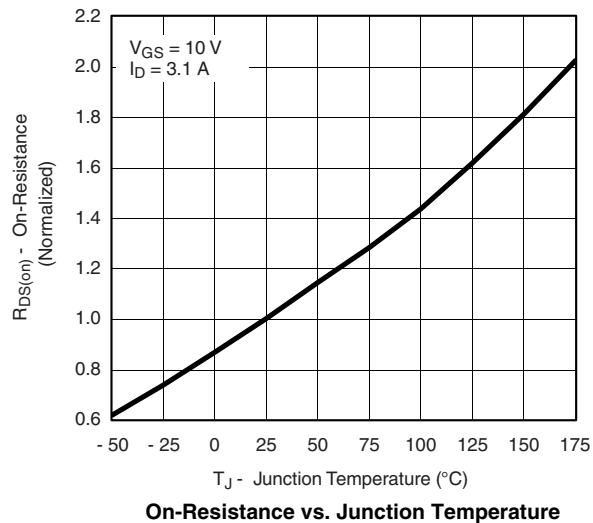
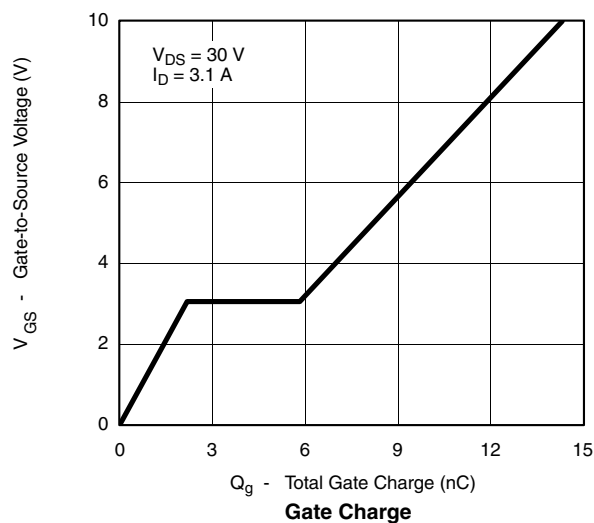
Transfer Characteristics



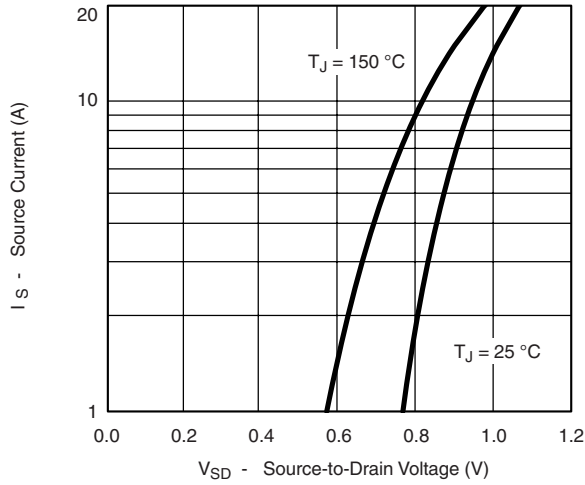
On-Resistance vs. Drain Current



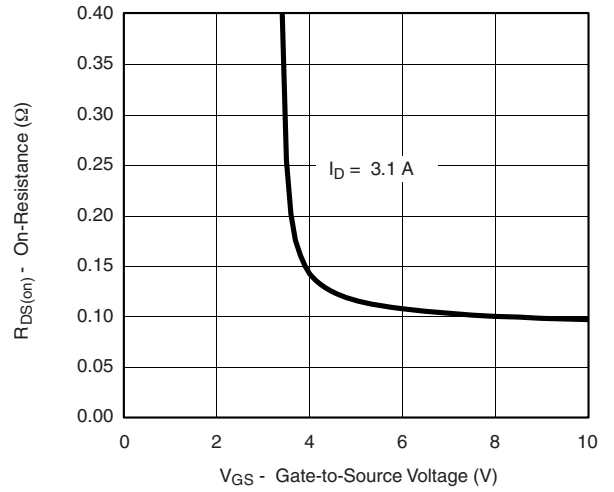
Capacitance



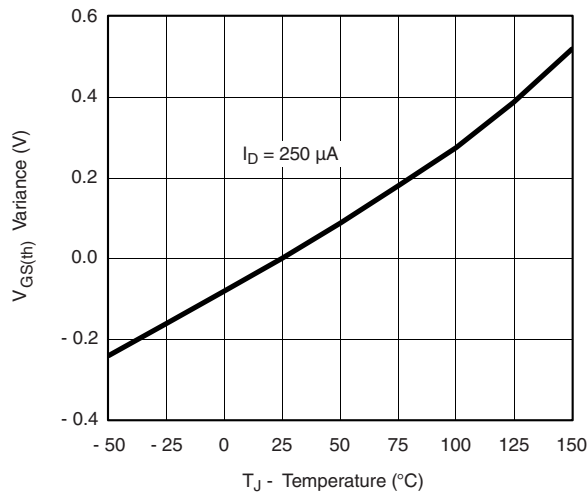
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



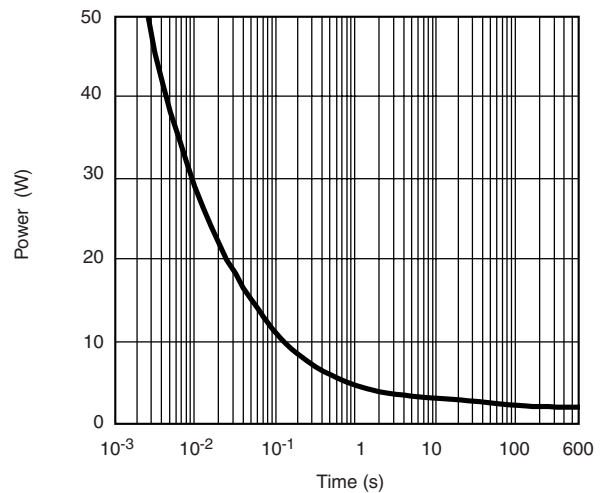
Source-Drain Diode Forward Voltage



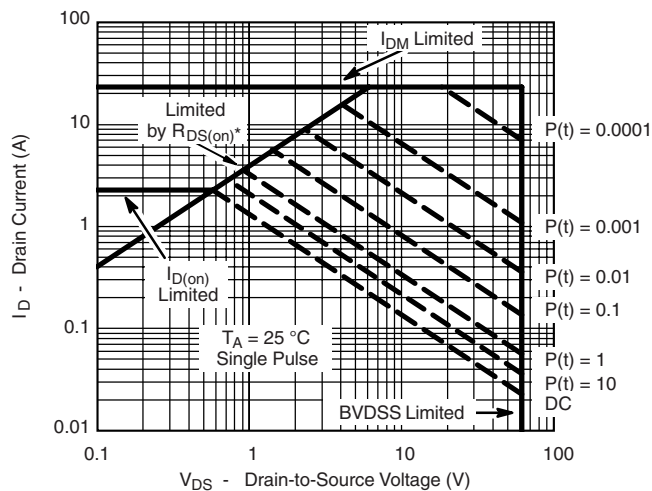
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

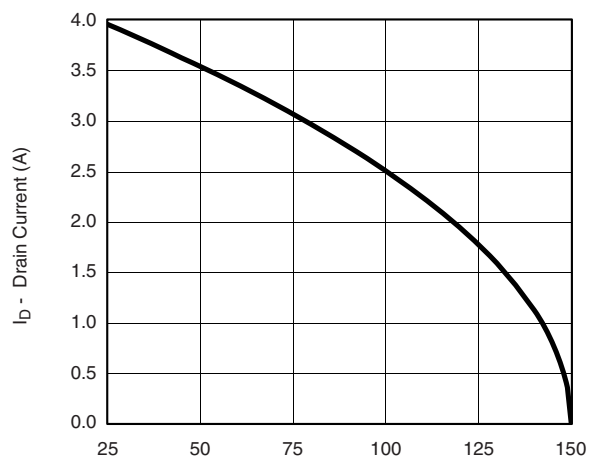


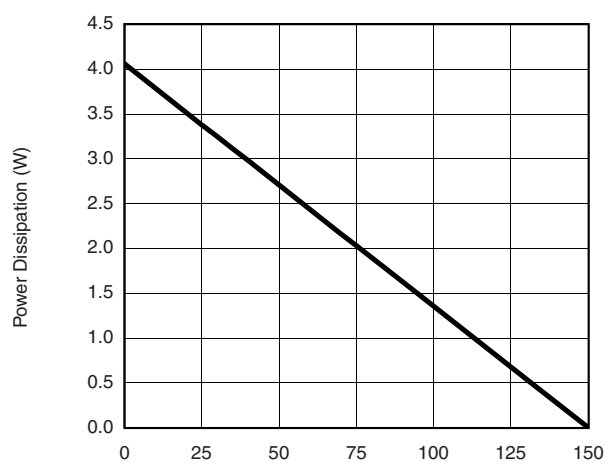
Single Pulse Power

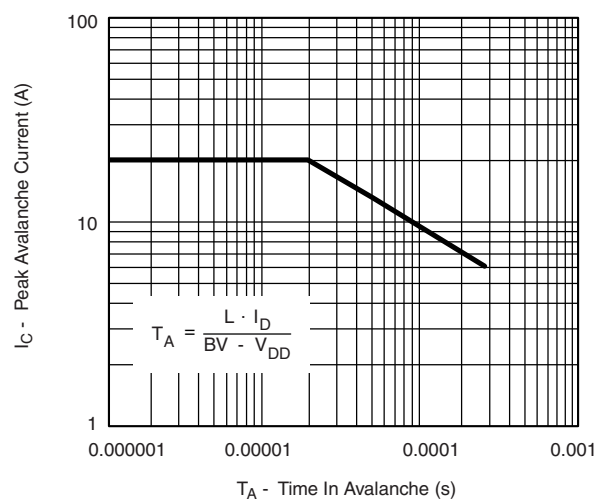


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

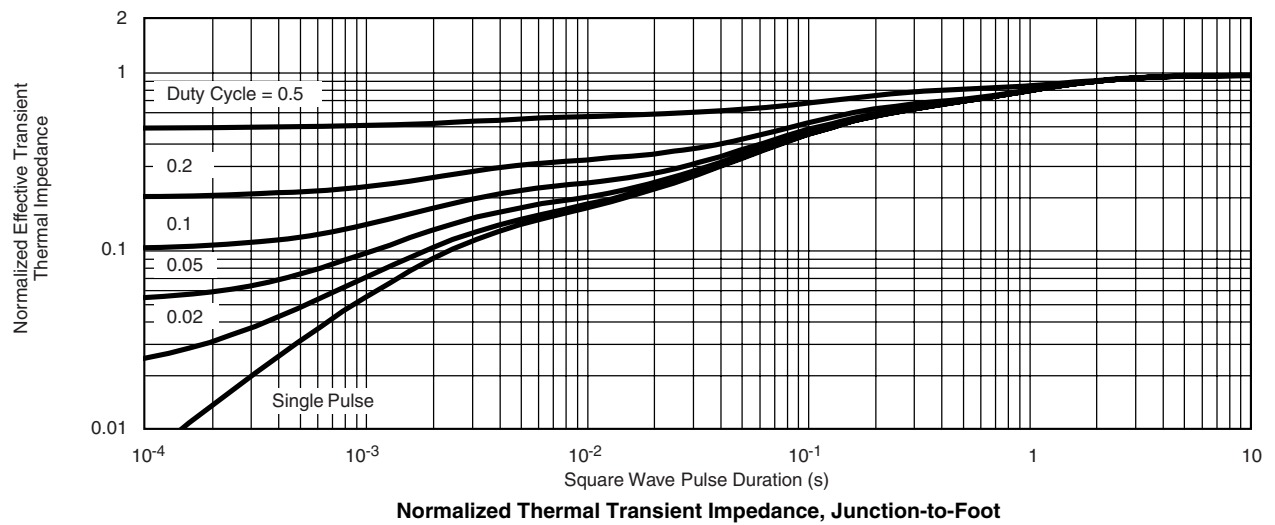
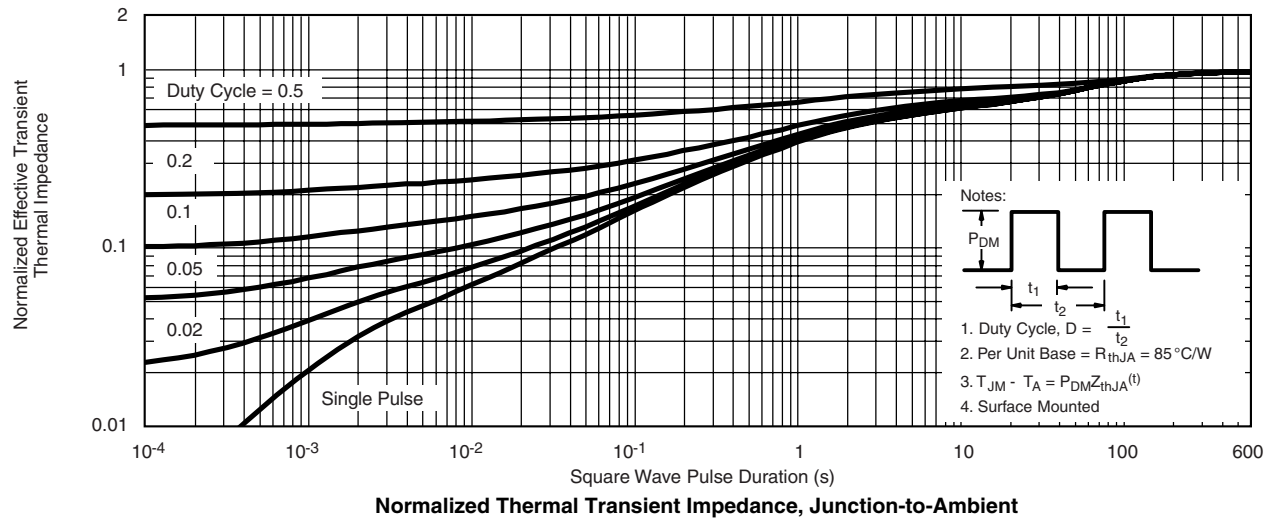
Safe Operating Area, Junction-to-Case

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

 T_C - Case Temperature (°C)

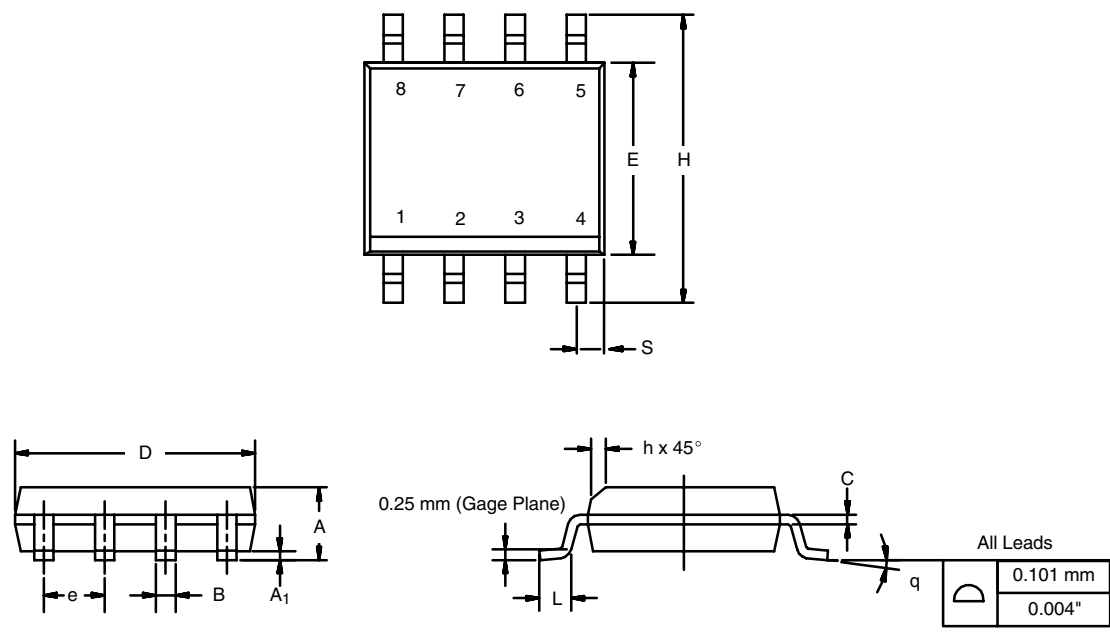
Current Derating*

 T_C - Case Temperature (°C)

Power Derating, Junction-to-Foot

Single Pulse Avalanche Capability

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

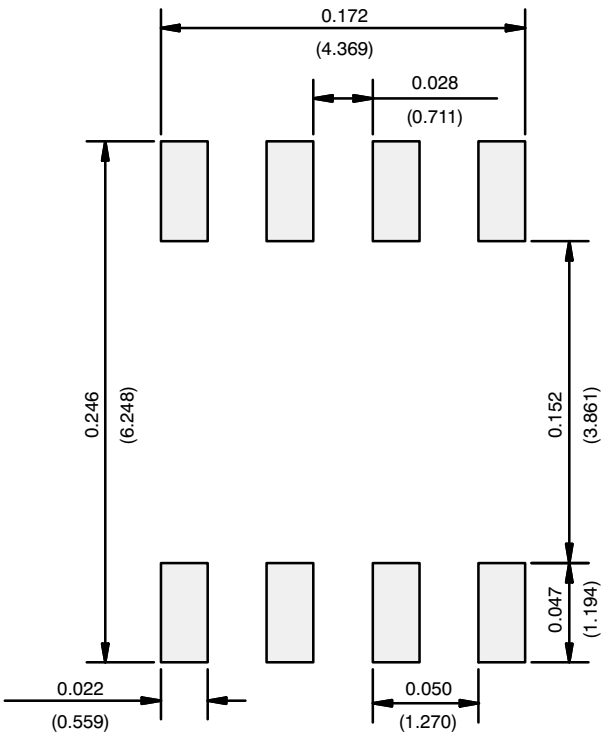
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


SOIC (NARROW): 8-LEAD
JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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All products due to improve reliability, function or design or for other reasons, product specifications and data are subject to change without notice.

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Taiwan VBsemi Electronics Co., Ltd. hereby certify that all of its products comply identified as halogen-free halogen-free standards required by the JEDEC JS709A. Please note that some Taiwanese VBsemi documents still refer to the definition of IEC 61249-2-21, and we are sure that all products conform to confirm compliance with IEC 61249-2-21 standard level JS709A.