

## RJK1028DSP-VB Datasheet

### N-Channel 100 V (D-S) MOSFET

#### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>d</sup>	$Q_g$ (Typ.)
100	0.124 at $V_{GS} = 10$ V	4.2	4.6 nC
	0.128 at $V_{GS} = 4.5$ V	3.9	

#### FEATURES

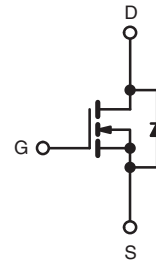
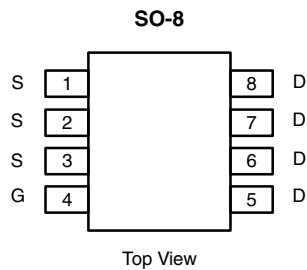
- Trench Power MOSFET
- 100 % UIS Tested

#### APPLICATIONS

- High Frequency Boost Converter
- LED Backlight for LCD TV



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**



N-Channel MOSFET

#### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ )	$T_C = 25^\circ\text{C}$	4.2	A
	$T_C = 70^\circ\text{C}$	3.5	
	$T_A = 25^\circ\text{C}$	3.0 <sup>a, b</sup>	
	$T_A = 70^\circ\text{C}$	2.4 <sup>a, b</sup>	
Pulsed Drain Current	$I_{DM}$	16	A
Continuous Source-Drain Diode Current	$T_C = 25^\circ\text{C}$	4.0	
	$T_A = 25^\circ\text{C}$	2 <sup>a, b</sup>	
Single Avalanche Current	$I_{AS}$	6	A
Single Avalanche Energy	$E_{AS}$	1.8	mJ
Maximum Power Dissipation	$T_C = 25^\circ\text{C}$	4.8	W
	$T_C = 70^\circ\text{C}$	3	
	$T_A = 25^\circ\text{C}$	2.4 <sup>a, b</sup>	
	$T_A = 70^\circ\text{C}$	1.5 <sup>a, b</sup>	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

#### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a, c</sup>	$R_{thJA}$	42	53	$^\circ\text{C/W}$
Maximum Junction-to-Foot (Drain)	$R_{thJF}$	21	26	

Notes:

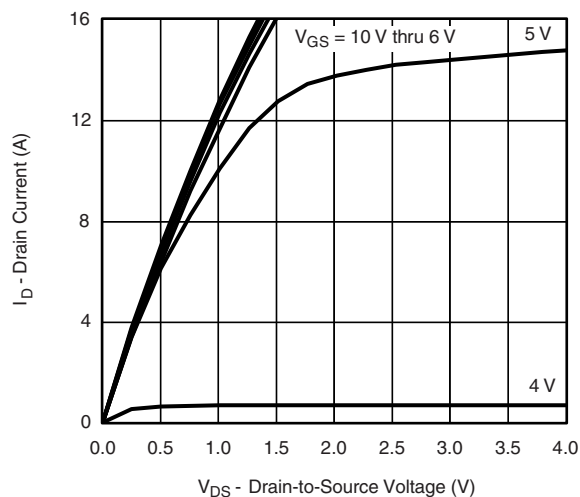
- Surface mounted on 1" x 1" FR4 board.
- $t = 10$  s.
- Maximum under steady state conditions is  $85^\circ\text{C/W}$ .
- Based on  $T_C = 25^\circ\text{C}$ .

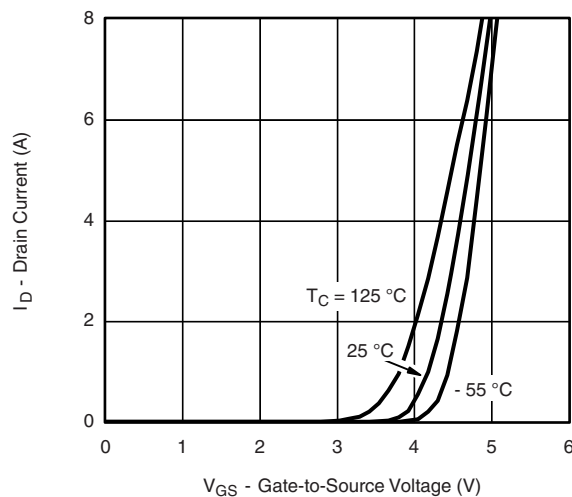
SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	100			V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA		110		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>			- 7.5		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1		3	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	8			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.7 A		0.124		Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 2.5 A		0.128		
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 2.7 A		7		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V, f = 1 MHz		470		pF
Output Capacitance	C <sub>oss</sub>			50		
Reverse Transfer Capacitance	C <sub>rss</sub>			25		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.7 A		7.1	11	nC
		V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 6 V, I <sub>D</sub> = 2.7 A		4.6	7	
Gate-Source Charge	Q <sub>gs</sub>			1.7		
Gate-Drain Charge	Q <sub>gd</sub>			2		
Gate Resistance	R <sub>g</sub>	f = 1 MHz		3		Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 50 V, R <sub>L</sub> = 23.8 Ω I <sub>D</sub> ≅ 2.1 A, V <sub>GEN</sub> = 6 V, R <sub>g</sub> = 1 Ω		10	15	ns
Rise Time	t <sub>r</sub>			10	15	
Turn-Off Delay Time	t <sub>d(off)</sub>			10	15	
Fall Time	t <sub>f</sub>			10	15	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 50 V, R <sub>L</sub> = 23.8 Ω I <sub>D</sub> ≅ 2.1 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		10	15	
Rise Time	t <sub>r</sub>			10	15	
Turn-Off Delay Time	t <sub>d(off)</sub>			12	20	
Fall Time	t <sub>f</sub>			10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			4	A
Pulse Diode Forward Current	I <sub>SM</sub>				8	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 2.1 A, V <sub>GS</sub> = 0 V		0.8	1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 2.1 A, dI/dt = 100 A/μs, T <sub>J</sub> = 25 °C		50	80	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			75	120	nC
Reverse Recovery Fall Time	t <sub>a</sub>			28		ns
Reverse Recovery Rise Time	t <sub>b</sub>			22		

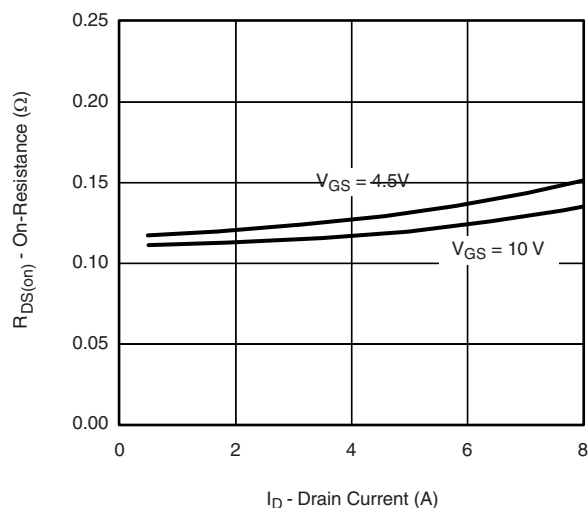
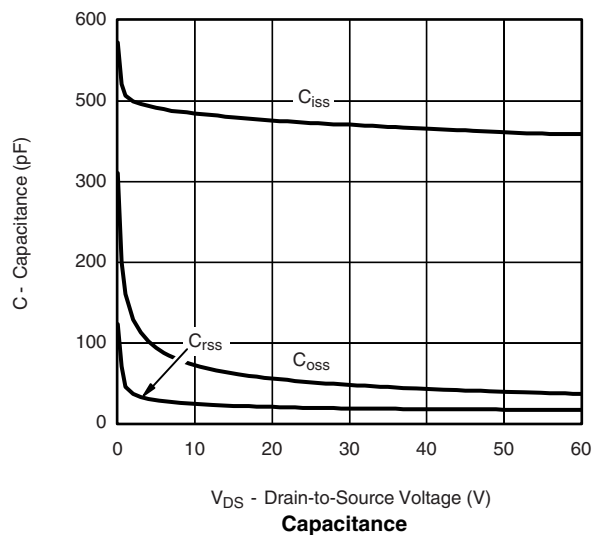
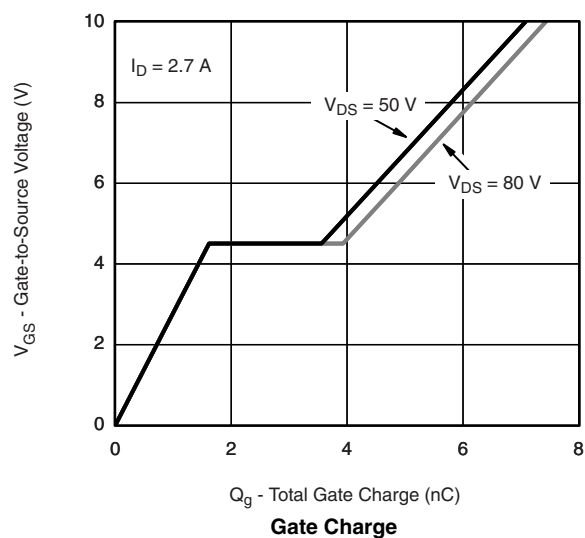
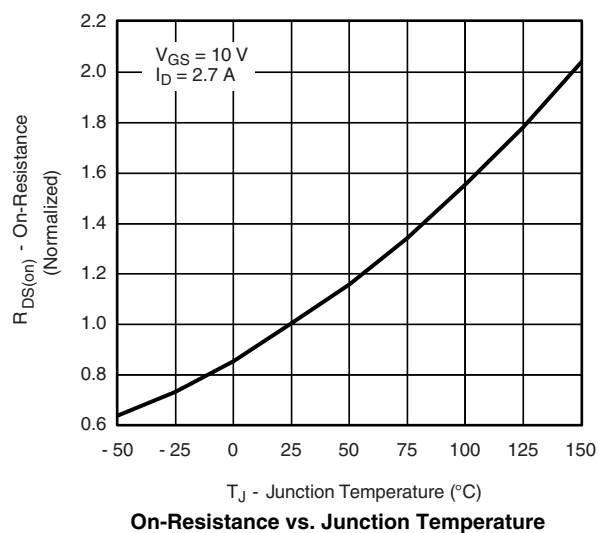
Notes:

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
 b. Guaranteed by design, not subject to production testing.

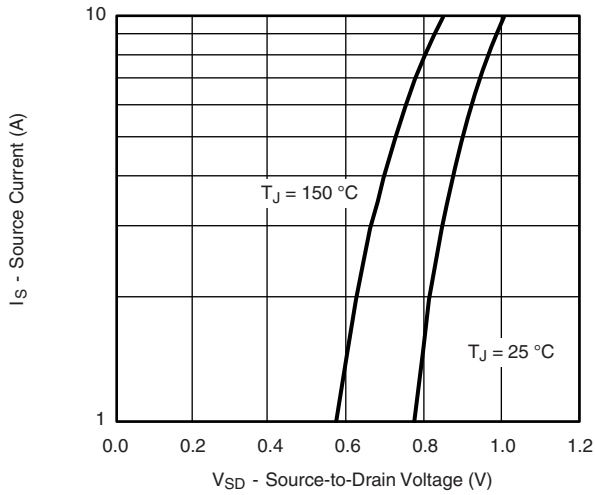
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

 $V_{DS}$  - Drain-to-Source Voltage (V)

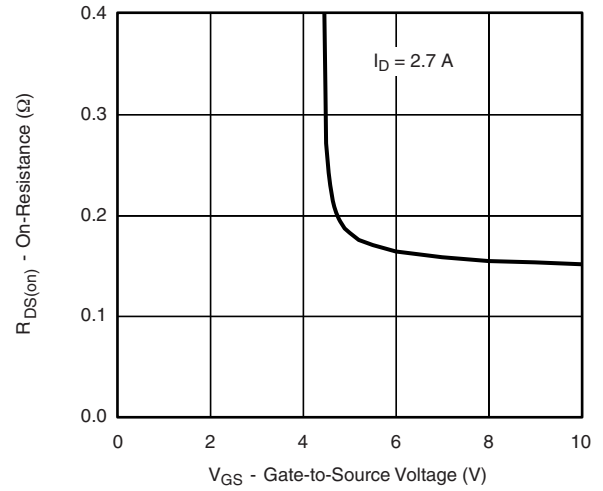
**Output Characteristics**

 $V_{GS}$  - Gate-to-Source Voltage (V)

**Transfer Characteristics**

**On-Resistance vs. Drain Current**

**Capacitance**

**Gate Charge**

**On-Resistance vs. Junction Temperature**

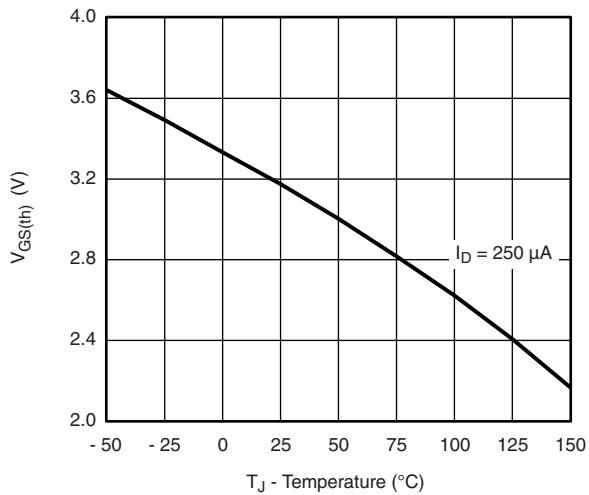
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



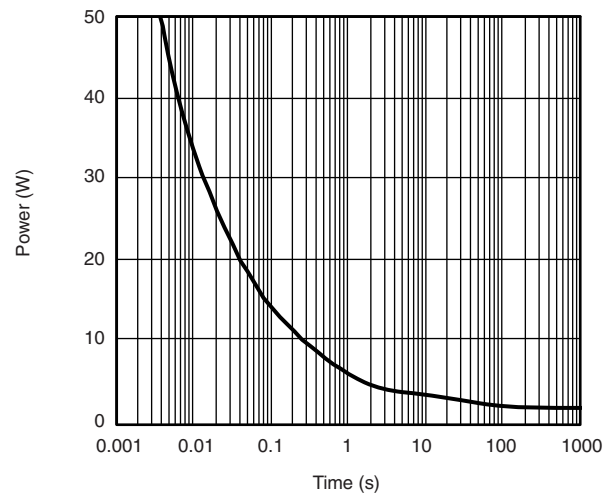
Source-Drain Diode Forward Voltage



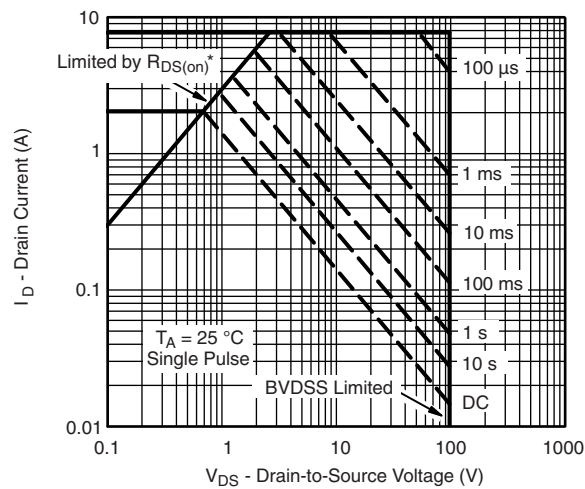
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



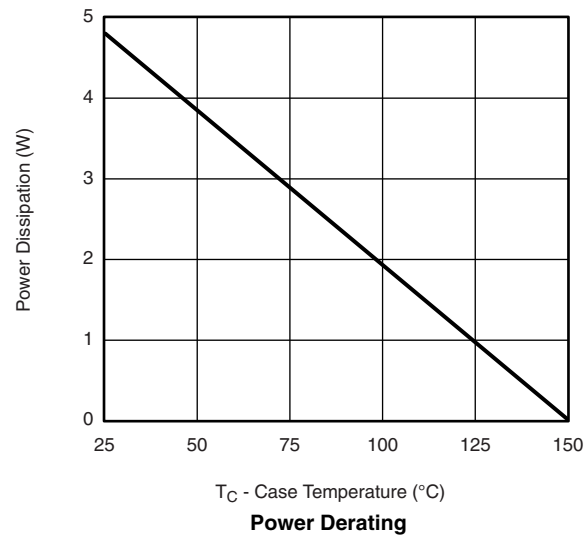
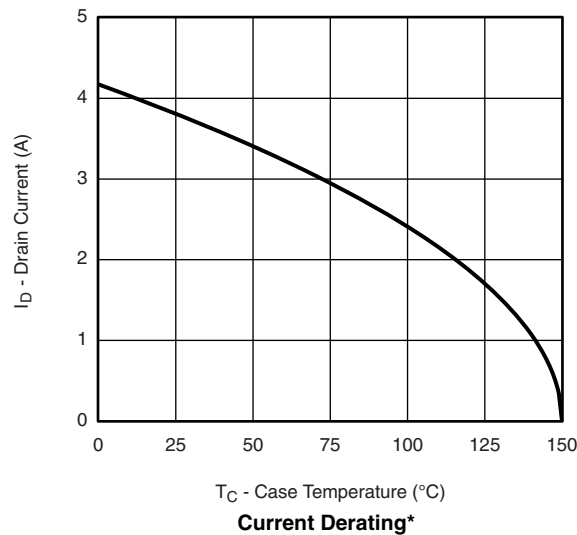
Single Pulse Power



\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

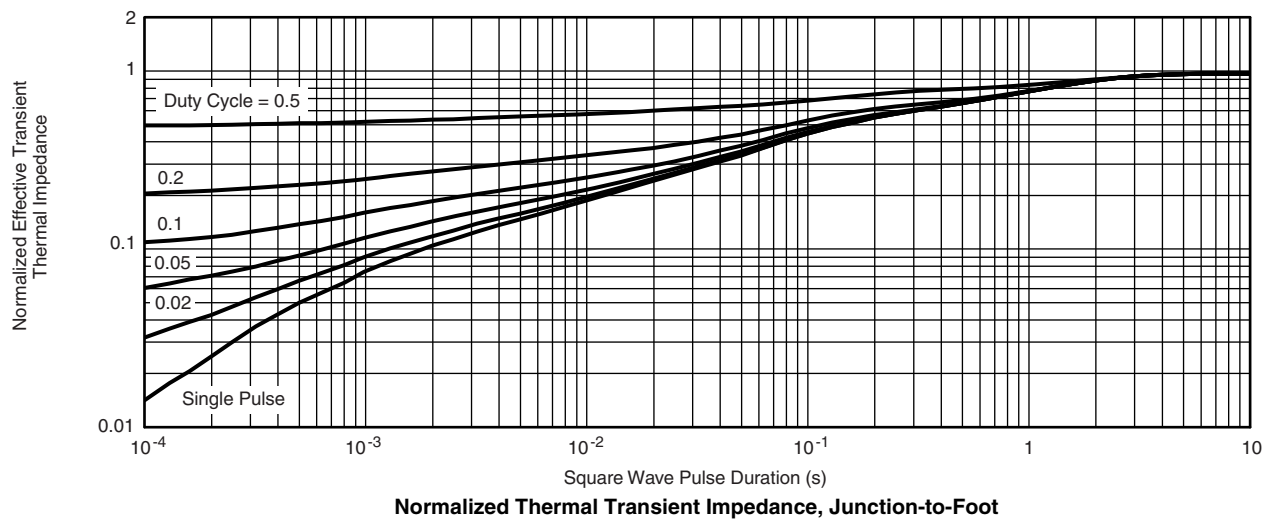
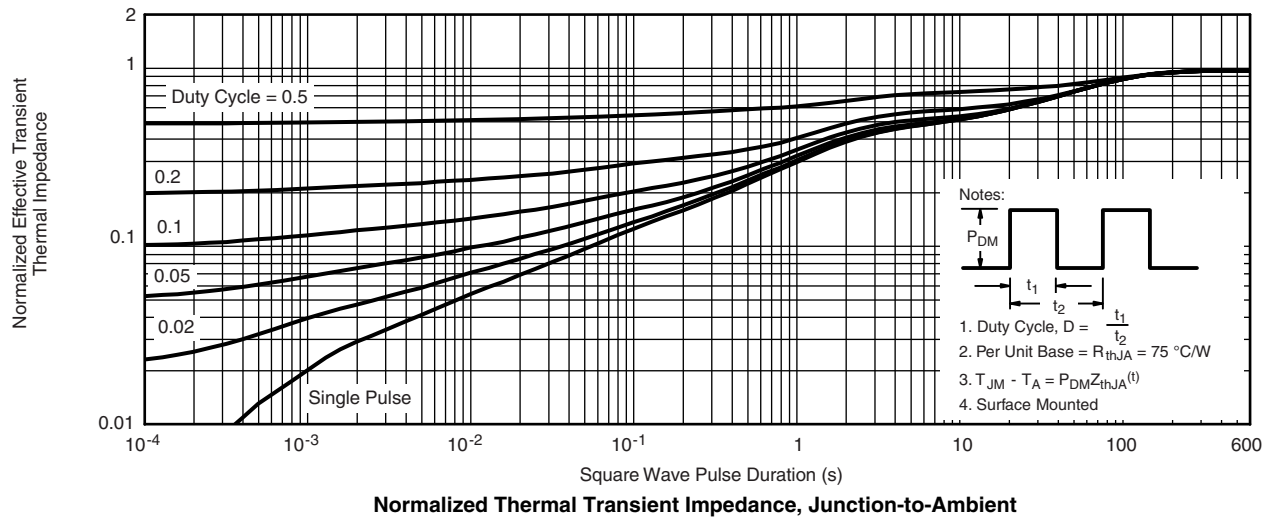
Safe Operating Area, Junction-to-Ambient

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

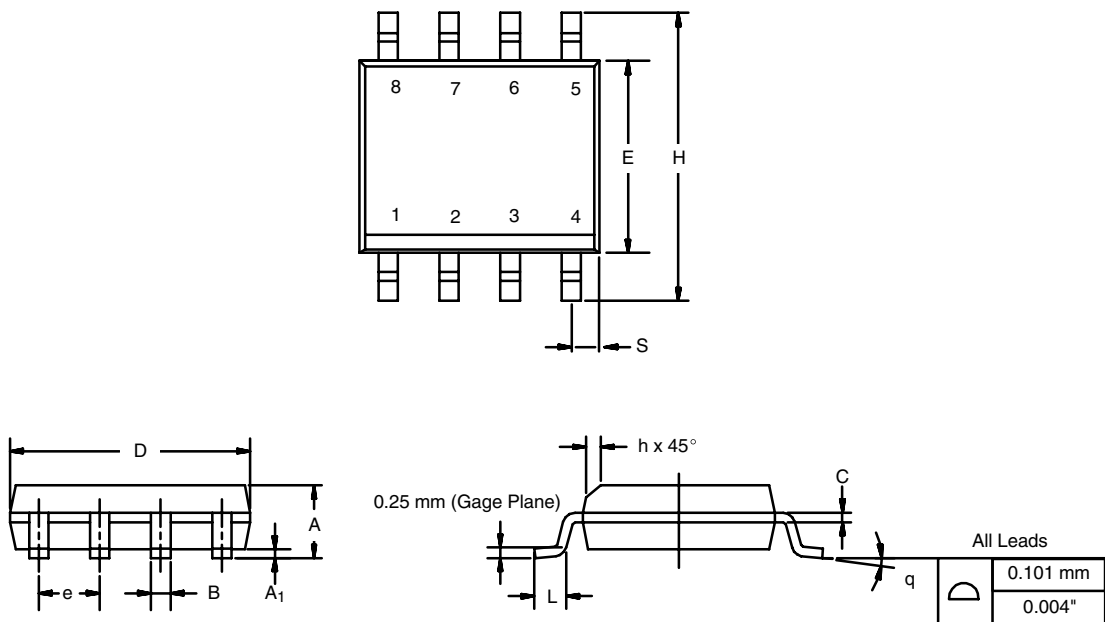


\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**SOIC (NARROW): 8-LEAD**  
JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

## RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads  
Dimensions in Inches/(mm)



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