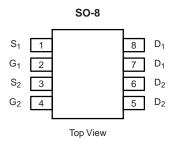


P2003KV-VB Datasheet Dual P-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^{d, e}	Q _g (Typ.)			
- 30	0.021 at V_{GS} = - 10 V	- 8.0	15 nC			
- 30	0.028 at V _{GS} = - 4.5 V	- 7.0	10110			



FEATURES

- Halogen-free
- Trench Power MOSFET
- 100 % UIS Tested

APPLICATIONS

- Load Switches
 - Notebook PCs
 - Desktop PCs
 - Game Stations



D₁ P-Channel MOSFET

G1 0

 S_1

D₂ P-Channel MOSFET

 S_2

C

G₂ C

ABSOLUTE MAXIMUM RATINGS	A = 25 C, unless othe	1		
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	- 30	V	
Gate-Source Voltage	V _{GS}	± 20	v	
	T _C = 25 °C		- 9.5 ^e	
Continuous Drain Current ($T_1 = 150 \text{ °C}$)	T _C = 70 °C		- 8.0 ^e	
Continuous Drain Current $(1) = 150$ C)	T _A = 25 °C	I _D	- 8.3 ^{a, b}	
	T _A = 70 °C		- 7.9 ^{a, b}	Α
Pulsed Drain Current	I _{DM}	- 32 ^e	A	
Orational Design Diada Oracet	T _C = 25 °C	1-	- 4.1	
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	- 2.0 ^{a, b}	
Avalanche Current	L = 0.1 mH	I _{AS}	- 20	
Single-Pulse Avalanche Energy	L = 0.1 IIIH	E _{AS}	20	mJ
	T _C = 25 °C		5.0	
Maximum Dowar Dissinction	T _C = 70 °C	P	3.2	w
Maximum Power Dissipation	T _A = 25 °C	P _D	2.5 ^{a, b}	VV
	T _A = 70 °C	1	1.6 ^{a, b}	
Operating Junction and Storage Temperature Rang	T _J , T _{stq}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient ^{a, c}	t ≤ 10 s	R _{thJA}	38	50	°C/W	
Maximum Junction-to-Foot	Steady State	R _{thJF}	20	25	C/VV	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. t = 10 s.

c. Maximum under Steady State conditions is 85 °C/W.

d. Based on T_C = 25 °C.

e. Limited by package.



Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static					1	1
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 30			V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	1 250.04		- 31		
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = - 250 μA		4.5		mV/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 1.0		- 3.0	V
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA
Zana Casta Maltana Durin Connant	1	$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55 \text{ °C}$			- 1	μA
Zero Gate Voltage Drain Current	IDSS				- 5	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge -10 \text{ V}, \text{ V}_{GS} = -10 \text{ V}$	- 30			А
		V _{GS} = - 10 V, I _D = - 7.3 A		0.021	0.021 0.028	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 6.2 A		0.028		
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 10 V, I _D = - 9.1 A		23		S
Dynamic ^b	L					
Input Capacitance	C _{iss}			1350		
Output Capacitance	C _{oss}	V _{DS} = - 15 V, V _{GS} = 0 V, f = 1 MHz		215		pF
Reverse Transfer Capacitance	C _{rss}			185		
Total Gate Charge	$Q_g = -$	V _{DS} = - 15 V, V _{GS} = - 10 V, I _D = - 9.1 A		32	50	nC
				15	25	
Gate-Source Charge	Q _{gs}	V_{DS} = - 15 V, V_{GS} = - 4.5 V, I_{D} = - 9.1 A		4		
Gate-Drain Charge	Q _{gd}			7.5		
Gate Resistance	R _g	f = 1 MHz		5.8		Ω
Turn-On Delay Time	t _{d(on)}			10	15	
Rise Time	t _r	V_{DD} = - 15 V, R _L = 15 Ω		8	15	
Turn-Off DelayTime	t _{d(off)}	$I_D \cong$ - 1 A, V_{GEN} = - 10 V, R_g = 1 Ω		45	70	1
Fall Time	t _f			12	25	
Turn-On Delay Time	t _{d(on)}			42	70	ns
Rise Time	t _r	V_{DD} = - 15 V, R _L = 15 Ω		35	60	
Turn-Off DelayTime	t _{d(off)}	$I_D \cong$ - 1 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		40	70	
Fall Time	t _f			16	30	
Drain-Source Body Diode Characterist	ics					
Continous Source-Drain Diode Current	۱ _s	T _C = 25 °C			- 4.1	•
Pulse Diode Forward Current	I _{SM}	-			- 32	A
Body Diode Voltage	V _{SD}	I _S = - 2 A, V _{GS} = 0 V		- 0.75	- 1.2	V
Body Diode Reverse Recovery Time				34	60	ns
Body Diode Reverse Recovery Charge	Q _{rr}			22	40	nC
Reverse Recovery Fall Time	t _a	I _F = - 2 A, dl/dt = 100 A/μs, T _J = 25 °C		11		ns
Reverse Recovery Rise Time	t _b	1		23		

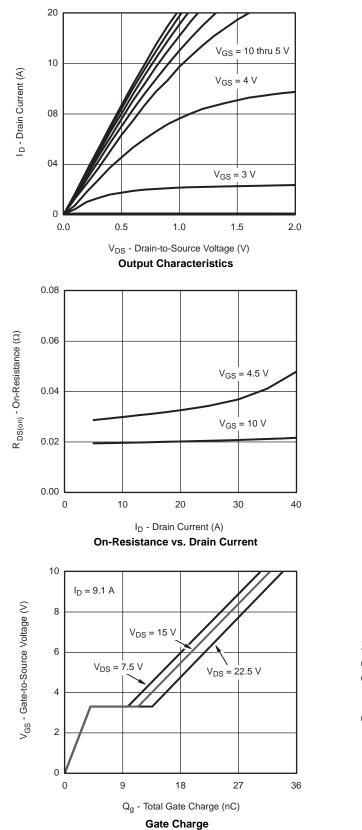
Notes:

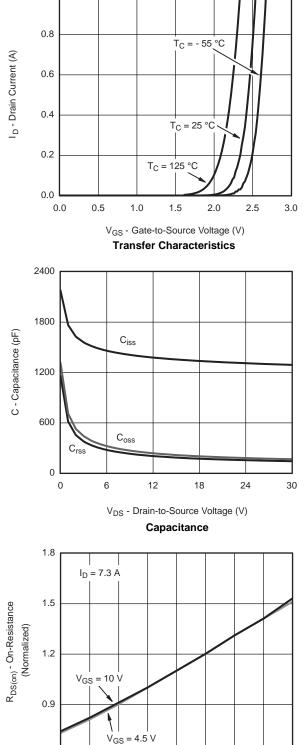
a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.







1.0

0.6

- 50

- 25

0

25

50

T_J - Junction Temperature (°C) On-Resistance vs. Junction Temperature

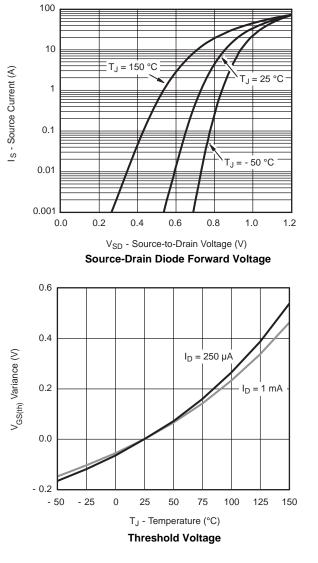
75

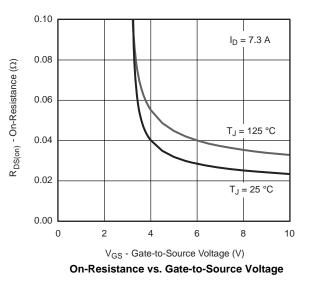
100

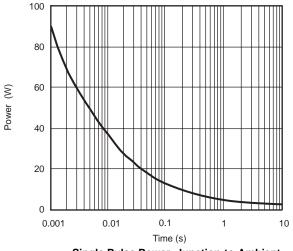
125 150

服务热线:400-655-8788

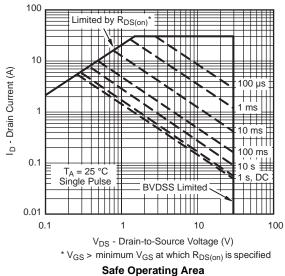




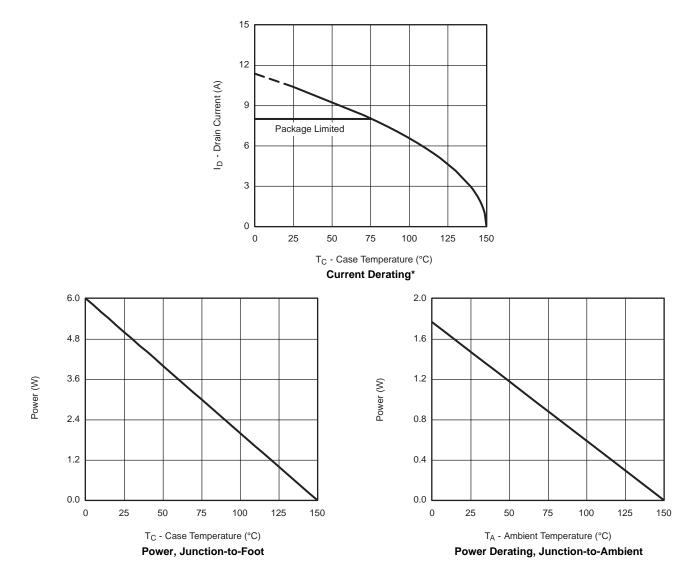




Single Pulse Power, Junction-to-Ambient

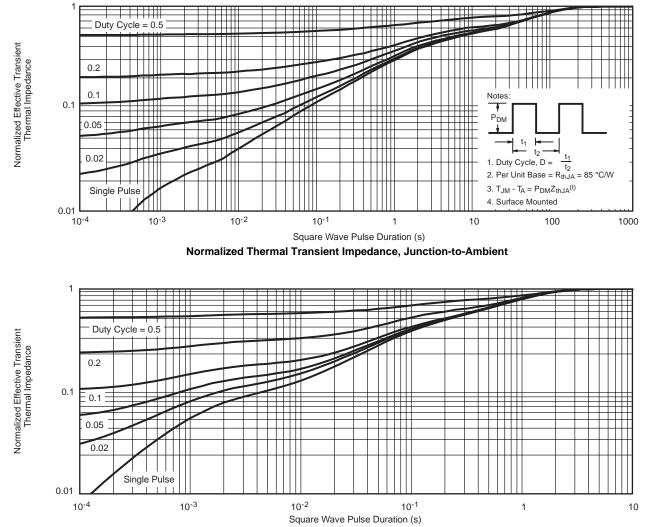






* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





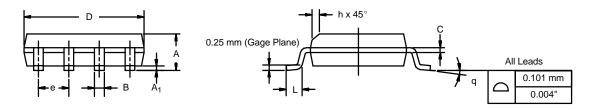
Normalized Thermal Transient Impedance, Junction-to-Foot



SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012





	MILLIM	IETERS	INCHES			
DIM	Min	Мах	Min	Max		
A	1.35	1.75	0.053	0.069		
A ₁	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
E	3.80	4.00	0.150	0.157		
е	1.27 BSC		0.050 BSC			
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498						



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)



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