

RoHS

COMPLIANT HALOGEN

FREE

NDS8961-NL-VB Datasheet Dual N-Channel 30-V (D-S) MOSFET

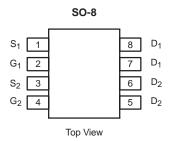
PRODUCT SUMMARY						
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)			
30	0.022 at V_{GS} = 10 V	6.8	15 nC			
30	0.026 at V _{GS} = 4.5 V	6.0	15110			

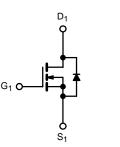
FEATURES

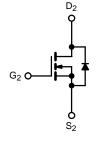
- Halogen-free According to IEC 61249-2-21
 Definition
- Trench Power MOSFET
- 100 % UIS Tested
- 100 % Rg Tested
- Compliant to RoHS Directive 2002/95/EC

APPLICATIONS

- Set Top Box
- Low Current DC/DC







N-Channel MOSFET

N-Channel MOSFET

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	30	V	
Gate-Source Voltage		V _{GS}	± 20	v	
	T _C = 25 °C	_	6.8 ^a		
Continuous Drain Current (T ₁ = 150 °C)	T _C = 70 °C	I _D	5.6		
	T _A = 25 °C	U	6.2 ^{b, c}		
	T _A = 70 °C		5.2 ^{b, c}	A	
Pulsed Drain Current		I _{DM}	30		
Continuous Source-Drain Diode Current	T _C = 25 °C	- I _S	2.25		
	T _A = 25 °C	'S	1.48 ^{b, c}		
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	5		
Single Pulse Avalanche Energy		E _{AS}	1.25	mJ	
	T _C = 25 °C		2.7		
Maximum Power Dissipation	T _C = 70 °C	– P _D	1.77	W	
Maximum Power Dissipation	T _A = 25 °C		1.78 ^{b, c}	vv	
	T _A = 70 °C	1	1.14 ^{b, c}		
Operating Junction and Storage Temperature	T _J , T _{stq}	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient ^{a, c, d}	t ≤ 10 s	R _{thJA}	58	70	°C/W	
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	38	45	0/11	

Notes:

a. Package limited, $T_C = 25 \ ^{\circ}C$.

b. Surface Mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. Maximum under Steady State conditions is 110 °C/W.

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static	- 1		•		•		
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = 250 \mu\text{A}$	30			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	1 250 4		32		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA		- 5.0			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	1.0		2.5	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
		$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			1	1	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C			10	μA	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	10			A	
		V _{GS} = 10 V, I _D = 5 A		0.022		Ω	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 4 A		0.026			
Forward Transconductance ^a	g _{fs}	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 5 \text{ A}$		16		S	
Dynamic ^b	<u> </u>			1			
Input Capacitance	C _{iss}			586			
Output Capacitance	C _{oss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz		117		pF	
Reverse Transfer Capacitance	C _{rss}			55			
Total Gate Charge	Qg	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 5 \text{ A}$		15		nC	
				3.7	5.6		
Gate-Source Charge	Q _{gs}	V_{DS} = 15 V, V_{GS} = 4.5 V, I_{D} = 5 A		1.4			
Gate-Drain Charge	Q _{gd}			1.05			
Gate Resistance	Rg	f = 1 MHz	0.8	4.3	8.6	Ω	
Turn-On Delay Time	t _{d(on)}			12	24	-	
Rise Time	t _r	V_{DD} = 15 V, R_L = 3 Ω		55	100		
Turn-Off Delay Time	t _{d(off)}	$\text{I}_\text{D} \cong \text{5}$ A, V_GEN = 4.5 V, R_g = 1 Ω		11	22		
Fall Time	t _f			8	16		
Turn-On Delay Time	t _{d(on)}			4	8	ns	
Rise Time	t _r	V_{DD} = 15 V, R_L = 3 Ω		9	18	-	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 5 \text{ A}, \text{ V}_{\text{GEN}}$ = 10 V, R_g = 1 Ω		10	20		
Fall Time	t _f			6	12		
Drain-Source Body Diode Characteristi	cs		1	•	1		
Continuous Source-Drain Diode Current	۱ _S	T _C = 25 °C			2.25		
Pulse Diode Forward Current	I _{SM}				24	A	
Body Diode Voltage	V _{SD}	$I_{S} = 2 \text{ A}, V_{GS} = 0 \text{ V}$		0.8	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			11	20	ns	
Body Diode Reverse Recovery Charge	Q _{rr}			4	8	nC	
Reverse Recovery Fall Time	ta	$I_F = 5 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, \text{T}_J = 25 ^\circ\text{C}$		7			
Reverse Recovery Rise Time	t _b	1		4	1	ns	

Notes:

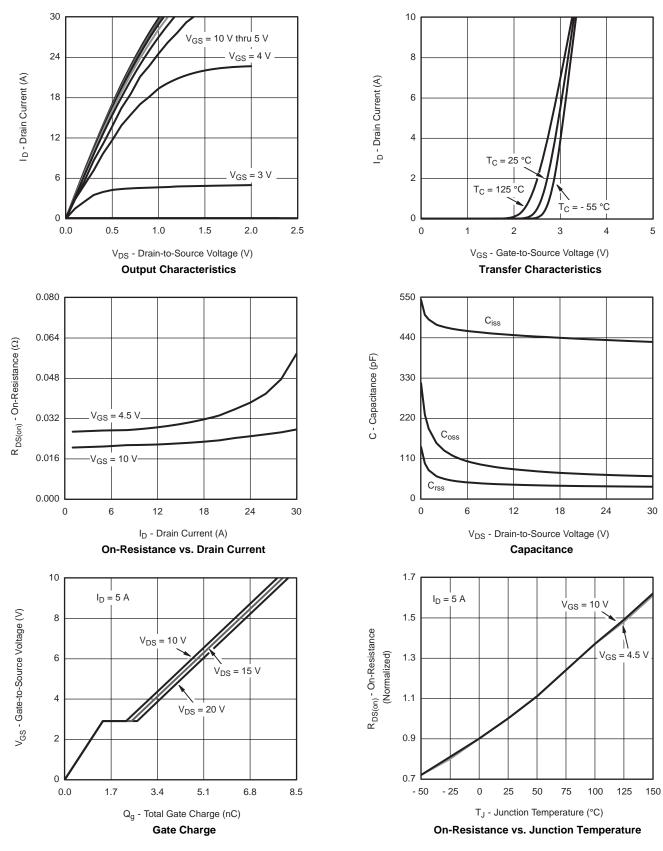
a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %

b. Guaranteed by design, not subject to production testing.

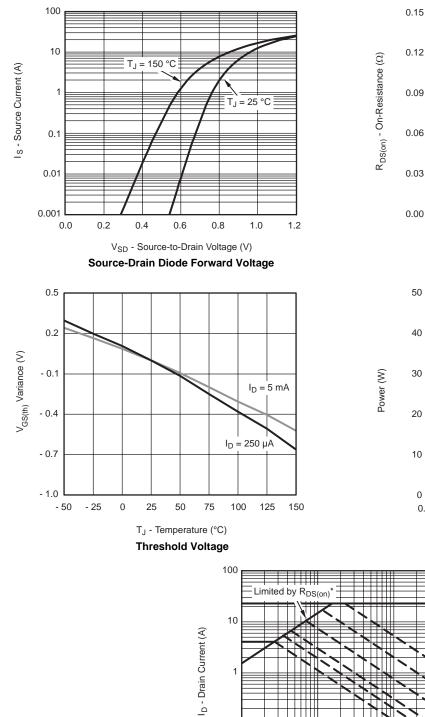
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



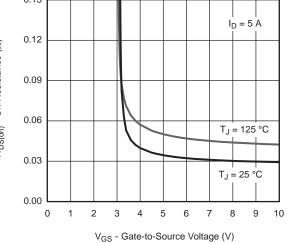




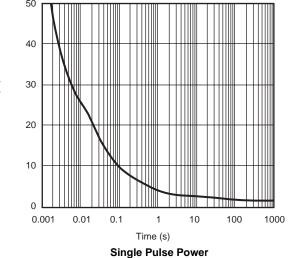


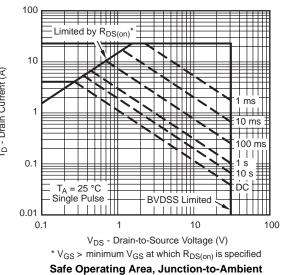


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



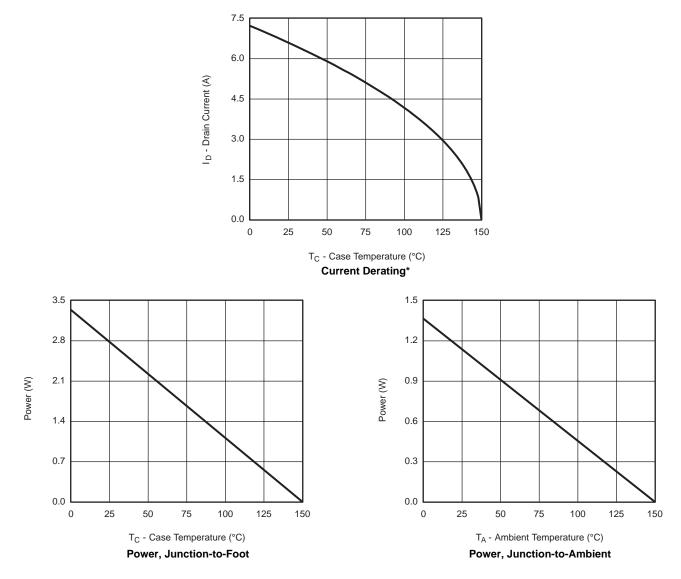
On-Resistance vs. Gate-to-Source Voltage







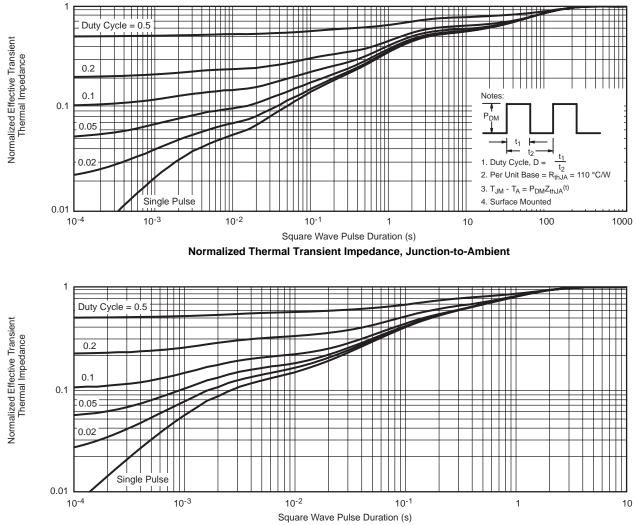
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.







Normalized Thermal Transient Impedance, Junction-to-Foot



SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012





	MILLIMETERS		INC	HES		
DIM	Min	Мах	Min	Max		
A	1.35	1.75	0.053	0.069		
A ₁	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
E	3.80	4.00	0.150	0.157		
е	1.27 BSC		0.050	50 BSC		
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498						



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)



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