

MTBA5C10Q8-VB Datasheet

N-and P-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY

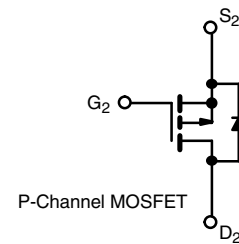
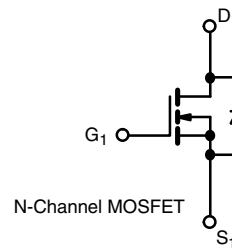
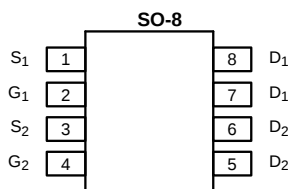
	V _{DS} (V)	R _{DS(on)} (Ω) MAX.	I _D (A) ^a	Q _g (TYP.)
N-Channel	100	0.080 at V _{GS} = 10 V	4.6	4
		0.100 at V _{GS} = 4.5 V	4.0	
P-Channel	-100	0.150 at V _{GS} = -10 V	-3.4	11.6
		0.165 at V _{GS} = -4.5 V	-3.2	

FEATURES

- Trench Power MOSFET
- 100 % R_g and UIS tested

APPLICATIONS

- H bridge / DC-AC inverter
- Brushless DC motors


RoHS
 COMPLIANT
 HALOGEN
FREE
ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Drain-Source Voltage		V _{DS}	100	-100	V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current (T _J = 150 °C)	T _F = 25 °C	I _D	4.6	-3.4	A
	T _F = 70 °C		3.7	-2.7	
	T _A = 25 °C		3.5 ^{b,c}	-2.5 ^{b,c}	
	T _A = 70 °C		2.6 ^{b,c}	-2 ^{b,c}	
Pulsed Drain Current (100 μs Pulse Width)		I _{DM}	25	-20	
Source-Drain Current Diode Current	T _F = 25 °C	I _S	3	-3.5	
	T _A = 25 °C		2 ^{b,c}	-1.9 ^{b,c}	
Pulsed Source-Drain Current (100 μs Pulse Width)		I _{SM}	25	-20	
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	5	-20	mJ
Single Pulse Avalanche Energy		E _{AS}	1.3	20	
Maximum Power Dissipation	T _F = 25 °C	P _D	3.6	4.2	W
	T _F = 70 °C		2.3	2.7	
	T _A = 25 °C		2.3 ^{b,c}	2.3 ^{b,c}	
	T _A = 70 °C		1.5 ^{b,c}	1.5 ^{b,c}	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	N-CHANNEL		P-CHANNEL		UNIT
			TYP.	MAX.	TYP.	MAX.	
Maximum Junction-to-Ambient ^{b,d}	t ≤ 10 s	R _{thJA}	35	55	33	55	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	20	35	17	30	

Notes

- Based on T_F = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under steady state conditions is 90 °C/W (n-channel) and 90 °C/W (p-channel).

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	N-Ch	100	-	-	V
		V _{GS} = 0 V, I _D = -250 μA	P-Ch	-100	-	-	
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA	N-Ch	-	70	-	mV/°C
		I _D = -250 μA	P-Ch	-	-103	-	
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	N-Ch	-	-5.7	-	
		I _D = -250 μA	P-Ch	-	4.5	-	
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	1.5	-	2.5	V
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	-1.5	-	-2.5	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	N-Ch	-	-	100	nA
			P-Ch	-	-	-100	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V	N-Ch	-	-	1	μA
		V _{DS} = -100 V, V _{GS} = 0 V	P-Ch	-	-	-1	
		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 55 °C	N-Ch	-	-	10	
		V _{DS} = -100 V, V _{GS} = 0 V, T _J = 55 °C	P-Ch	-	-	-10	
On-State Drain Current ^b	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	N-Ch	10	-	-	A
		V _{DS} = -5 V, V _{GS} = -10 V	P-Ch	-10	-	-	
Drain-Source On-State Resistance ^b	R _{DS(on)}	V _{GS} = 10 V, I _D = 2 A	N-Ch	-	0.080	-	Ω
		V _{GS} = -10 V, I _D = -2 A	P-Ch	-	0.150	-	
		V _{GS} = 4.5 V, I _D = 1.5 A	N-Ch	-	0.100	-	
		V _{GS} = -4.5 V, I _D = -1 A	P-Ch	-	0.165	-	
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 2 A	N-Ch	-	9	-	S
		V _{DS} = -15 V, I _D = -2 A	P-Ch	-	9.3	-	
Dynamic ^a							
Input Capacitance	C _{iss}	N-Channel V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz P-Channel V _{DS} = -50 V, V _{GS} = 0 V, f = 1 MHz	N-Ch	-	360	-	pF
Output Capacitance	C _{oss}		P-Ch	-	1150	-	
			N-Ch	-	130	-	
Reverse Transfer Capacitance	C _{rss}		P-Ch	-	65	-	
			N-Ch	-	20	-	
			P-Ch	-	40	-	
Total Gate Charge	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 4.5 A	N-Ch	-	7.5	11.5	nC
		V _{DS} = -50 V, V _{GS} = -10 V, I _D = -5 A	P-Ch	-	24	36	
Gate-Source Charge	Q _{gs}	N-Channel V _{DS} = 50 V, V _{GS} = 4.5 V, I _D = 4.5 A P-Channel V _{DS} = -50 V, V _{GS} = -4.5 V, I _D = -5 A	N-Ch	-	4	6	
			P-Ch	-	11.6	18	
Gate-Drain Charge	Q _{gd}		N-Ch	-	1.2	-	
			P-Ch	-	3.8	-	
			N-Ch	-	2	-	
			P-Ch	-	5	-	
Gate Resistance	R _g	f = 1 MHz	N-Ch	0.6	3.3	6.6	Ω
			P-Ch	3	13	26	

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Dynamic ^a							
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 50 V, R _L = 13.8 Ω I _D ≅ 3.6 A, V _{GEN} = 10 V, R _g = 1 Ω	N-Ch	-	5	10	ns
			P-Ch	-	7	15	
Rise Time	t _r		N-Ch	-	11	20	
			P-Ch	-	11	20	
Turn-Off Delay Time	t _{d(off)}	N-Ch	-	12	25		
		P-Ch	-	65	130		
Fall Time	t _f	N-Ch	-	6	15		
		P-Ch	-	20	40		
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 50 V, R _L = 13.8 Ω I _D ≅ 3.6 A, V _{GEN} = 4.5 V, R _g = 1 Ω	N-Ch	-	32	65	
			P-Ch	-	55	110	
Rise Time	t _r		N-Ch	-	73	150	
			P-Ch	-	80	160	
Turn-Off Delay Time	t _{d(off)}	N-Ch	-	14	30		
		P-Ch	-	42	85		
Fall Time	t _f	N-Ch	-	12	25		
		P-Ch	-	25	50		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	T _F = 25 °C	N-Ch	-	-	3	A
			P-Ch	-	-	-3.5	
Pulse Diode Forward Current ^a	I _{SM}		N-Ch	-	-	30	
			P-Ch	-	-	-20	
Body Diode Voltage	V _{SD}	I _S = 3.6 A	N-Ch	-	0.83	1.2	V
		I _S = -4 A	P-Ch	-	-0.8	-1.2	
Body Diode Reverse Recovery Time	t _{rr}	N-Channel I _F = 3.6 A, dI/dt = 100 A/μs, T _J = 25 °C	N-Ch	-	30	60	ns
			P-Ch	-	42	85	
Body Diode Reverse Recovery Charge	Q _{rr}		N-Ch	-	27	55	nC
			P-Ch	-	93	190	
Reverse Recovery Fall Time	t _a	P-Channel I _F = -4 A, dI/dt = -100 A/μs, T _J = 25 °C	N-Ch	-	19	-	ns
			P-Ch	-	36	-	
Reverse Recovery Rise Time	t _b		N-Ch	-	11	-	
			P-Ch	-	6	-	

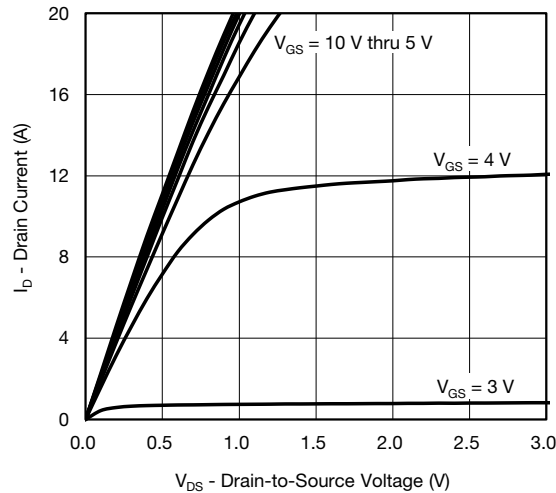
Notes

- a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

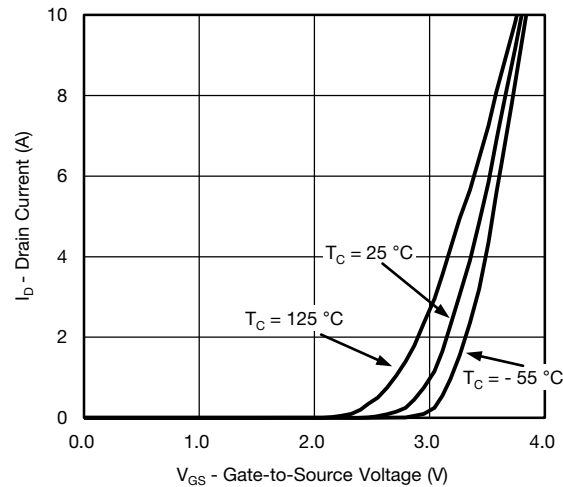
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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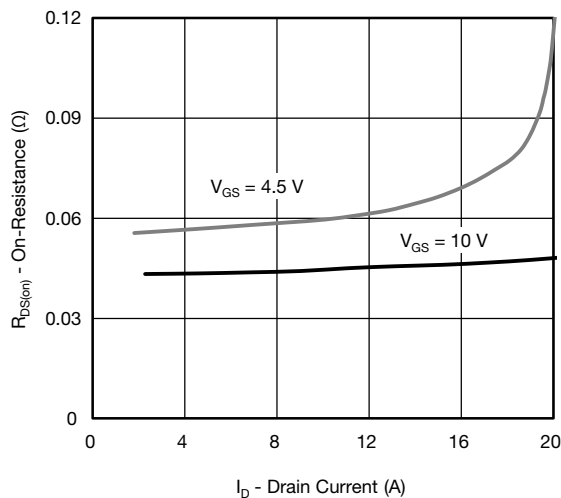
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



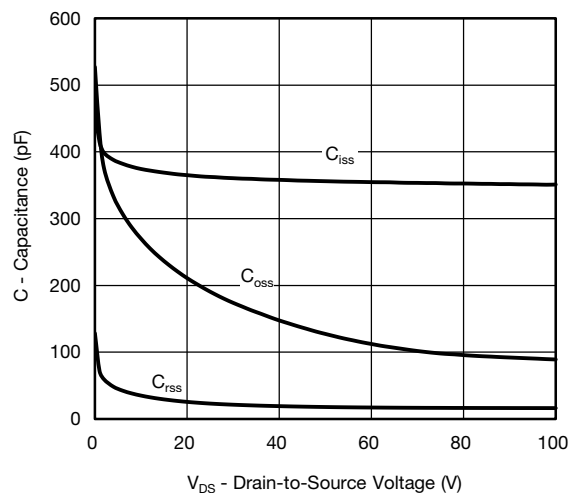
Output Characteristics



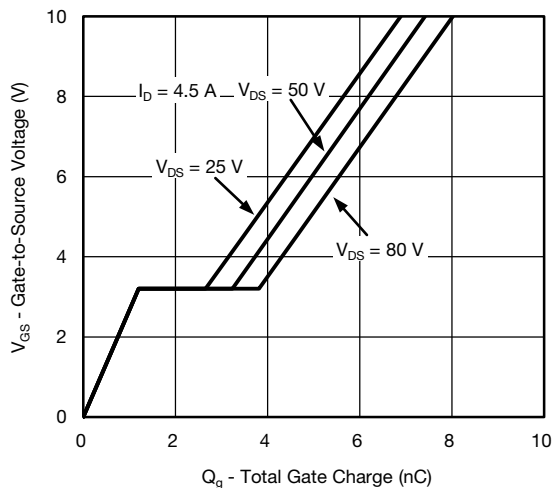
Transfer Characteristics



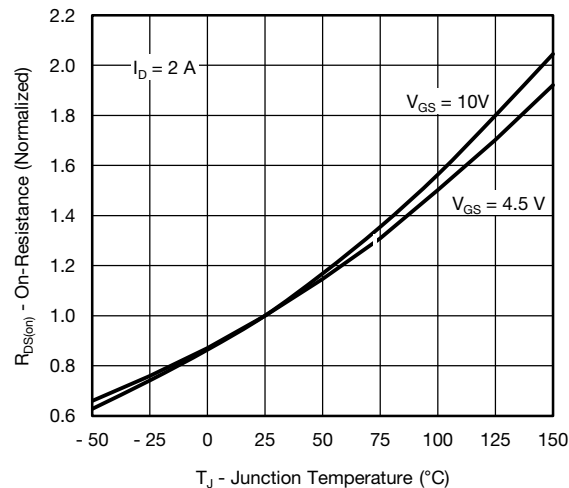
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

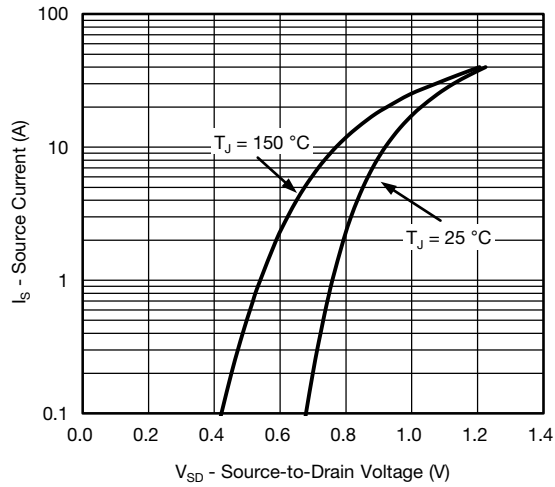


Gate Charge

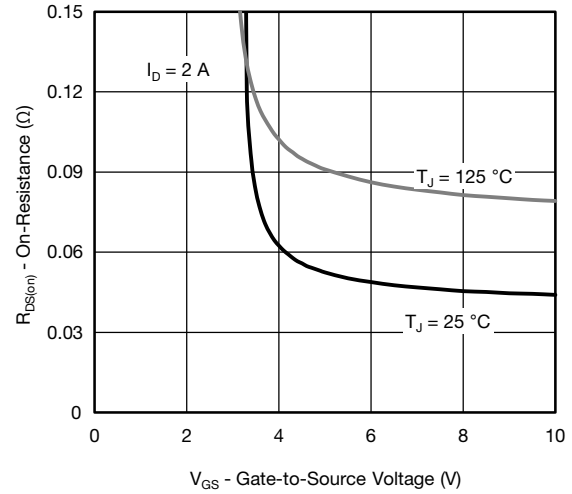


On-Resistance vs. Junction Temperature

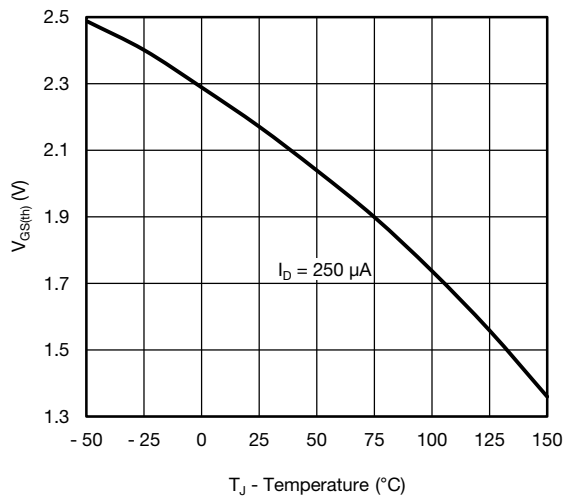
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



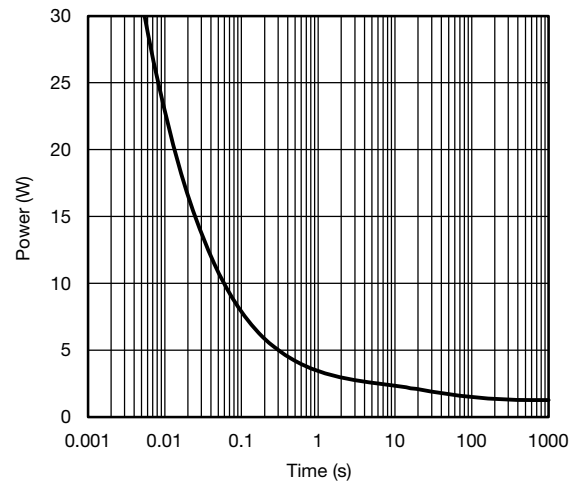
Source-Drain Diode Forward Voltage



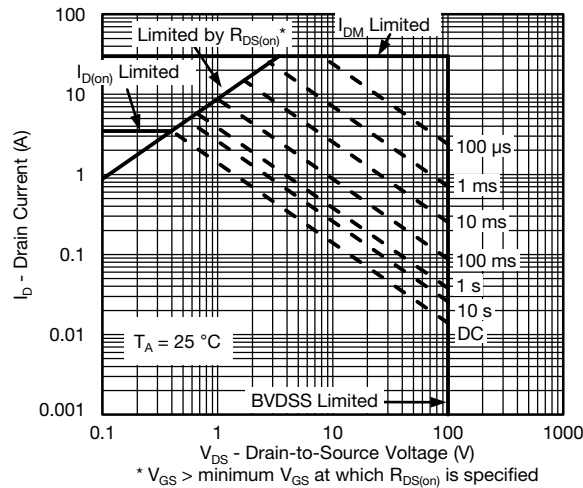
On-Resistance vs. Gate-to-Source Voltage



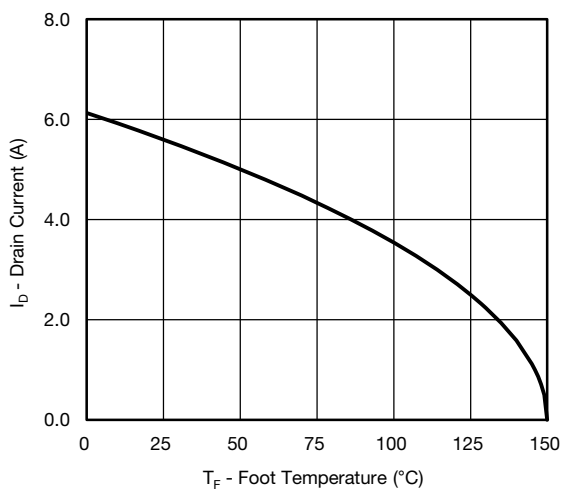
Threshold Voltage



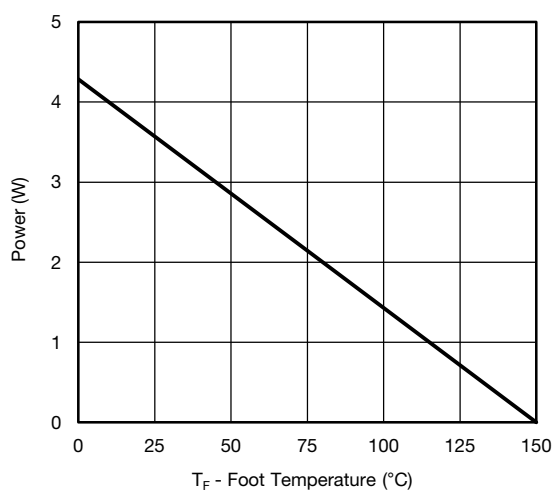
Single Pulse Power, Junction-to-Ambient



N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



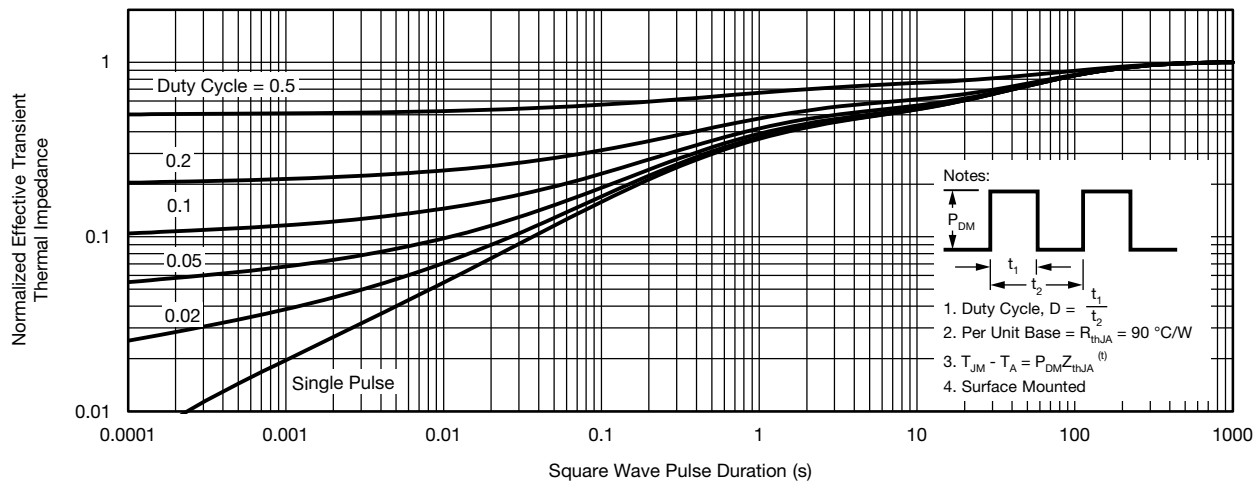
Current Derating*



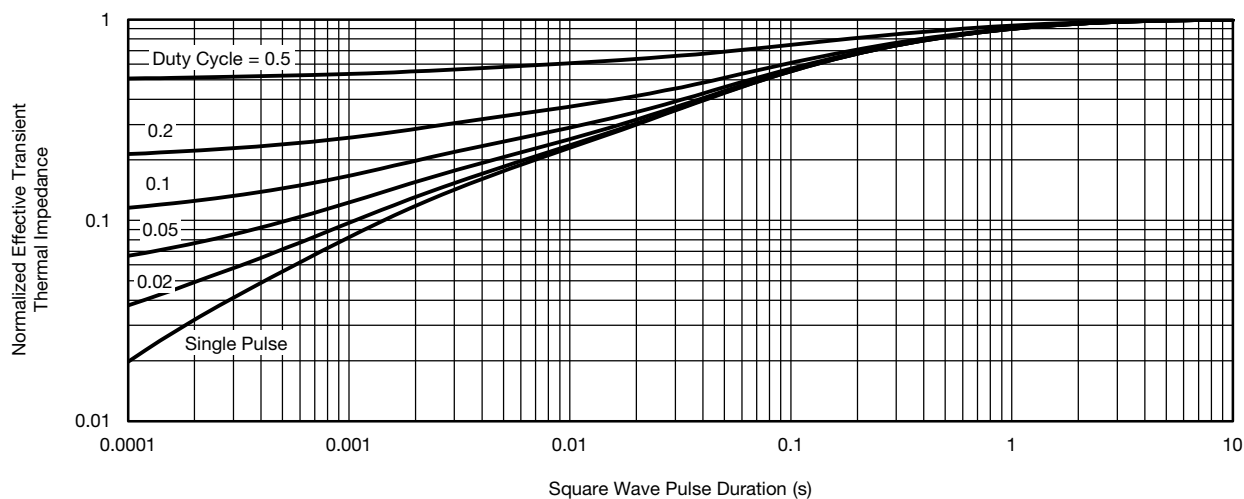
Power Derating, Junction-to-Foot

* The power dissipation P_D is based on $T_{J(max.)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

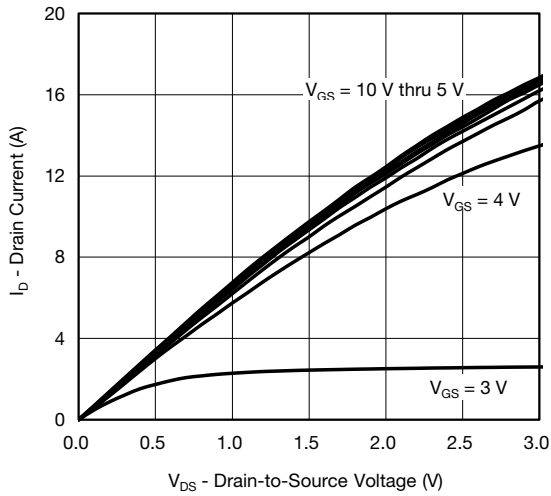


Normalized Thermal Transient Impedance, Junction-to-Ambient

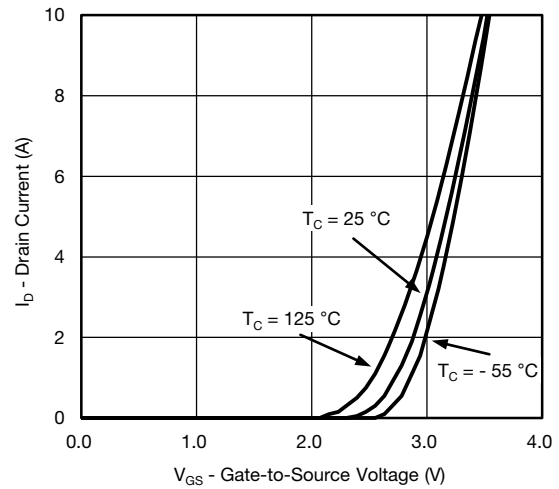


Normalized Thermal Transient Impedance, Junction-to-Foot

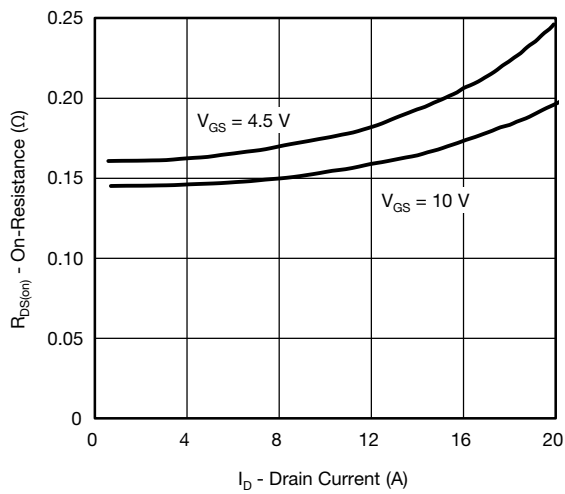
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



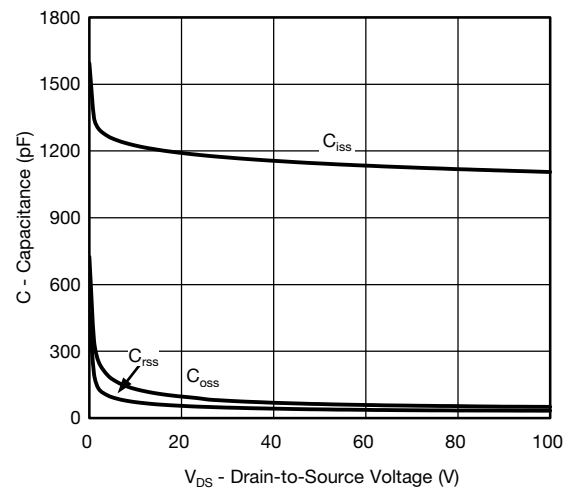
Output Characteristics



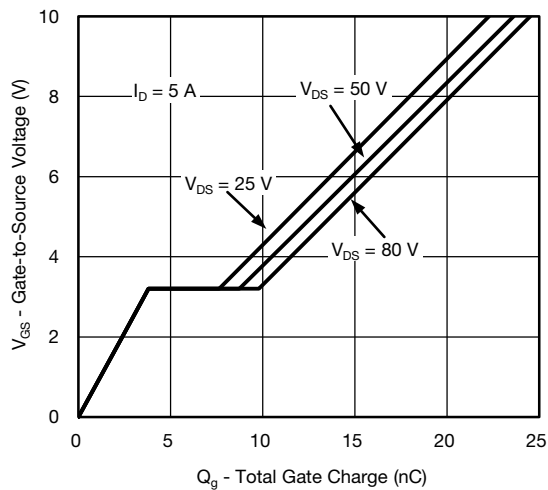
Transfer Characteristics



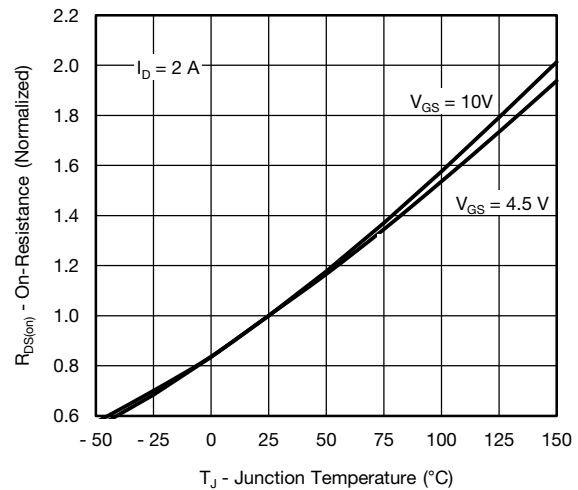
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

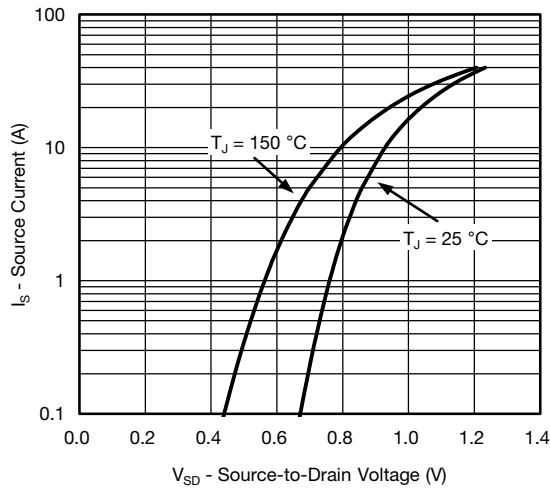


Gate Charge

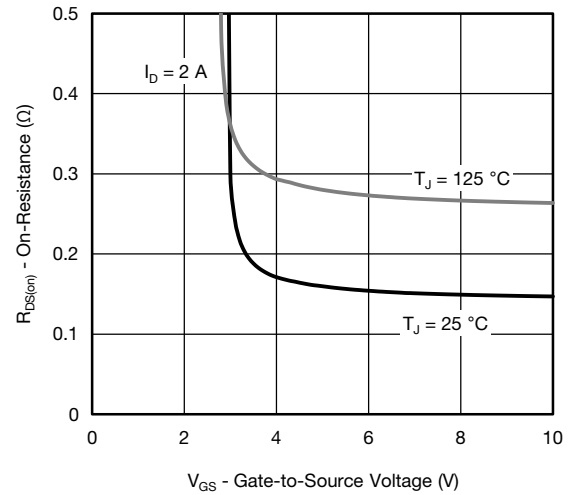


On-Resistance vs. Junction Temperature

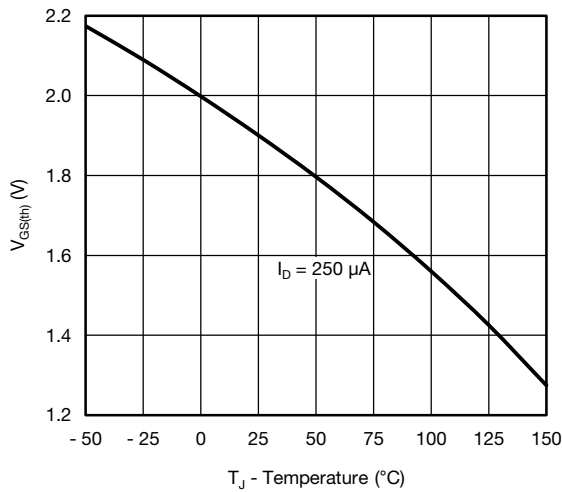
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, (unless otherwise noted)



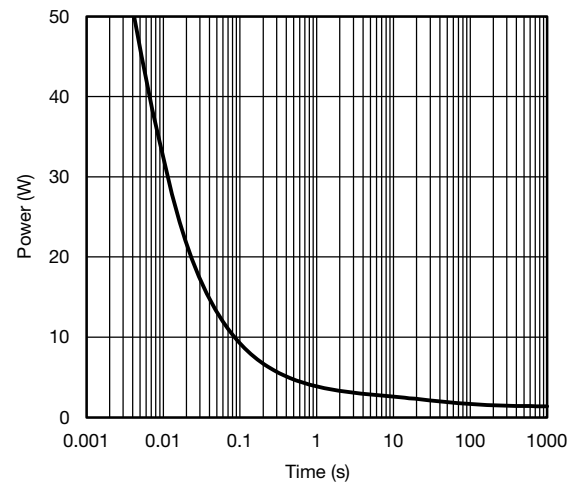
Source-Drain Diode Forward Voltage



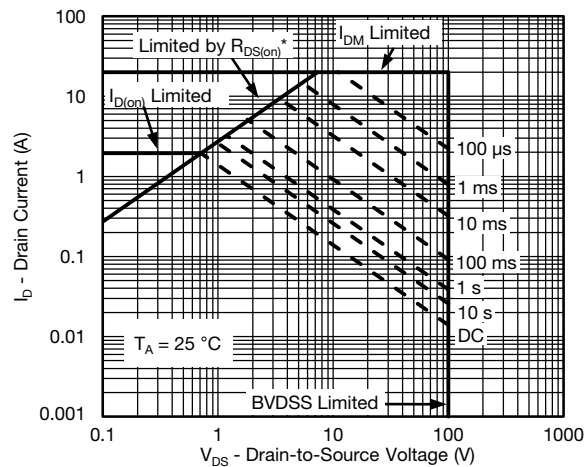
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

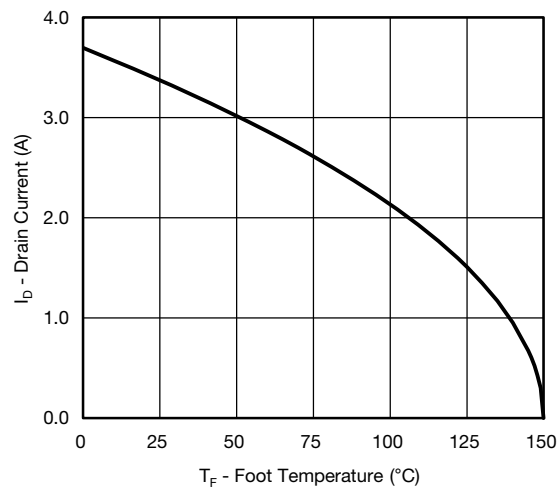


Single Pulse Power, Junction-to-Ambient

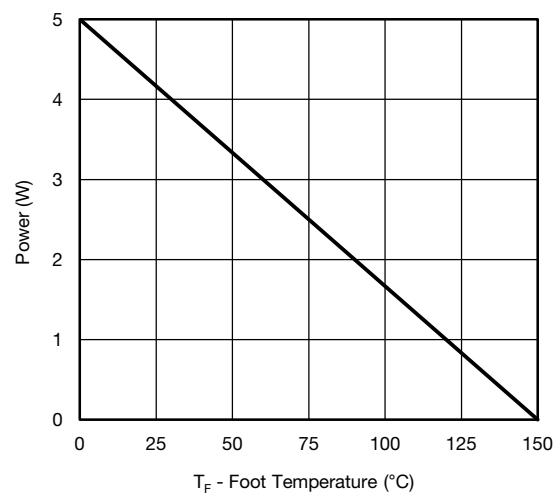


Safe Operating Area, Junction-to-Ambient

P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



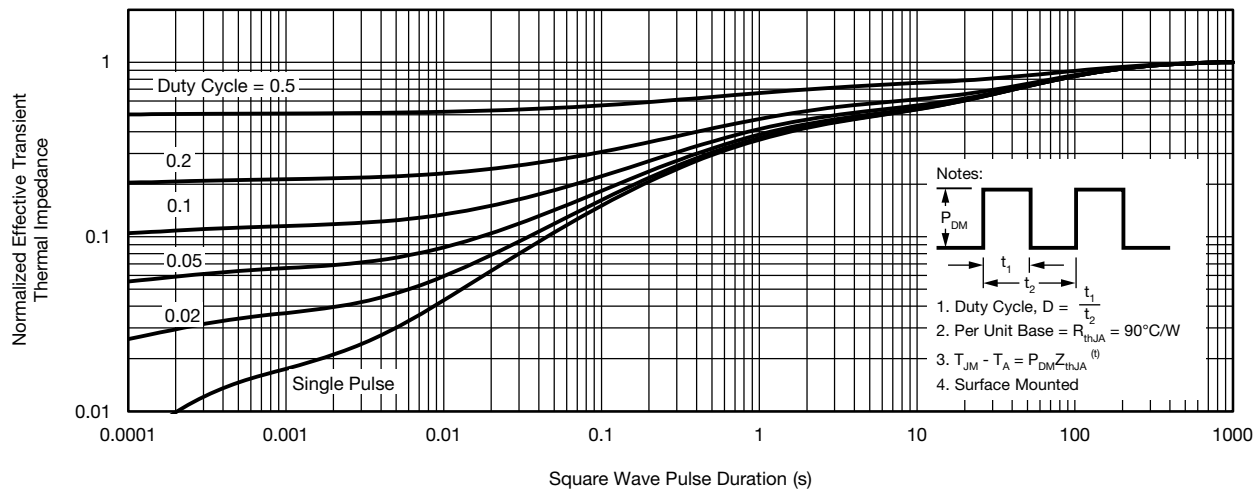
Current Derating*



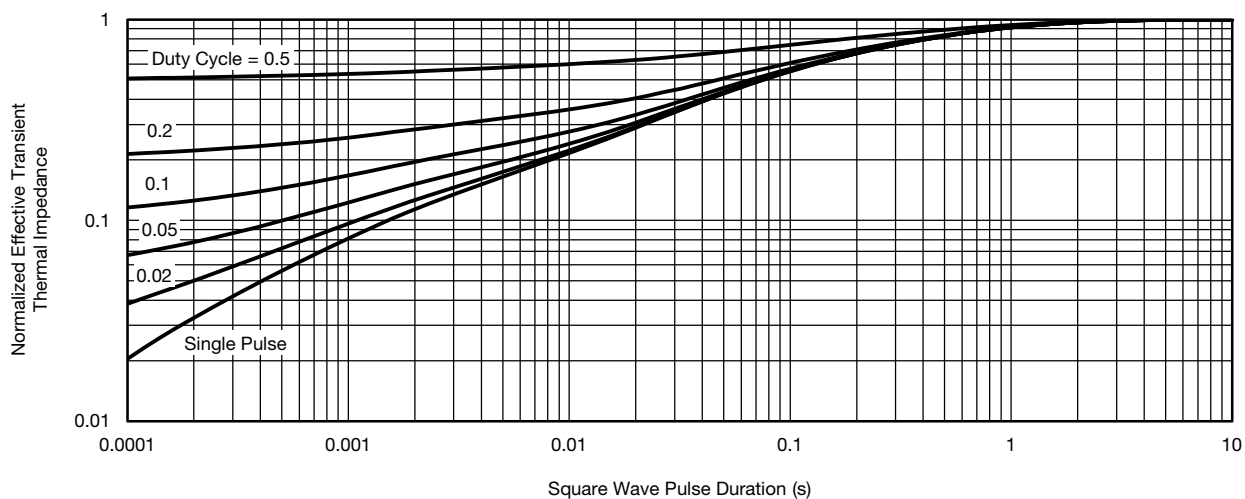
Power Derating, Junction-to-Foot

* The power dissipation P_D is based on $T_{J(max.)} = 150\text{ }^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

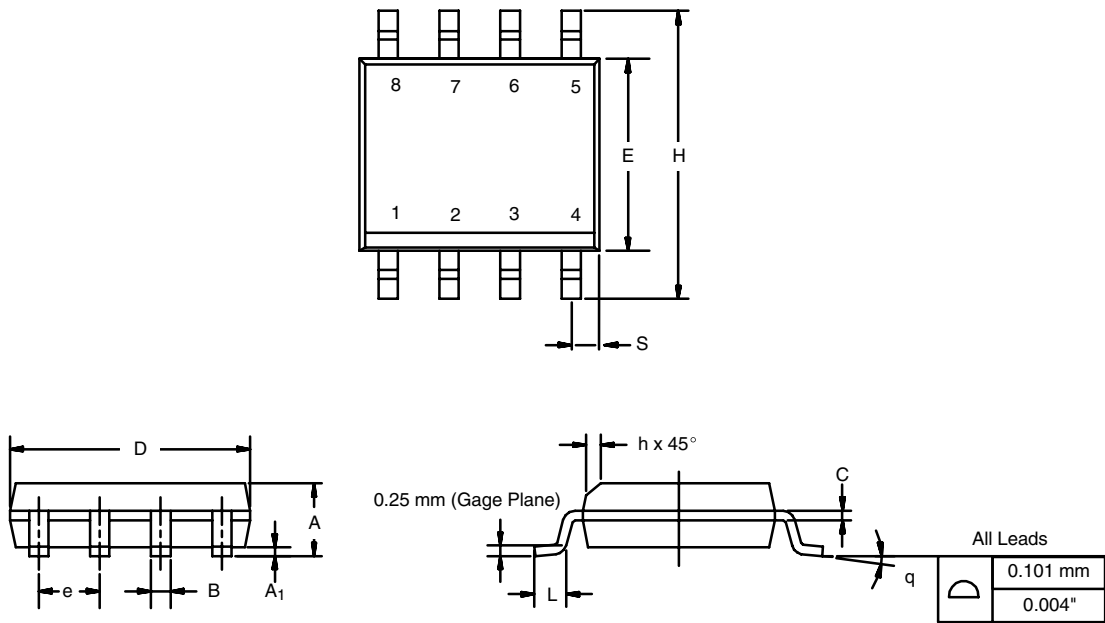


Normalized Thermal Transient Impedance, Junction-to-Ambient



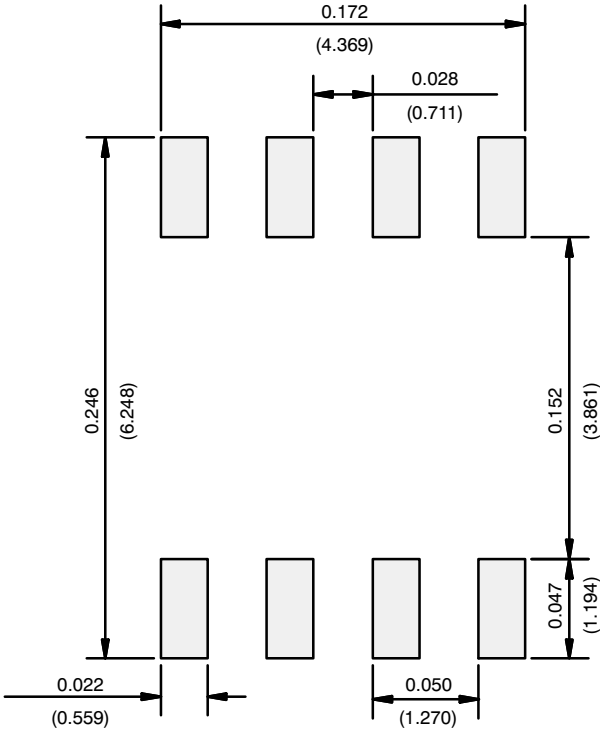
Normalized Thermal Transient Impedance, Junction-to-Foot

SOIC (NARROW): 8-LEAD
JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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All products due to improve reliability, function or design or for other reasons, product specifications and data are subject to change without notice.

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Taiwan VBsemi Electronics Co., Ltd. hereby certify that all of its products comply identified as halogen-free halogen-free standards required by the JEDEC JS709A. Please note that some Taiwanese VBsemi documents still refer to the definition of IEC 61249-2-21, and we are sure that all products conform to confirm compliance with IEC 61249-2-21 standard level JS709A.