

MDS5753ERH-VB Datasheet Dual N-Channel 30 V (D-S) MOSFET

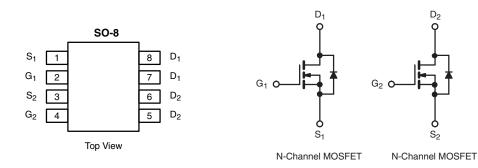
PRODUCT SUMMARY						
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)			
30	0.016 at V _{GS} = 10 V	8.5	7.1			
30	0.020 at V _{GS} = 4.5 V	7.6	7.1			

FEATURES

- Trench Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC

APPLICATIONS

- Notebook System Power
- Low Current DC/DC



ABSOLUTE MAXIMUM RATINGS (T _A =	25 °C, unless othe	rwise noted)		
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	30	V	
Gate-Source Voltage	V _{GS}	± 20		
	T _C = 25 °C		8.5	
Continuous Drain Current (T ₁ = 150 °C)	T _C = 70 °C	1_	7.5	1
Continuous Drain Current (1) = 150°C)	T _A = 25 °C	I _D	7.2 ^{b, c}	1
	T _A = 70 °C		5.9 ^{b, c}	1
Pulsed Drain Current	I _{DM}	30	A	
Source-Drain Current Diode Current	T _C = 25 °C	L.	2.8	
Source-Drain Guiterit Diode Guiterit	T _A = 25 °C	I _S	1.8 ^{b, c}	1
Pulsed Source-Drain Current	I _{SM}	30		
Single Pulse Avalanche Current		I _{AS}	10	
Single Pulse Avalanche Energy	L = 0.1 mH	E _{AS}	5	-
	T _C = 25 °C		3.1	
Maximum Dawar Discinction	T _C = 70 °C	Pn	2.0	w
Maximum Power Dissipation	T _A = 25 °C	' D	2.0 ^{b, c}	~ ~ ~
	T _A = 70 °C		1.25 ^{b, c}	1
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Тур.	Max.	Unit		
Maximum Junction-to-Ambient ^{b, d}	t ≤ 10 s	R _{thJA}	52	62.5	°C/W		
Maximum Junction-to-Foot (Drain)	Steady-State	R _{thJF}	30	40	0/11		

Notes:

a. Based on T_C = 25 °C.

b. Surface mounted on 1" x 1" FR4 board.

b. Surface c. t = 10 s.

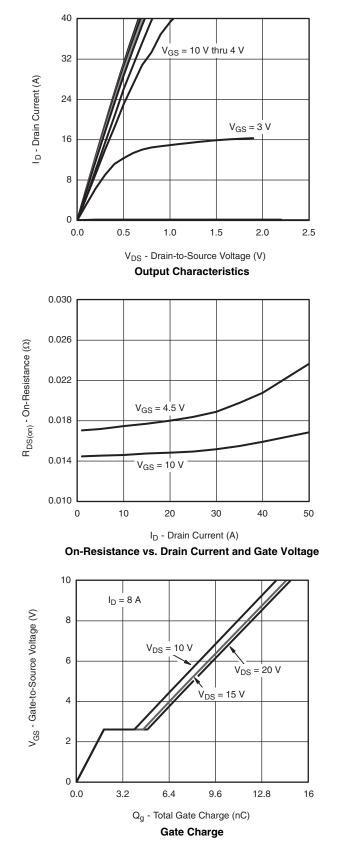
d. Maximum under steady state conditions is 110 °C/W.

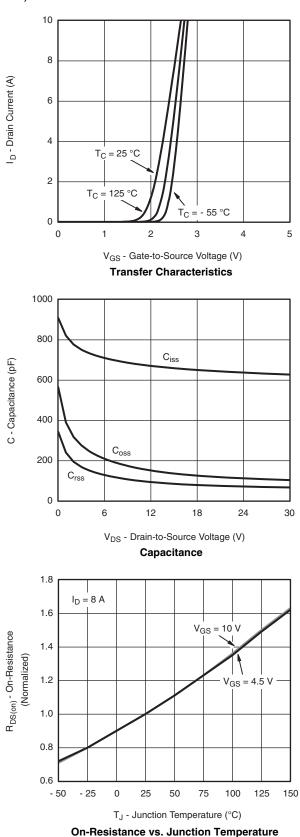


SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static		·		•			
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = 250 \mu\text{A}$	30			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = 250 μA		3.0		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$GS(th)/T_J$ $I_D = 250 \mu A$		- 5.2		mv/°C	
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	1.2		2.5	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			100	nA	
Zara Cata Valtaga Drain Current	lana	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$		1			
Zero Gate Voltage Drain Current	IDSS	$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ TJ} = 55 ^{\circ}\text{C}$			10	μΑ	
On -State Drain Current ^b	I _{D(on)}	$V_{DS} = 5 V, V_{GS} = 10 V$	20			А	
	Б	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 8 \text{ A}$		0.016		Ω	
Drain-Source On-State Resistance ^D	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 5 A		0.020			
Forward Transconductance ^b	9 _{fs}	V _{DS} = 15 V, I _D = 8 A		27		S	
Dynamic ^a	•	·		•			
Input Capacitance	C _{iss}			660			
Output Capacitance	C _{oss}	$V_{DS} = 15 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ I}_{D} = 1 \text{ MHz}$		140		pF	
Reverse Transfer Capacitance	C _{rss}			86			
Total Gate Charge	0	$V_{DS} = 15 \text{ V}, \text{ V}_{GS} = 10 \text{ V}, \text{ I}_{D} = 8 \text{ A}$		14.5	22		
	Q _g			7.1	11		
Gate-Source Charge	Q _{gs}	V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 8 A		1.9			
Gate-Drain Charge	Q _{gd}			2.7			
Gate Resistance	Rg	f = 1 MHz	0.5	2.6	5.2	Ω	
Turn-On Delay Time	t _{d(on)}			14	28		
Rise Time	t _r	V_{DD} = 15 V, R_L = 3 Ω		45	80		
Turn-Off Delay Time	t _{d(off)}	$\text{I}_\text{D} \cong \text{5}$ A, V_GEN = 4.5 V, R_g = 1 Ω		18	35		
Fall Time	t _f			12	24	20	
Turn-On Delay Time	t _{d(on)}			7	14	- ns -	
Rise Time	t _r	V_{DD} = 15 V, R_L = 3 Ω		10	20		
Turn-Off Delay Time	t _{d(off)}	$\text{I}_\text{D} \cong \text{5 A}, \text{ V}_\text{GEN} = \text{10 V}, \text{ R}_\text{g} = \text{1 } \Omega$		15	30		
Fall Time	t _f			7	14		
Drain-Source Body Diode Characteristi	cs	·		•			
Continuous Source-Drain Diode Current	۱ _S	$T_{C} = 25 \ ^{\circ}C$			2.8		
Pulse Diode Forward Current ^a	I _{SM}	M			30	A	
Body Diode Voltage	V _{SD}	I _S = 2 A		0.77	1.1	V	
Body Diode Reverse Recovery Time	t _{rr}			17	34	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	1 = 5.0 dt/dt = 100.0 dt/dt = 25.00		9	18	nC	
Reverse Recovery Fall Time	t _a	IE = 3 A. U/UI = 100 A/US. II = 23 U		10			
Reverse Recovery Rise Time	t _b			7		nS nS	
	•			•			

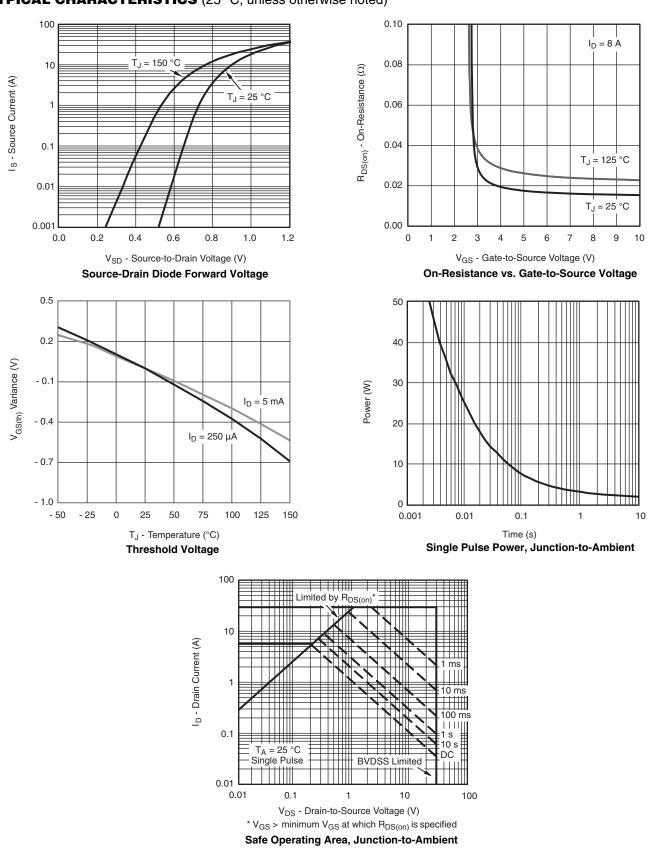
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



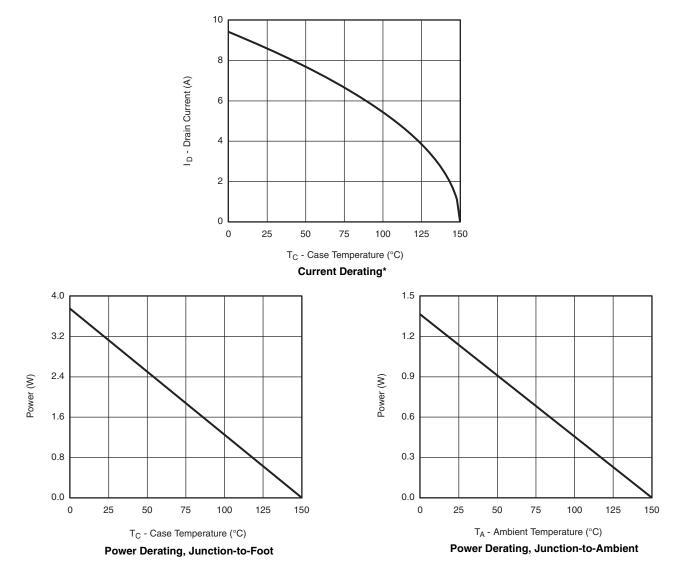






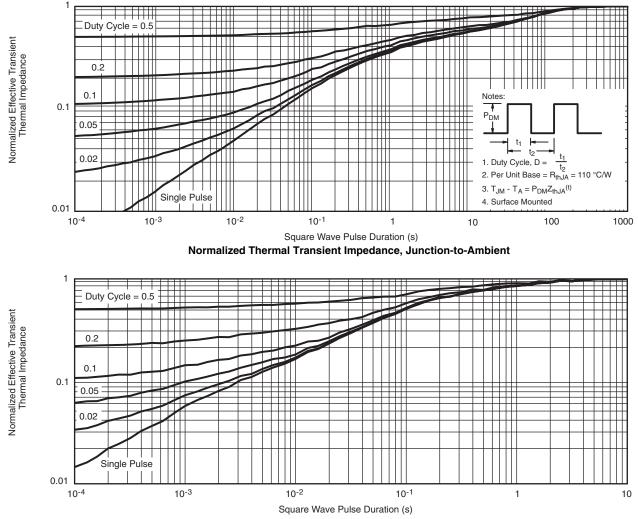






* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

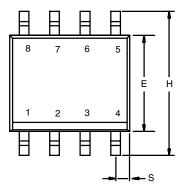


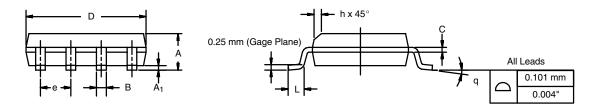


Normalized Thermal Transient Impedance, Junction-to-Foot



SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012

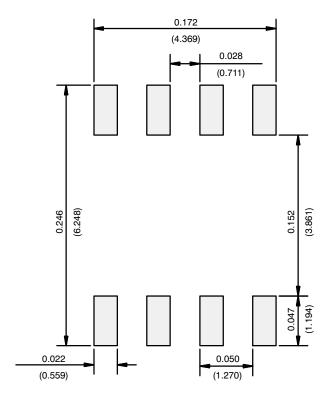




	MILLIM	IETERS	INCHES		
DIM	Min	Мах	Min	Мах	
A	1.35	1.75	0.053	0.069	
A ₁	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
E	3.80	4.00	0.150	0.157	
е	1.27 BSC		0.050 BSC		
н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498					



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)



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