

IRF7468TRPBF-VB Datasheet N-Channel 40-V (D-S) MOSFET

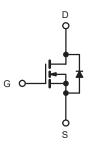
PRODUCT SUMMARY						
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^d	Q _g (Typ.)			
40	0.014 at V _{GS} = 10 V	10	15 nC			
40	0.016 at V _{GS} = 4.5 V	9	13110			

FEATURES

- Halogen-free According to IEC 61249-2-21
 Definition
- Trench Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS directive 2002/95/EC

APPLICATIONS

- Synchronous Rectification
- POL, IBC
 - Secondary Side



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted						
Parameter	Symbol	Limit	Unit			
Drain-Source Voltage		V _{DS}	40	V		
Gate-Source Voltage		V _{GS}	± 20	v		
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C T _C = 70 °C	I _D	10 8			
	T _A = 25 °C T _A = 70 °C		10.4 ^{a, b} 8.8 ^{a, b}	Α		
Pulsed Drain Current		I _{DM}	50			
Avalanche Current	L = 0.1 mH	I _{AS}	15			
Avalanche Energy	L = 0.1 mm	E _{AS}	11	mJ		
Continuous Source-Drain Diode Current	T _C = 25 °C T _A = 25 °C	- I _S	5 2.1 ^{a, b}	Α		
Maximum Power Dissipation	$T_{C} = 25 °C$ $T_{C} = 70 °C$ $T_{A} = 25 °C$	PD	6 3.8 2.5 ^{a, b}	w		
$T_{A} = 70 °C$ Operating Junction and Storage Temperature Range		TJ, Tstg	1.6 ^{a, b} - 55 to 150	°C		

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient ^{a, c}	t ≤ 10 s	R _{thJA}	37	50	°C/W		
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	17	21	0,11		

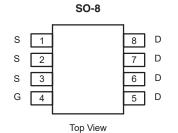
Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. t = 10 s.

c. Maximum under Steady State conditions is 85 °C/W.

d. Based on T_C = 25 °C.



SPECIFICATIONS $T_J = 25 \text{ °C}$, Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static	Cymbol			Typ.	max.	Unit	
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	40			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$			40		- mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA		- 6			
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1	-	3	V	
Gate-Source Leakage		$V_{DS} = 0 V, V_{GS} = \pm 20 V$	-		± 100	nA	
g-	000	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$			1		
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 40 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 55 ^{\circ}\text{C}$			5	μA	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 V, V_{GS} = 10 V$	50			А	
		$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 12.4 \text{ A}$		0.014		+	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 10.8 A		0.016		Ω	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 12.4 A		56		S	
Dynamic ^b					1		
Input Capacitance	C _{iss}			2000		pF	
Output Capacitance	C _{oss}	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz		260			
Reverse Transfer Capacitance	C _{rss}			150			
	$V_{DS} = 10 \text{ V}, \text{ V}_{CS} = 10 \text{ V}, \text{ I}_{D} = 10 \text{ V}$	V _{DS} = 10 V, V _{GS} = 10 V, I _D = 12.4 A		33	50	nC	
Total Gate Charge				15	23		
Gate-Source Charge	Q _{gs}	V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 12.4 A		6.7			
Gate-Drain Charge	Q _{gd}			5.1			
Gate Resistance	R _g	f = 1 MHz		1.4	2.1	Ω	
Turn-On Delay Time	t _{d(on)}			25	40		
Rise Time	t _r	V_{DD} = 20 V, R _L = 2 Ω		12	20		
Turn-Off Delay Time	t _{d(off)}	${ m I}_{ m D}\cong$ 10 A, ${ m V}_{ m GEN}$ = 4.5 V, ${ m R}_{ m g}$ = 1 Ω		25	40		
Fall Time	t _f			10	15		
Turn-On Delay Time	t _{d(on)}			10	15	ns	
Rise Time	t _r	V_{DD} = 20 V, R _L = 2 Ω		15	25	-	
Turn-Off Delay Time	t _{d(off)}	$\text{I}_\text{D}\cong$ 10 A, V_GEN = 10 V, Rg = 1 Ω		30	45		
Fall Time	t _f			10	15		
Drain-Source Body Diode Characteristi	cs						
Continuous Source-Drain Diode Current	۱ _S	T _C = 25 °C			30	A	
Pulse Diode Forward Current	I _{SM}				50	А	
Body Diode Voltage	V _{SD}	I _S = 10 A, V _{GS} = 0 V		0.8	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			30	60	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	I _F = 10 A, dl/dt = 100 A/μs, T _{.I} = 25 °C		26	52	nC	
Reverse Recovery Fall Time	t _a	$_{1}$ $_{10}$		17.5		ne	
Reverse Recovery Rise Time	t _b			12.5		ns	

Notes:

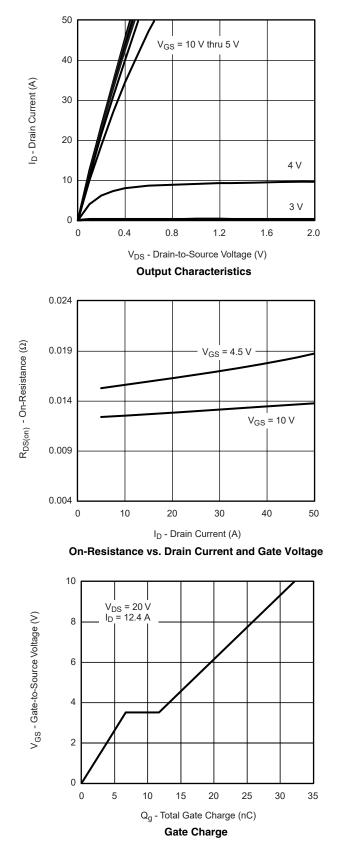
a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%$

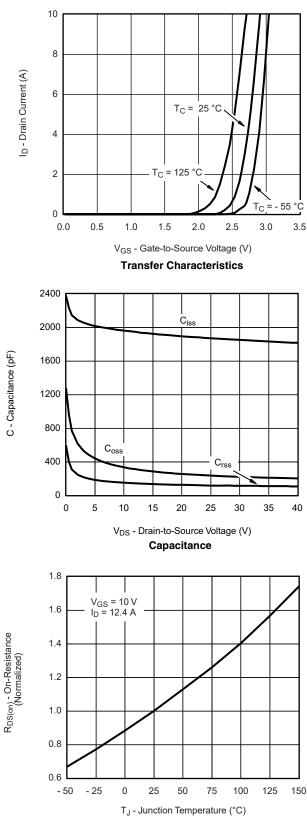
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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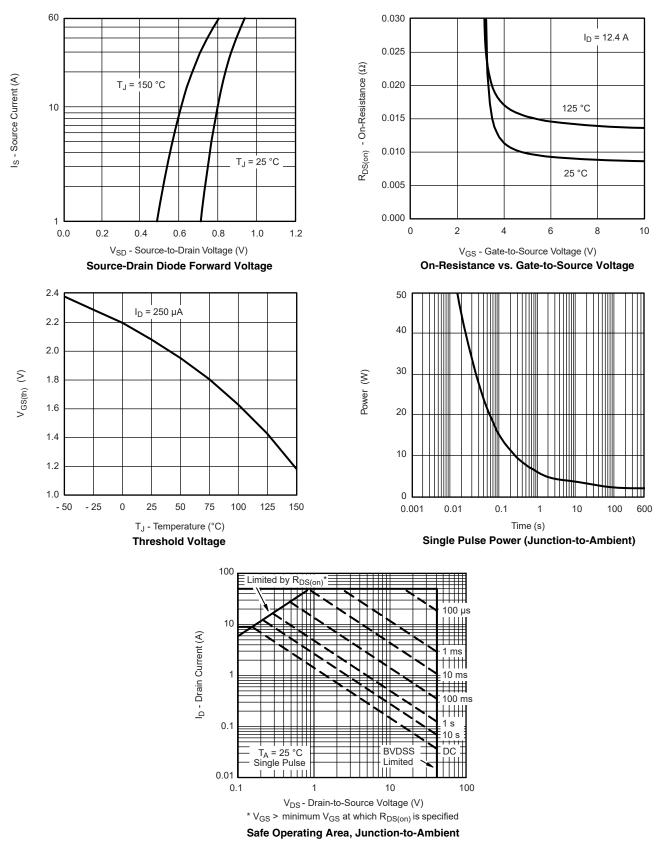




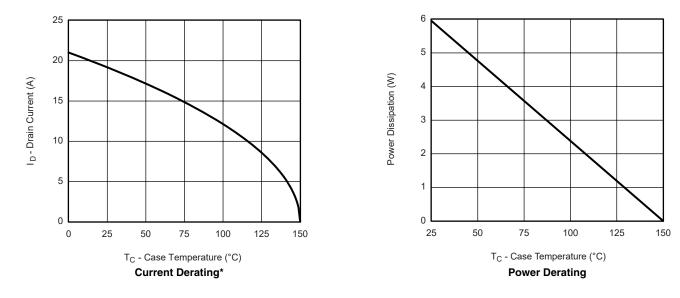


On-Resistance vs. Junction Temperature



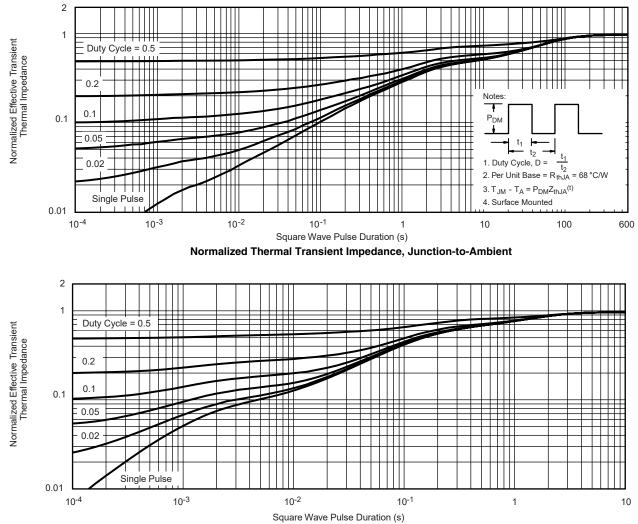






* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



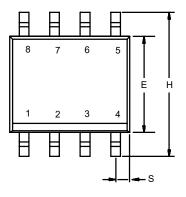


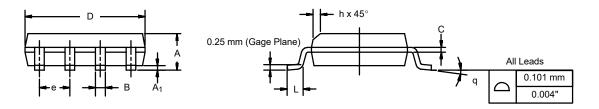
Normalized Thermal Transient Impedance, Junction-to-Foot



SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012

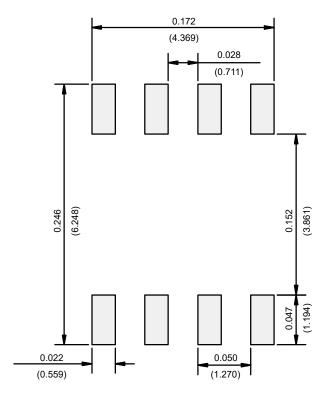




	MILLIM	IETERS	INCHES		
DIM	Min	Мах	Min	Max	
A	1.35	1.75	0.053	0.069	
A ₁	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
E	3.80	4.00	0.150	0.157	
е	1.27	BSC	0.050 BSC		
Н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498					



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)



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