

# FDS6689S-NL-VB Datasheet N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY						
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)			
30	0.004 at V <sub>GS</sub> = 10 V	18	6.8 nC			
30	0.005 at V <sub>GS</sub> = 4.5 V	16	0.0110			

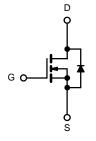
**SO-8** 

#### **FEATURES**

- · Halogen-free
- Trench Power MOSFET
- Optimized for High-Side Synchronous Rectifier Operation
- 100 % R<sub>g</sub> Tested
- 100 % UIS Tested

#### **APPLICATIONS**

- Notebook CPU Core
  - High-Side Switch



N-Channel MOSFET

S <u>1</u>		8	D
S 2		7	D
S 3		6	D
G 4		5	D
	Top View		

Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	V <sub>DS</sub>	30	\ /		
Gate-Source Voltage		$V_{GS}$	± 20	V	
	T <sub>C</sub> = 25 °C		18		
Continuous Drain Current (T. – 150 °C)	T <sub>C</sub> = 70 °C		16		
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>A</sub> = 25 °C	I <sub>D</sub>	15 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C		13 <sup>b, c</sup>	^	
Pulsed Drain Current		I <sub>DM</sub>	50	A	
Continuous Course Davis Diode Coursest	T <sub>C</sub> = 25 °C		3.8		
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	2.1 <sup>b, c</sup>		
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	22		
Avalanche Energy	L = 0.1 IIII	E <sub>AS</sub>	24	mJ	
	T <sub>C</sub> = 25 °C		4.5		
Marianan Barran Disaination	T <sub>C</sub> = 70 °C	В	2.8	10/	
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	2.5 <sup>b, c</sup>	W	
	T <sub>A</sub> = 70 °C		1.6 <sup>b, c</sup>		
Operating Junction and Storage Temperature Ra	T <sub>J</sub> , T <sub>stq</sub>	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>b, d</sup>	t ≤ 10 s	R <sub>thJA</sub>	38	50	°C/W	
Maximum Junction-to-Foot (Drain)	Steady State	R <sub>thJF</sub>	22	28	C/VV	

#### Notes:

- a. Base on  $T_C = 25$  °C.
- b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. Maximum under Steady State conditions is 85 °C/W.



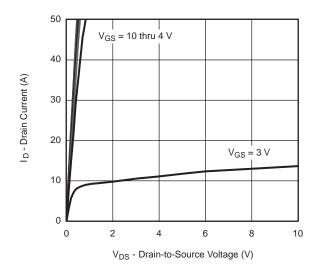
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static	1 1			, ,,		<u> </u>	
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V, } I_{D} = 250  \mu\text{A}$	30			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	J 250A		28		mV/°C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA		- 6			
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.0		3.0	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
7 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			1	μΑ	
Zero Gate Voltage Drain Current	IDSS	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 \text{ °C}$			10		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	20			Α	
	_	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 11 A	0.004			1	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A		0.005		Ω	
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 11 A		52		S	
Dynamic <sup>b</sup>	<u> </u>			1			
Input Capacitance	C <sub>iss</sub>			820			
Output Capacitance	C <sub>oss</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz		195		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>			73			
Total Gate Charge	Qg	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 11 A		15	23	nC	
				6.8	10.2		
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 5 \text{ V}, I_{D} = 11 \text{ A}$		2.5			
Gate-Drain Charge	Q <sub>gd</sub>			2.3			
Gate Resistance	R <sub>g</sub>	f = 1 MHz	0.36	1.8	3.6	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			16	24		
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 1.4 $\Omega$		12	18		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 9 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		16	24		
Fall Time	t <sub>f</sub>			10	20	ns	
Turn-On Delay Time	t <sub>d(on)</sub>			8	16	113	
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 1.4 $\Omega$		10	20		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 9 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		16	24		
Fall Time	t <sub>f</sub>			8	15		
<b>Drain-Source Body Diode Characteris</b>	ics						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			25	Α	
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				50		
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 9 A		0.8	1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			15	30	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> = 9 A, dl/dt = 100 A/μs, T <sub>J</sub> = 25 °C		6	12	nC	
Reverse Recovery Fall Time	t <sub>a</sub>	i <sub>F</sub> = 0 Λ, αιναι = 100 Λ/μο, 1 <sub>J</sub> = 20 0		8		nc	
Reverse Recovery Rise Time	t <sub>b</sub>			7		ns	

#### Notes

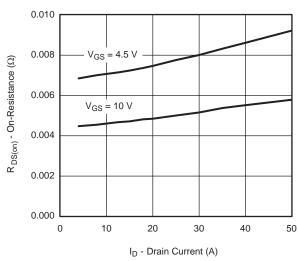
- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

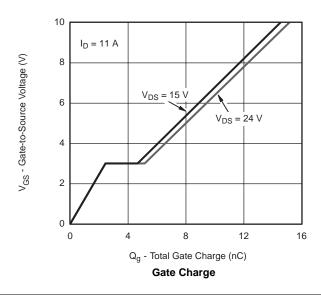




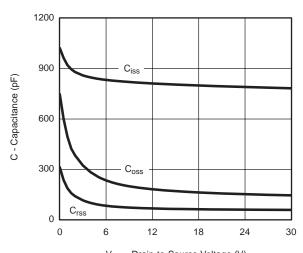
#### **Output Characteristics**



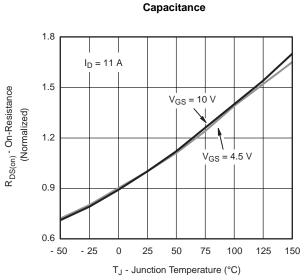
#### On-Resistance vs. Drain Current and Gate Voltage



V<sub>GS</sub> - Gate-to-Source Voltage (V) **Transfer Characteristics** 

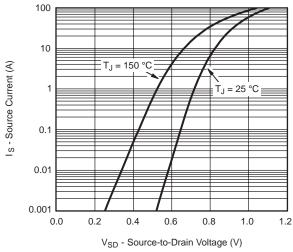


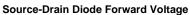
V<sub>DS</sub> - Drain-to-Source Voltage (V)

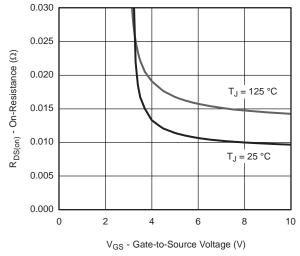


On-Resistance vs. Junction Temperature

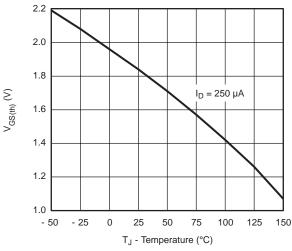




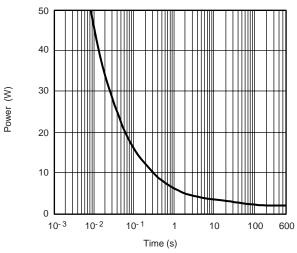




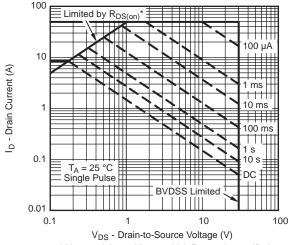
On-Resistance vs. Gate-to-Source Voltage



**Threshold Voltage** 



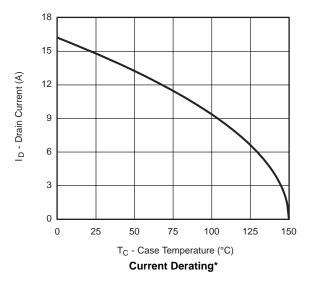
Single Pulse Power, Junction-to-Ambient

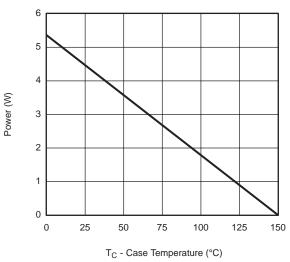


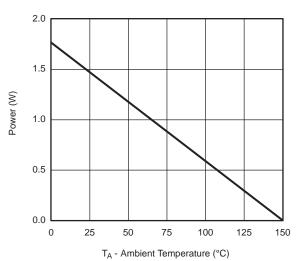
\*  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

Safe Operating Area, Junction-to-Ambient







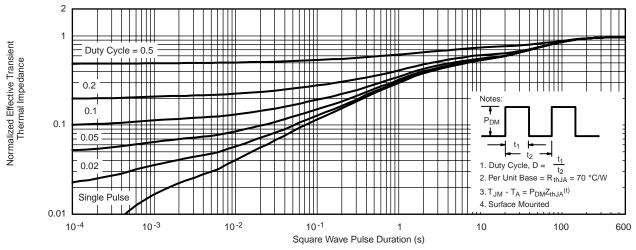


Power Derating, Junction-to-Foot

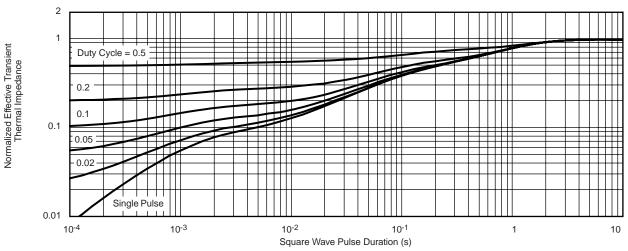
Power Derating, Junction-to-Ambient

<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max)}$  = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





#### Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot



**SOIC (NARROW): 8-LEAD**JEDEC Part Number: MS-012







	MILLIM	IETERS	INC	HES	
DIM	Min	Max	Min	Max	
Α	1.35	1.75	0.053	0.069	
A <sub>1</sub>	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
E	3.80	4.00	0.150	0.157	
е	1.27	1.27 BSC		) BSC	
Н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
FCN: C-06527-Rev I 11-Sep-06					

ECN: C-06527-Rev. I, 11-Sep-06

DWG: 5498



#### **RECOMMENDED MINIMUM PADS FOR SO-8**



Recommended Minimum Pads Dimensions in Inches/(mm)



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