

FDS3512-NL-VB Datasheet

N-Channel 100 V (D-S) MOSFET



RoHS
COMPLIANT
HALOGEN
FREE
Available

| PRODUCT SUMMARY | | |
|-------------------------------------|--------|-----------|
| V_{DS} | 100 | V |
| $R_{DS(on)}$ $V_{GS} = 10\text{ V}$ | 32 | $m\Omega$ |
| I_D | 9 | A |
| Configuration | Single | |

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Extremely Low Q_{gd} for Switching Losses
- 100 % R_g Tested
- 100 % Avalanche Tested
- Compliant to RoHS Directive 2002/95/EC

APPLICATIONS

- Primary Side Switch



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

| Parameter | Symbol | Limit | Unit |
|--|----------------|------------------------------------|---------------------|
| Drain-Source Voltage | V_{DS} | 100 | V |
| Gate-Source Voltage | V_{GS} | ± 20 | |
| Continuous Drain Current ($T_J = 150\text{ }^{\circ}\text{C}$) | I_D | $T_C = 25\text{ }^{\circ}\text{C}$ | 9 |
| | | $T_C = 70\text{ }^{\circ}\text{C}$ | 6 |
| | | $T_A = 25\text{ }^{\circ}\text{C}$ | 6 ^{b, c} |
| | | $T_A = 70\text{ }^{\circ}\text{C}$ | 5 ^{b, c} |
| Pulsed Drain Current | I_{DM} | 40 | A |
| Continuous Source-Drain Diode Current | I_S | $T_C = 25\text{ }^{\circ}\text{C}$ | 7 |
| | | $T_A = 25\text{ }^{\circ}\text{C}$ | 3.8 ^{b, c} |
| Single Pulse Avalanche Current | I_{AS} | 30 | |
| Single Pulse Avalanche Energy | E_{AS} | 112 | mJ |
| Maximum Power Dissipation | P_D | $T_C = 25\text{ }^{\circ}\text{C}$ | 14 |
| | | $T_C = 70\text{ }^{\circ}\text{C}$ | 5 |
| | | $T_A = 25\text{ }^{\circ}\text{C}$ | 4 ^{b, c} |
| | | $T_A = 70\text{ }^{\circ}\text{C}$ | 2 ^{b, c} |
| Operating Junction and Storage Temperature Range | T_J, T_{stg} | - 55 to 150 | $^{\circ}\text{C}$ |

THERMAL RESISTANCE RATINGS

| Parameter | Symbol | Typical | Maximum | Unit |
|---|------------|---------|---------|----------------------|
| Maximum Junction-to-Ambient ^{b, f} | R_{thJA} | 33 | 40 | $^{\circ}\text{C/W}$ |
| Maximum Junction-to-Foot (Drain) | R_{thJF} | 17 | 21 | |

Notes:

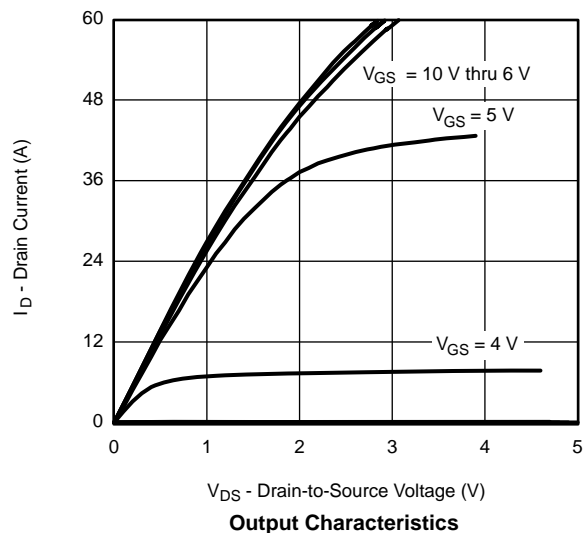
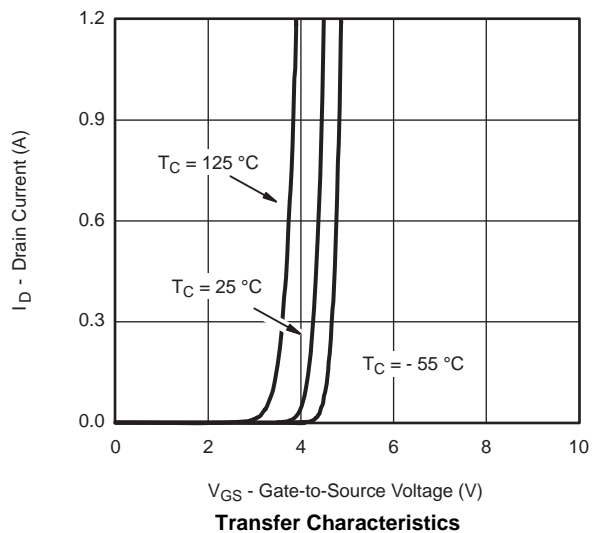
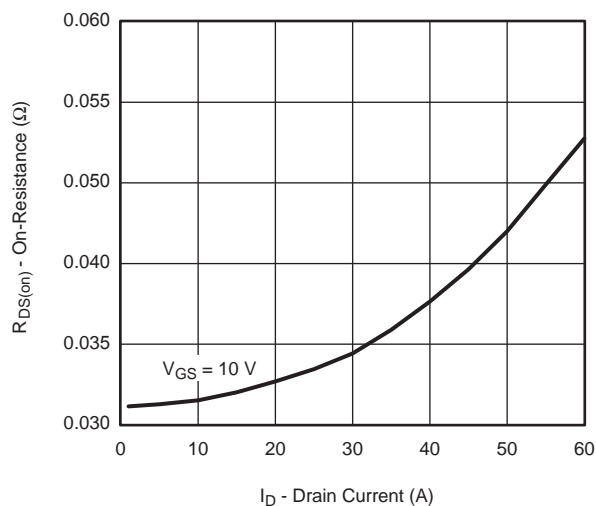
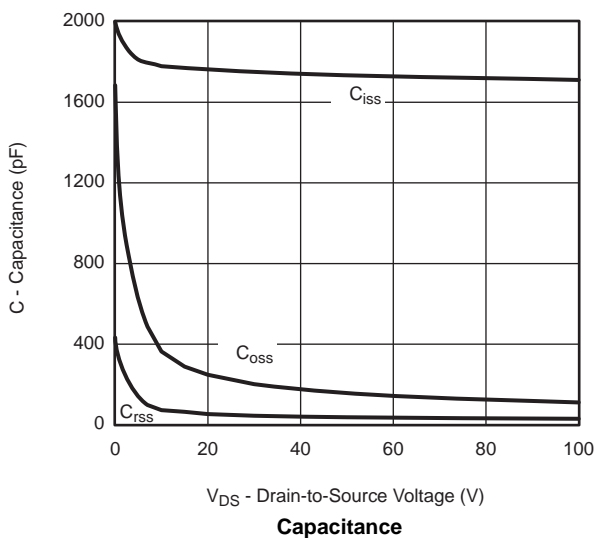
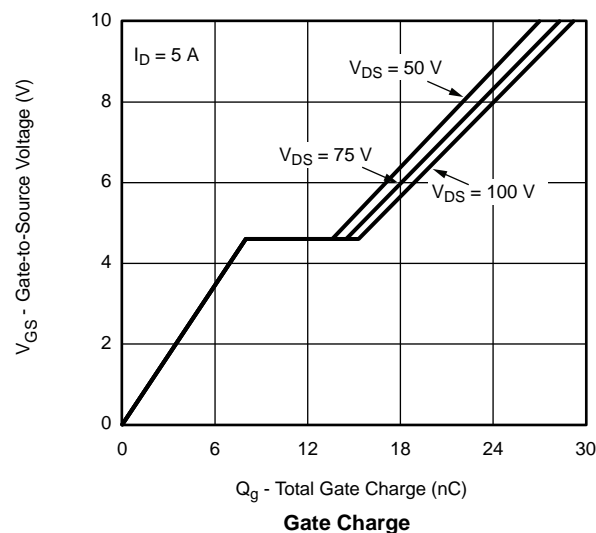
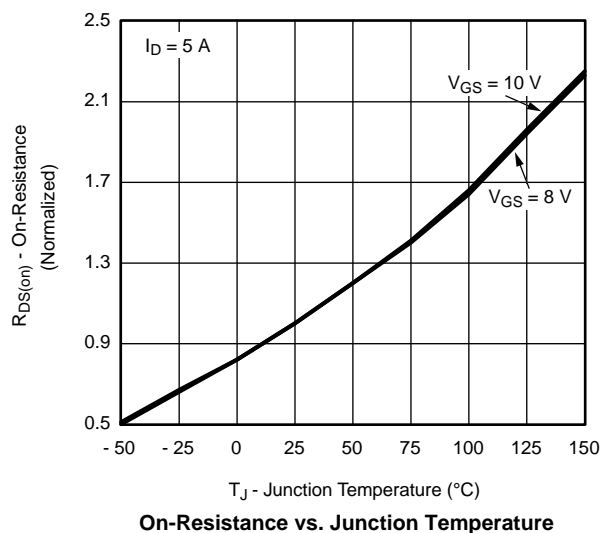
- Based on $T_C = 25\text{ }^{\circ}\text{C}$.
- Surface mounted on 1" x 1" FR4 board.
- $t = 10\text{ s}$.
- Maximum under steady state conditions is 80 $^{\circ}\text{C/W}$.

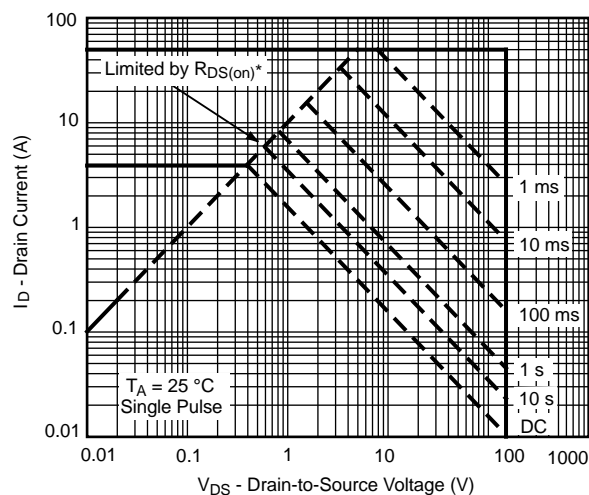
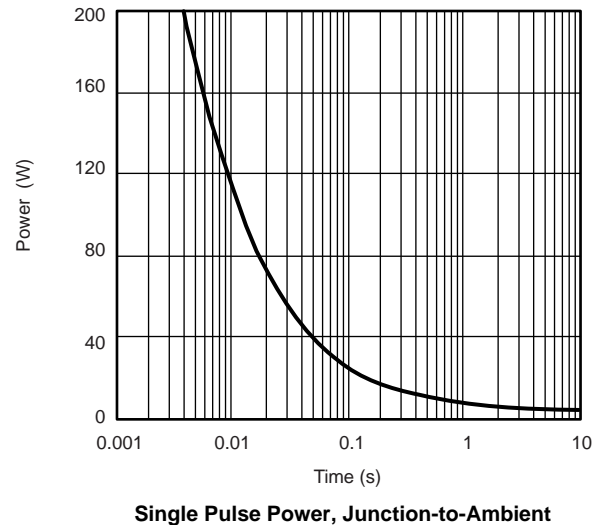
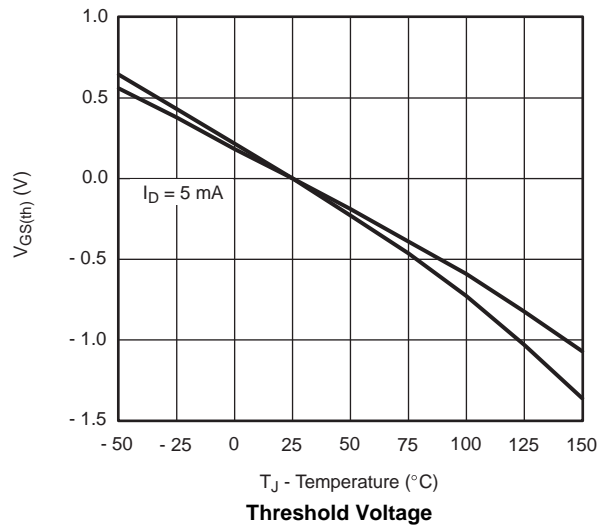
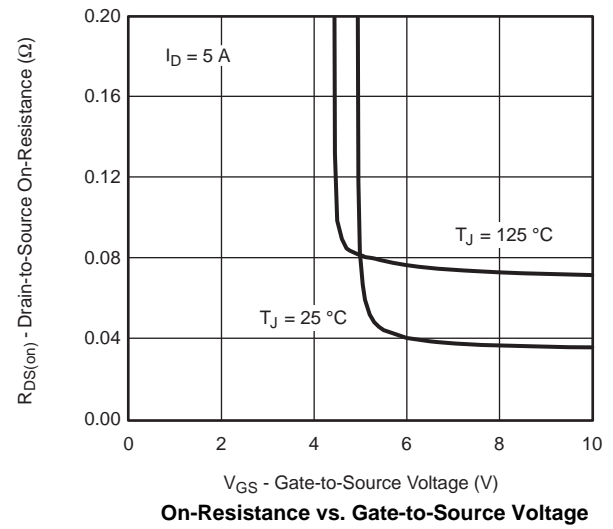
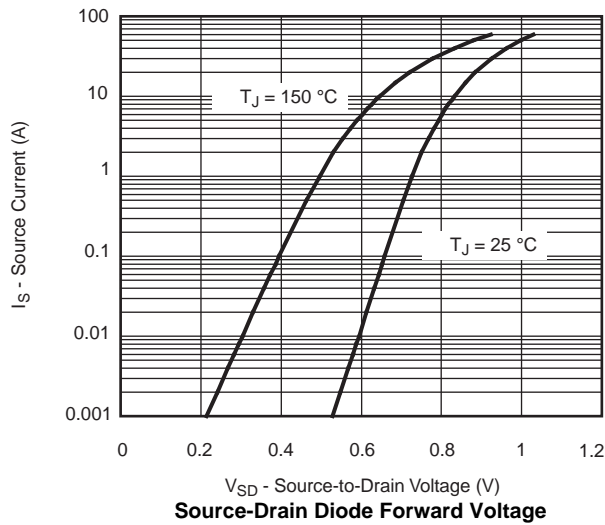
| SPECIFICATIONS (T _J = 25 °C, unless otherwise noted) | | | | | | |
|---|--------------------------------------|--|------|------|-------|-------|
| Parameter | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
| Static | | | | | | |
| Drain-Source Breakdown Voltage | V _{DS} | V _{GS} = 0 V, I _D = 250 μA | 100 | | | V |
| V _{DS} Temperature Coefficient | ΔV _{DS} /T _J | I _D = 250 μA | | 172 | | mV/°C |
| V _{GS(th)} Temperature Coefficient | ΔV _{GS(th)} /T _J | | | - 10 | | |
| Gate-Source Threshold Voltage | V _{GS(th)} | V _{DS} = V _{GS} , I _D = 250 μA | 1.0 | | 3.0 | V |
| Gate-Source Leakage | I _{GSS} | V _{DS} = 0 V, V _{GS} = ± 20 V | | | ± 100 | nA |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{DS} = 100 V, V _{GS} = 0 V | | | 1 | μA |
| | | V _{DS} = 100 V, V _{GS} = 0 V, T _J = 55 °C | | | 10 | |
| On-State Drain Current ^a | I _{D(on)} | V _{DS} ≥ 10 V, V _{GS} = 10 V | 30 | | | A |
| Drain-Source On-State Resistance ^a | R _{DS(on)} | V _{GS} = 10 V, I _D = 5 A | | 32 | | mΩ |
| | | V _{GS} = 4.5 V, I _D = 5 A | | 33 | | |
| Forward Transconductance ^a | g _{fs} | V _{DS} = 15 V, I _D = 5 A | | 20 | | S |
| Dynamic ^b | | | | | | |
| Input Capacitance | C _{iss} | V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz | | 1900 | | pF |
| Output Capacitance | C _{oss} | | | 150 | | |
| Reverse Transfer Capacitance | C _{rss} | | | 50 | | |
| Total Gate Charge | Q _g | V _{DS} = 75 V, V _{GS} = 10 V, I _D = 5 A | | 28.5 | 43 | nC |
| Gate-Source Charge | Q _{gs} | V _{DS} = 75 V, V _{GS} = 8 V, I _D = 5 A | | 23 | 35 | |
| Gate-Drain Charge | Q _{gd} | | | 8 | | |
| Gate Resistance | R _g | | | 6.5 | | |
| Gate Resistance | R _g | f = 1 MHz | | 0.80 | 1.3 | Ω |
| Turn-on Delay Time | t _{d(on)} | V _{DD} = 50 V, R _L = 10 Ω I _D ≡ 5 A, V _{GEN} = 10 V, R _g = 1 Ω | | 14 | 21 | ns |
| Rise Time | t _r | | | 12 | 18 | |
| Turn-Off Delay Time | t _{d(off)} | | | 22 | 33 | |
| Fall Time | t _f | | | 6 | 10 | |
| Turn-On Delay Time | t _{d(on)} | V _{DD} = 50 V, R _L = 10 Ω I _D ≡ 5 A, V _{GEN} = 8 V, R _g = 1 Ω | | 16 | 24 | |
| Rise Time | t _r | | | 12 | 18 | |
| Turn-Off Delay Time | t _{d(off)} | | | 20 | 30 | |
| Fall Time | t _f | | | 7 | 12 | |
| Drain-Source Body Diode Characteristics | | | | | | |
| Continuous Source-Drain Diode Current | I _S | T _C = 25 °C | | | 7.7 | A |
| Pulse Diode Forward Current ^a | I _{SM} | | | | 50 | |
| Body Diode Voltage | V _{SD} | I _S = 2.6 A | | 0.77 | 1.2 | V |
| Body Diode Reverse Recovery Time | t _{rr} | I _F = 5 A, dI/dt = 100 A/μs, T _J = 25 °C | | 63 | 95 | ns |
| Body Diode Reverse Recovery Charge | Q _{rr} | | | 110 | 165 | nC |
| Reverse Recovery Fall Time | t _a | | | 49 | | ns |
| Reverse Recovery Rise Time | t _b | | | 14 | | |

Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
 a. Guaranteed by design, not subject to production testing.

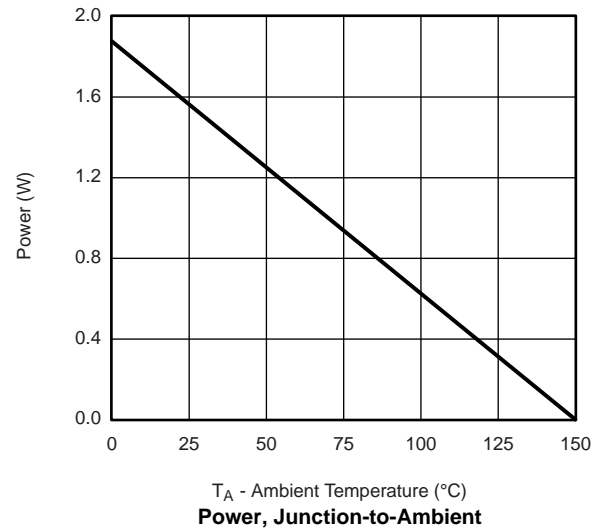
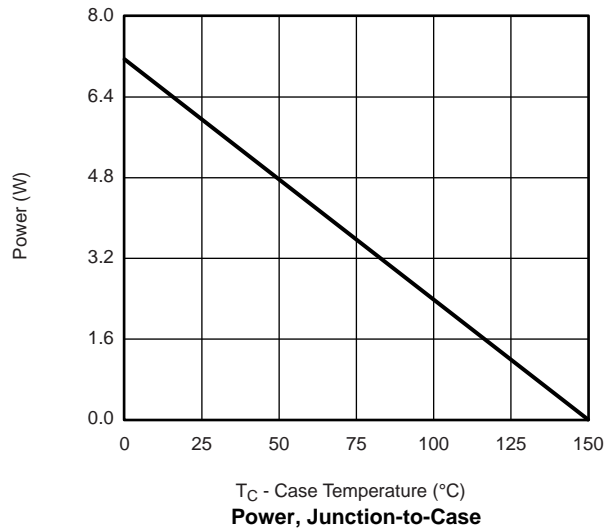
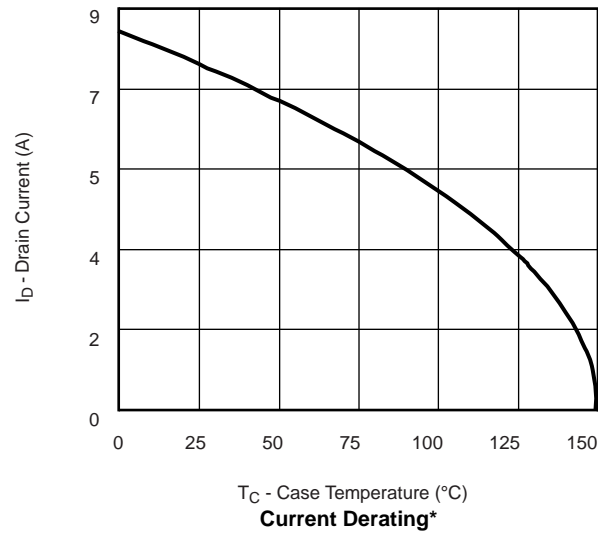
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


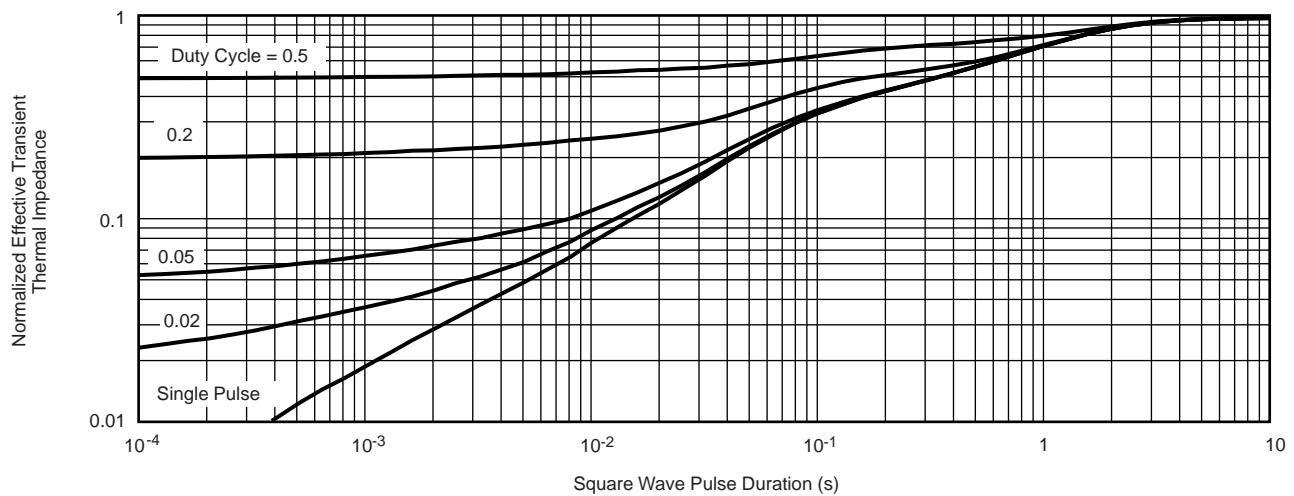
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


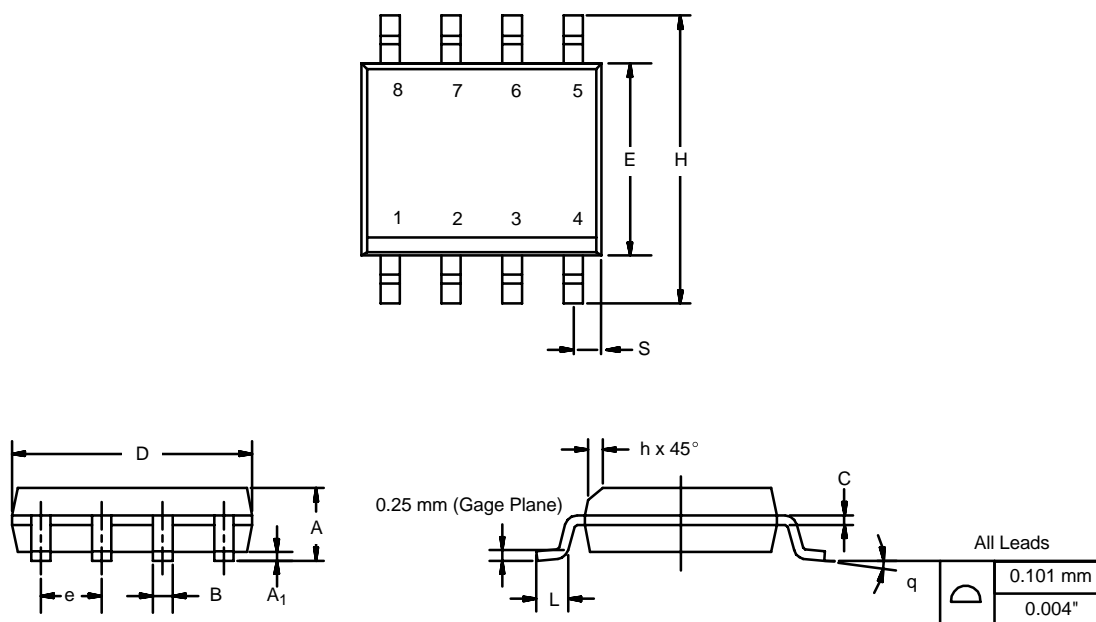
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Foot

SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



| DIM | MILLIMETERS | | INCHES | |
|----------------|-------------|------|-----------|-------|
| | Min | Max | Min | Max |
| A | 1.35 | 1.75 | 0.053 | 0.069 |
| A ₁ | 0.10 | 0.20 | 0.004 | 0.008 |
| B | 0.35 | 0.51 | 0.014 | 0.020 |
| C | 0.19 | 0.25 | 0.0075 | 0.010 |
| D | 4.80 | 5.00 | 0.189 | 0.196 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.020 |
| L | 0.50 | 0.93 | 0.020 | 0.037 |
| q | 0° | 8° | 0° | 8° |
| S | 0.44 | 0.64 | 0.018 | 0.026 |

ECN: C-06527-Rev. I, 11-Sep-06
DWG: 5498

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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