

F7307Q-VB Datasheet

N- and P-Channel 20-V (D-S) MOSFETS

PRODUCT SUMMARY

	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
N-Channel	20	0.006 at V _{GS} = 4.5 V	15 ^a	11 nC
		0.010 at V _{GS} = 2.5 V	12 ^a	
P-Channel	-20	0.016 at V _{GS} = -4.5 V	-8.5 ^a	25 nC
		0.020 at V _{GS} = -2.5 V	-7.0 ^a	

FEATURES

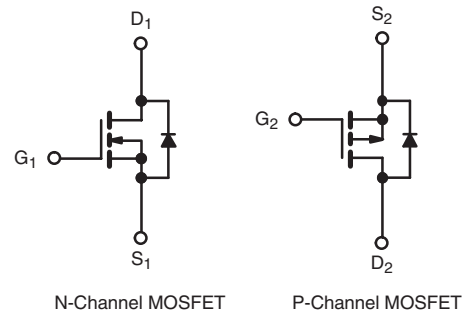
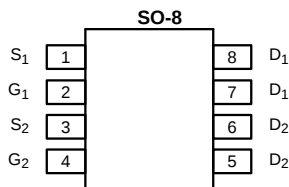
- Halogen-free
- Trench Power MOSFETs

APPLICATIONS

- Load Switch
- DC/DC Converter



RoHS
COMPLIANT



ABSOLUTE MAXIMUM RATINGS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V _{DS}	20	-20	V
Gate-Source Voltage	V _{GS}	±12		V
Continuous Drain Current ($T_J = 150\text{ }^{\circ}\text{C}$)	I _D	15	-8.5	A
		12	-6.8	
		13 ^{b, c}	-7.0 ^{b, c}	
		11 ^{b, c}	-5.6 ^{b, c}	
Pulsed Drain Current	I _{DM}	30	-30	A
Source Drain Current Diode Current	I _S	5.3	-4.4	A
		3.9 ^{b, c}	-2.9 ^{b, c}	
Maximum Power Dissipation	P _D	3.1	3.2	W
		2.1	2.2	
		2.1 ^{b, c}	2.2 ^{b, c}	
		1.7 ^{b, c}	1.76 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	N-Channel		P-Channel		Unit
		Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient ^{b, d}	R _{thJA}	85	110	81	105	°C/W
Maximum Junction-to-Foot (Drain)	R _{thJF}	62	80	57	75	

Notes:

a. $T_C = 25\text{ }^{\circ}\text{C}$.

b. Surface Mounted on 1" x 1" FR4 board.

c. $t = 10\text{ s}$.

d. Maximum under Steady State conditions is 145 °C/W.

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	N-Ch	20			V
		$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-20			
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	N-Ch		22		mV/ $^{\circ}\text{C}$
		$I_D = -250\text{ }\mu\text{A}$	P-Ch		-21		
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	N-Ch		-3.5		
		$I_D = -250\text{ }\mu\text{A}$	P-Ch		3.5		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N-Ch	0.6		1.5	V
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-0.6		-1.5	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$	N-Ch P-Ch			± 100 ± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	N-Ch			1	μA
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$	P-Ch			-1	
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^{\circ}\text{C}$	N-Ch			10	
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^{\circ}\text{C}$	P-Ch			-10	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 4.5\text{ V}$	N-Ch	30			A
		$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	P-Ch	-30			
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 5.7\text{ A}$	N-Ch		0.006		Ω
		$V_{GS} = -4.5\text{ V}, I_D = -5.1\text{ A}$	P-Ch		0.016		
		$V_{GS} = 2.5\text{ V}, I_D = 4.4\text{ A}$	N-Ch		0.010		
		$V_{GS} = -2.5\text{ V}, I_D = -4.2\text{ A}$	P-Ch		0.020		
Forward Transconductance ^b	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 5.7\text{ A}$	N-Ch		17		S
		$V_{DS} = -10\text{ V}, I_D = -5.1\text{ A}$	P-Ch		22		
Dynamic ^a							
Input Capacitance	C_{iss}	N-Channel $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch P-Ch		1250 1600		pF
Output Capacitance	C_{oss}		N-Ch P-Ch		180 280		
Reverse Transfer Capacitance	C_{rss}	P-Channel $V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch P-Ch		100 65		
Total Gate Charge	Q_g	$V_{DS} = 10\text{ V}, V_{GS} = 10\text{ V}, I_D = 5.7\text{ A}$	N-Ch		23	35	nC
		$V_{DS} = -10\text{ V}, V_{GS} = -10\text{ V}, I_D = -5.1\text{ A}$	P-Ch		44	61	
		N-Channel $V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 5.7\text{ A}$	N-Ch P-Ch		11 25	20 35	
			P-Channel $V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -5.1\text{ A}$	N-Ch P-Ch		1.8 3	
Gate-Source Charge	Q_{gs}			N-Ch P-Ch		0.9 5.5	
Gate-Drain Charge	Q_{gd}		N-Ch P-Ch		0.9 5.5		
Gate Resistance	R_g	$f = 1\text{ MHz}$	N-Ch P-Ch		2 6		Ω

Notes:

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Dynamic ^a							
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 10\text{ V}, R_L = 2.2\text{ }\Omega$ $I_D \cong 4.5\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$ P-Channel $V_{DD} = -10\text{ V}, R_L = 2.4\text{ }\Omega$ $I_D \cong -4.1\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$	N-Ch		12	20	ns
			P-Ch		30	45	
Rise Time	t_r		N-Ch		10	15	
			P-Ch		25	40	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		25	40	
			P-Ch		45	70	
Fall Time	t_f		N-Ch		10	15	
			P-Ch		15	25	
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 10\text{ V}, R_L = 2.2\text{ }\Omega$ $I_D \cong 4.5\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$ P-Channel $V_{DD} = -10\text{ V}, R_L = 2.4\text{ }\Omega$ $I_D \cong -4.1\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$	N-Ch		10	15	ns
			P-Ch		10	15	
Rise Time	t_r		N-Ch		10	15	
			P-Ch		10	15	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		20	30	
			P-Ch		45	70	
Fall Time	t_f		N-Ch		8	15	
			P-Ch		15	25	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^{\circ}\text{C}$	N-Ch			1.3	A
			P-Ch			-1.4	
Pulse Diode Forward Current ^a	I_{SM}		N-Ch			30	
			P-Ch			-30	
Body Diode Voltage	V_{SD}	$I_S = 4.5\text{ A}, V_{GS} = 0\text{ V}$	N-Ch		0.8	1.2	V
		$I_S = -4.1\text{ A}, V_{GS} = 0\text{ V}$	P-Ch		-0.8	-1.2	
Body Diode Reverse Recovery Time	t_{rr}	N-Channel $I_F = 4.5\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^{\circ}\text{C}$ P-Channel $I_F = -4.1\text{ A}, dI/dt = -100\text{ A}/\mu\text{s}, T_J = 25\text{ }^{\circ}\text{C}$	N-Ch		15	30	ns
			P-Ch		35	55	
Body Diode Reverse Recovery Charge	Q_{rr}		N-Ch		6	12	nC
			P-Ch		21	35	
Reverse Recovery Fall Time	t_a		N-Ch		7.6		ns
			P-Ch		18		
Reverse Recovery Rise Time	t_b		N-Ch		7.4		
			P-Ch		17		

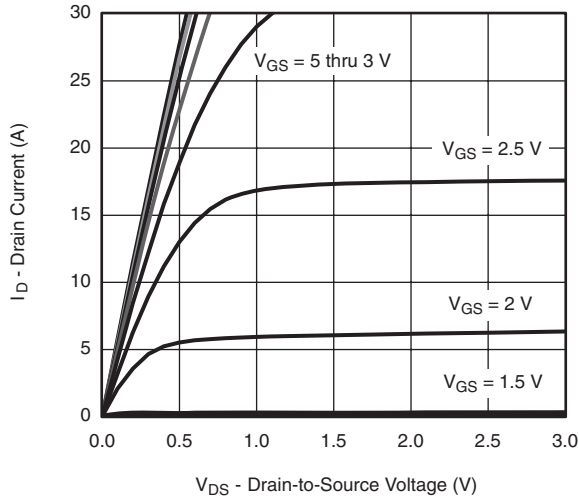
Notes:

a. Guaranteed by design, not subject to production testing.

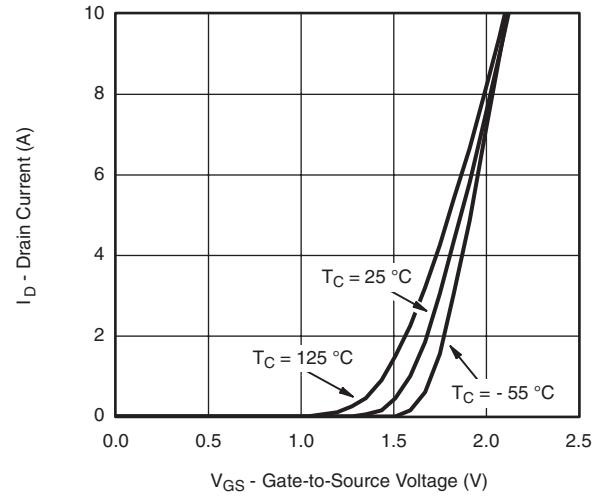
b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

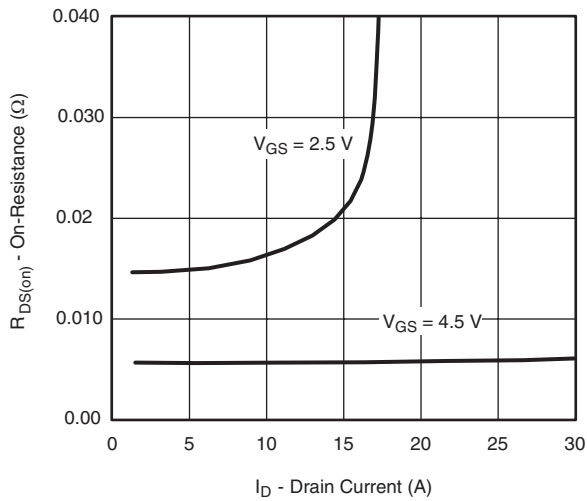
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



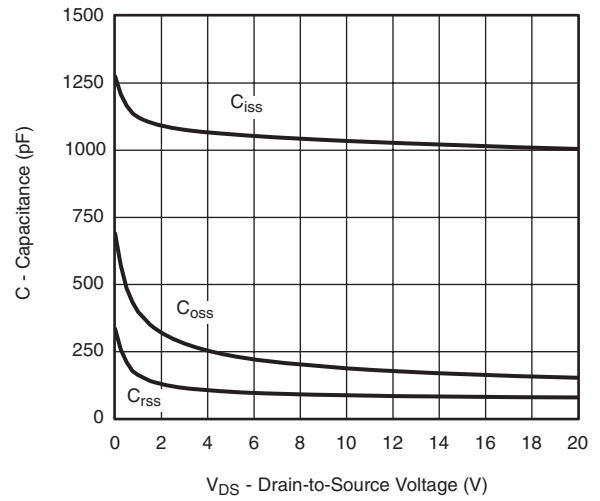
Output Characteristics



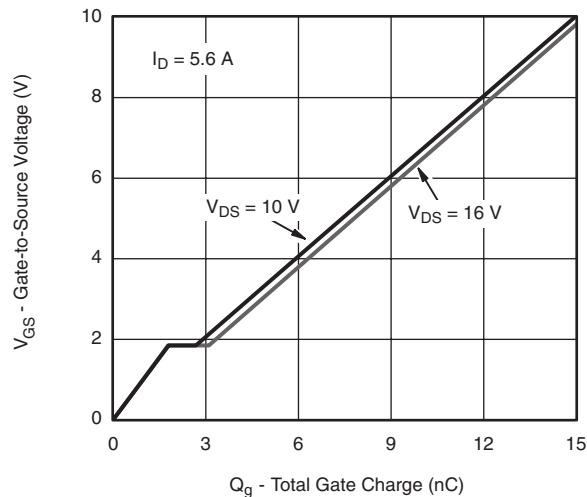
Transfer Characteristics



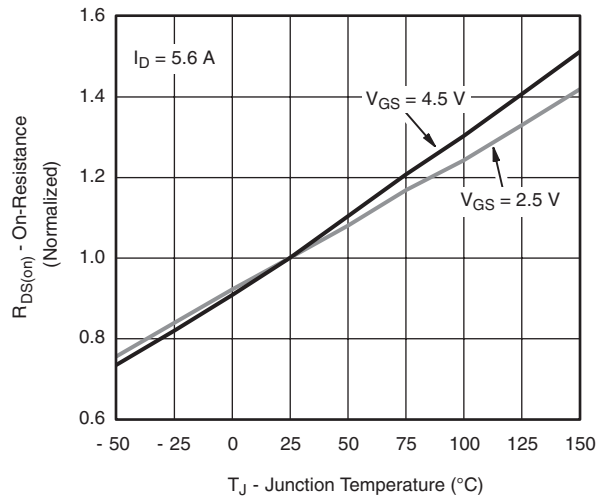
On-Resistance vs. Drain Current



Capacitance

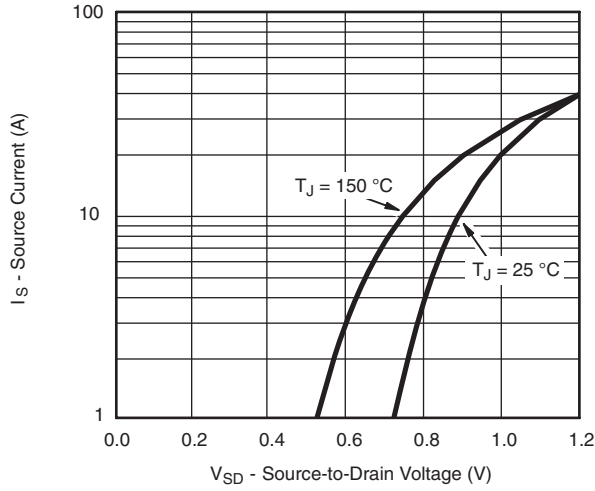


Gate Charge

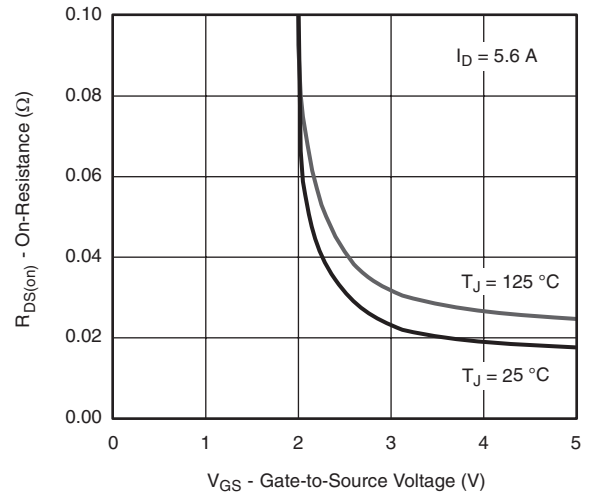


On-Resistance vs. Junction Temperature

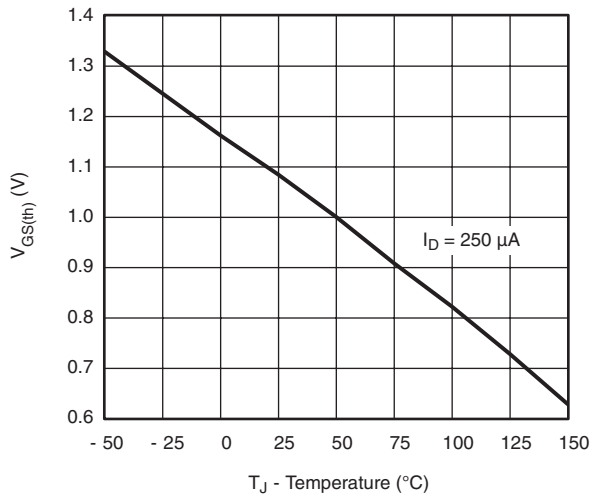
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



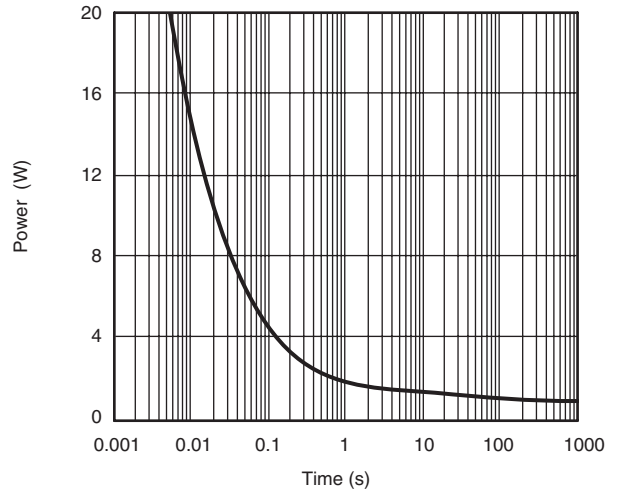
Source-Drain Diode Forward Voltage



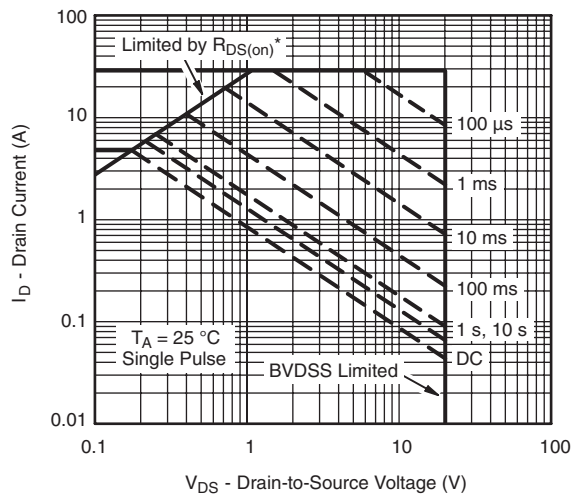
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



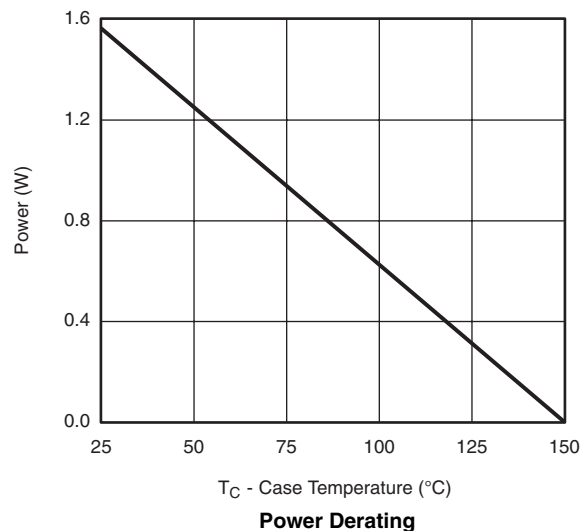
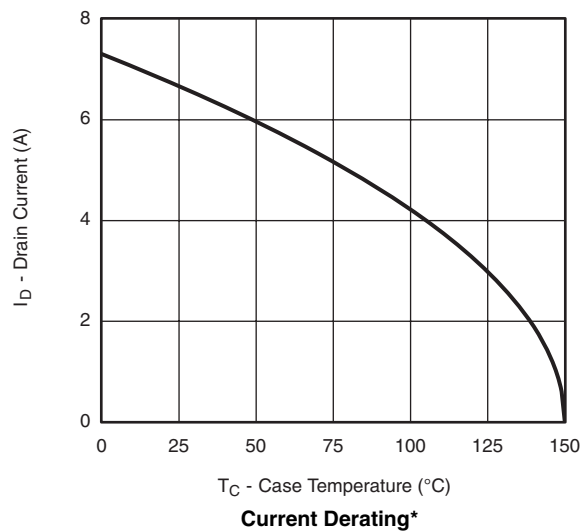
Single Pulse Power



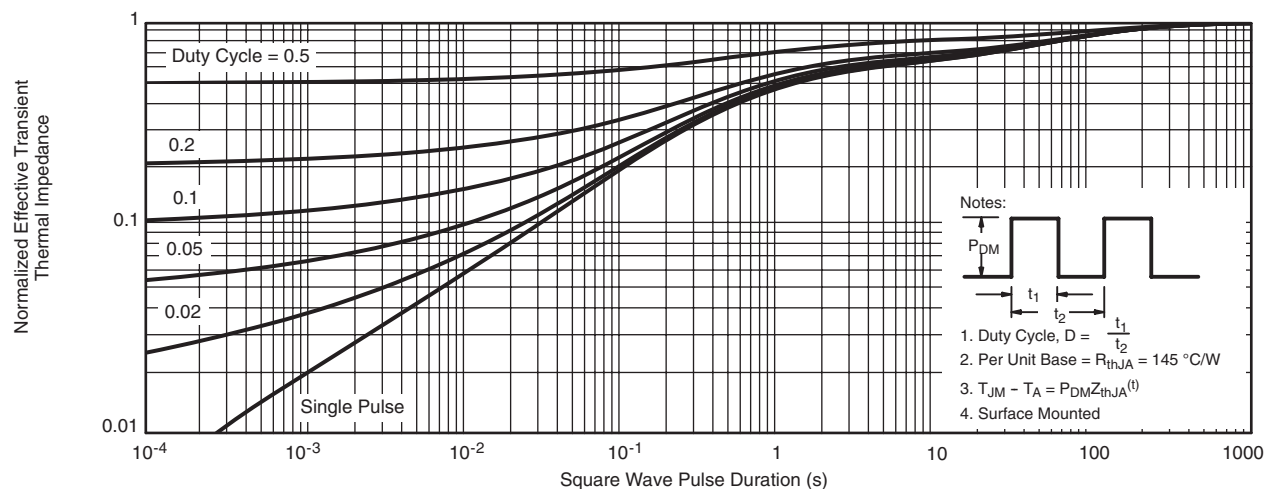
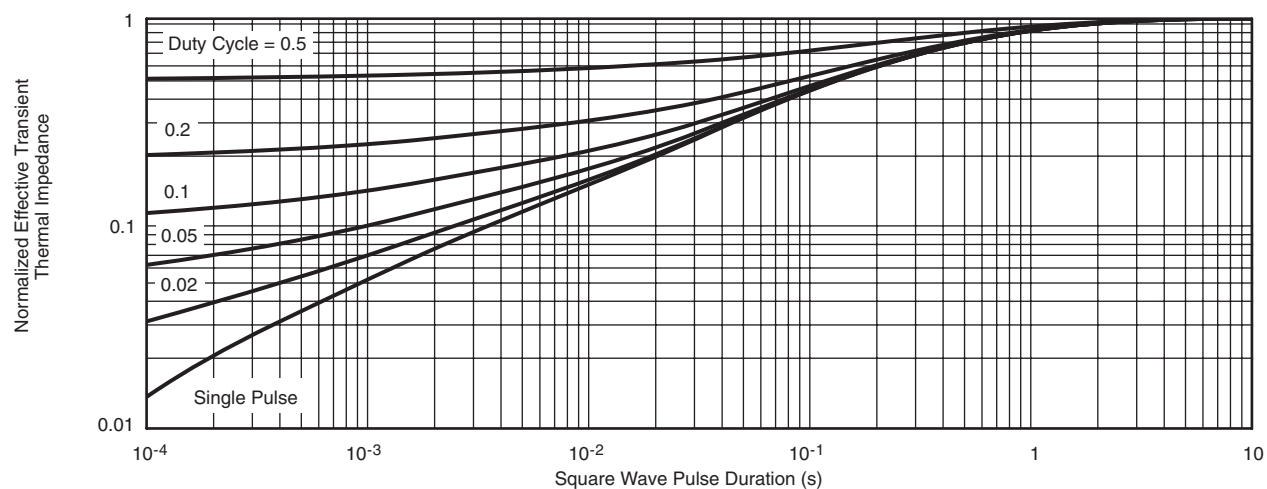
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

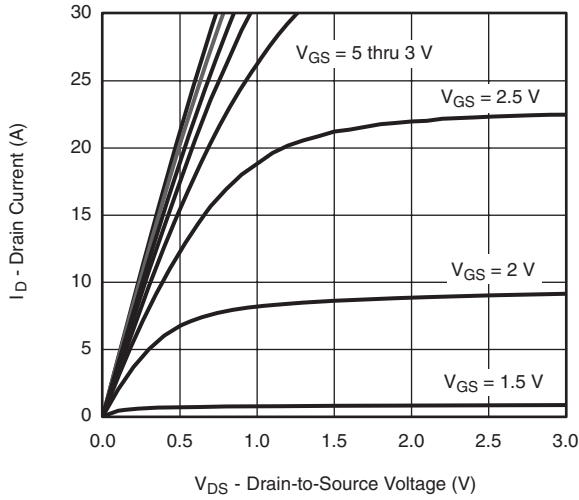
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



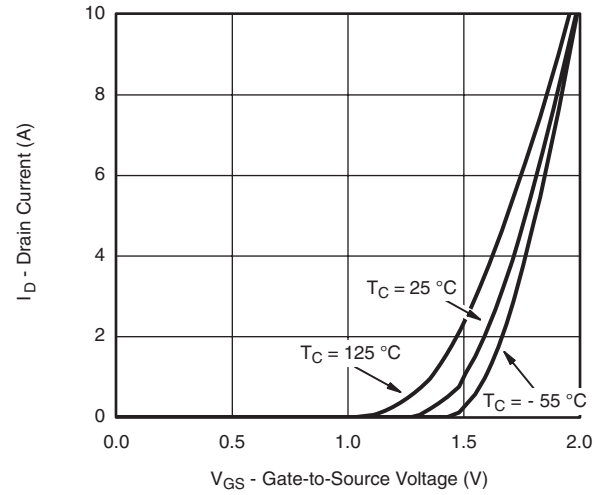
* The power dissipation P_D is based on $T_{J(max)} = 150\text{ }^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Foot

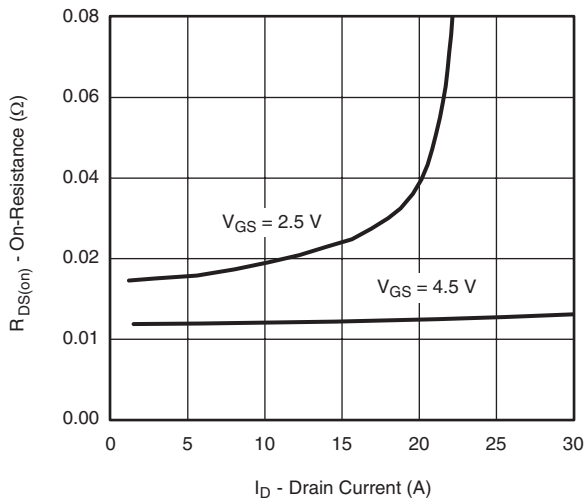
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



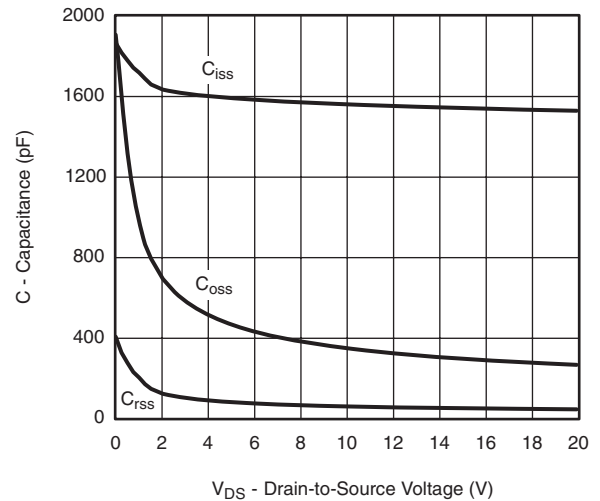
Output Characteristics



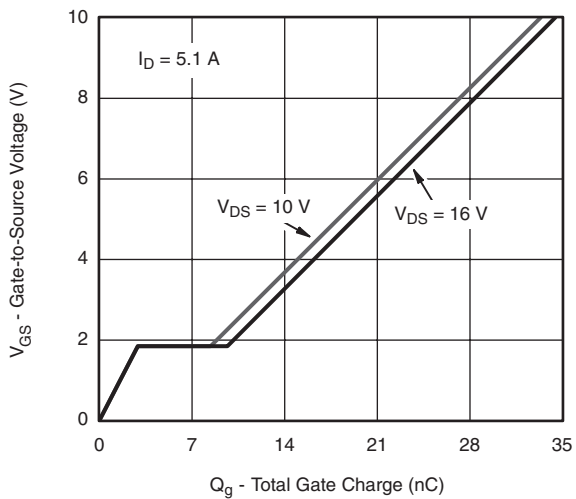
Transfer Characteristics



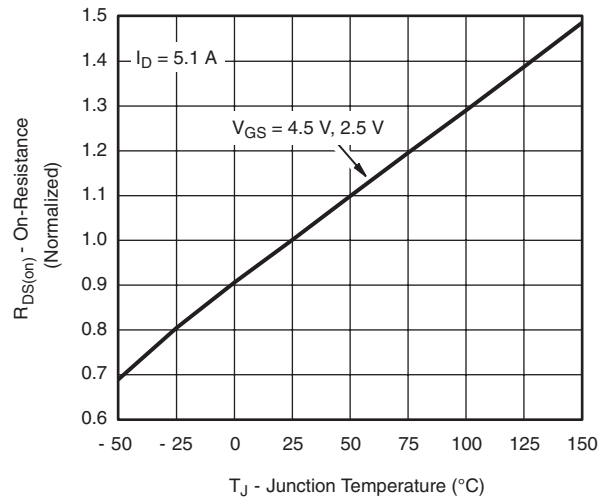
On-Resistance vs. Drain Current



Capacitance

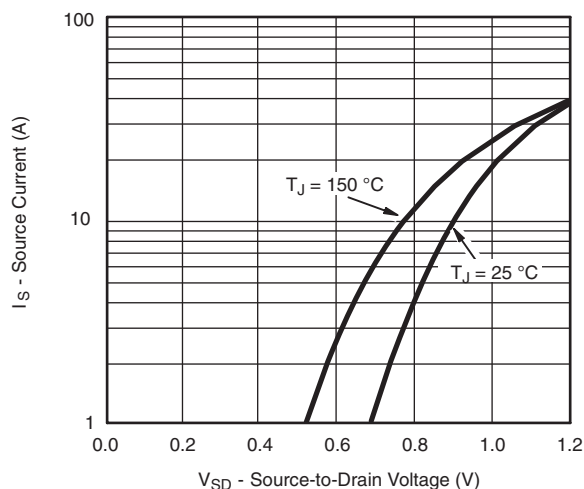


Gate Charge

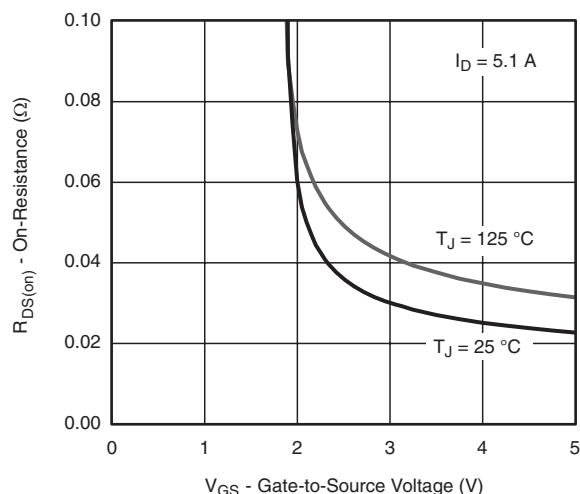


On-Resistance vs. Junction Temperature

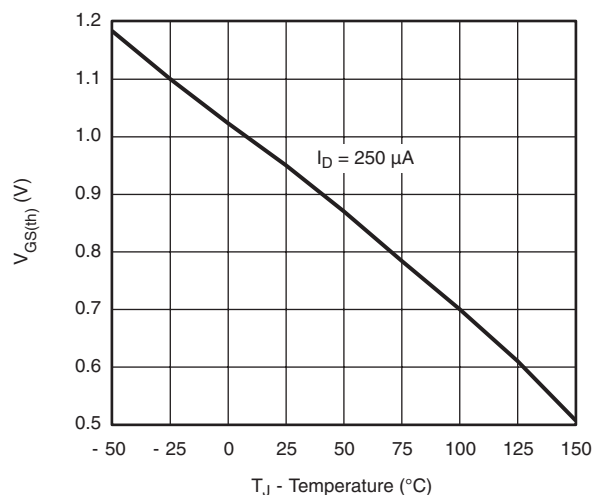
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



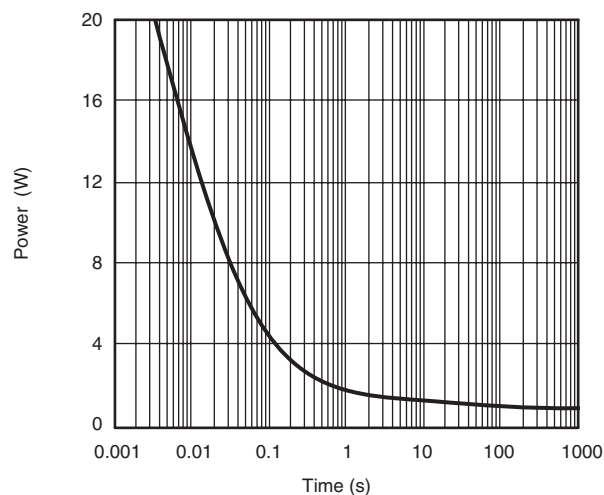
Source-Drain Diode Forward Voltage



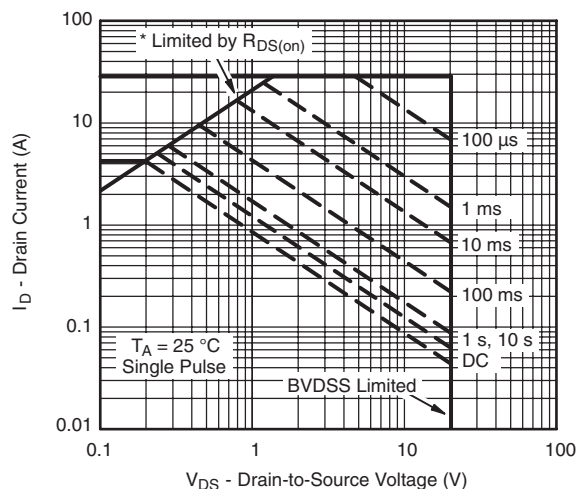
On-Resistance vs. Gate-to-Source



Threshold Voltage



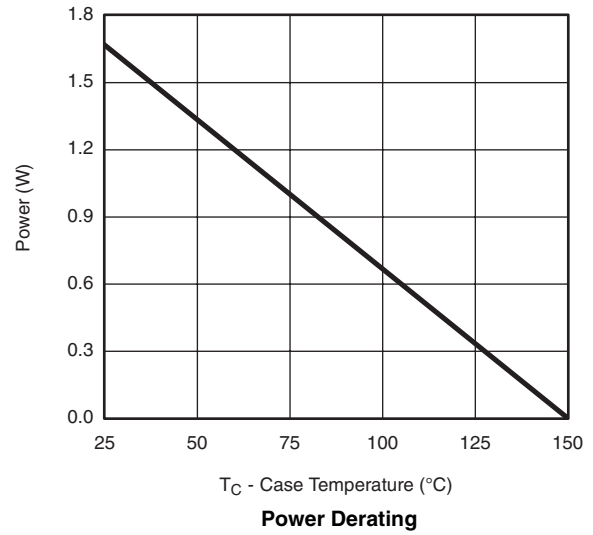
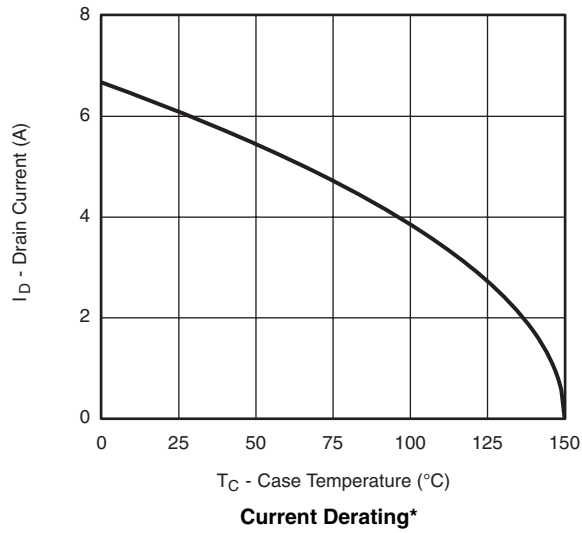
Single Pulse Power



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

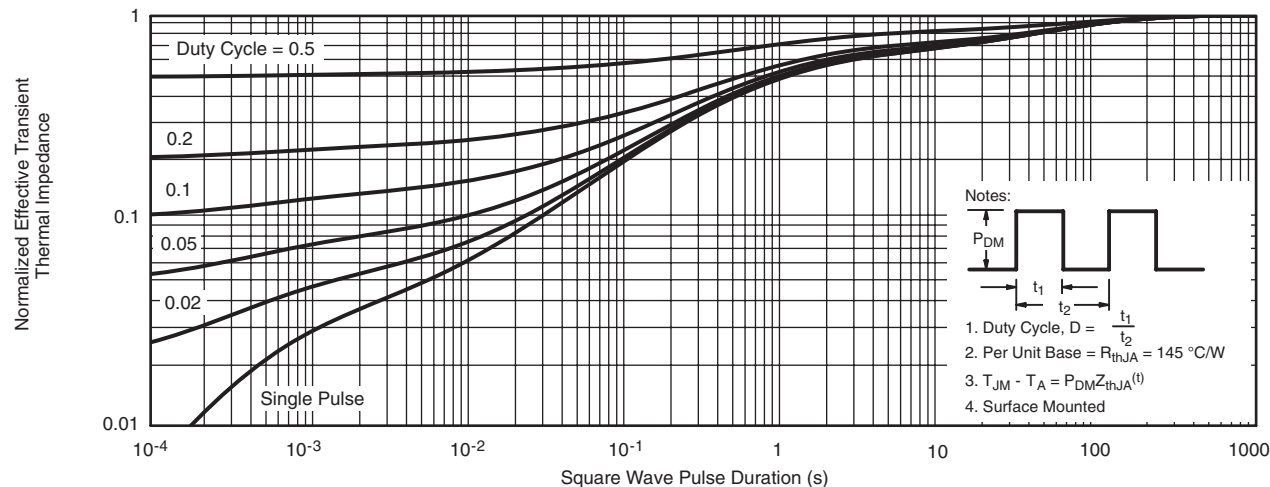
Safe Operating Area, Junction-to-Ambient

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

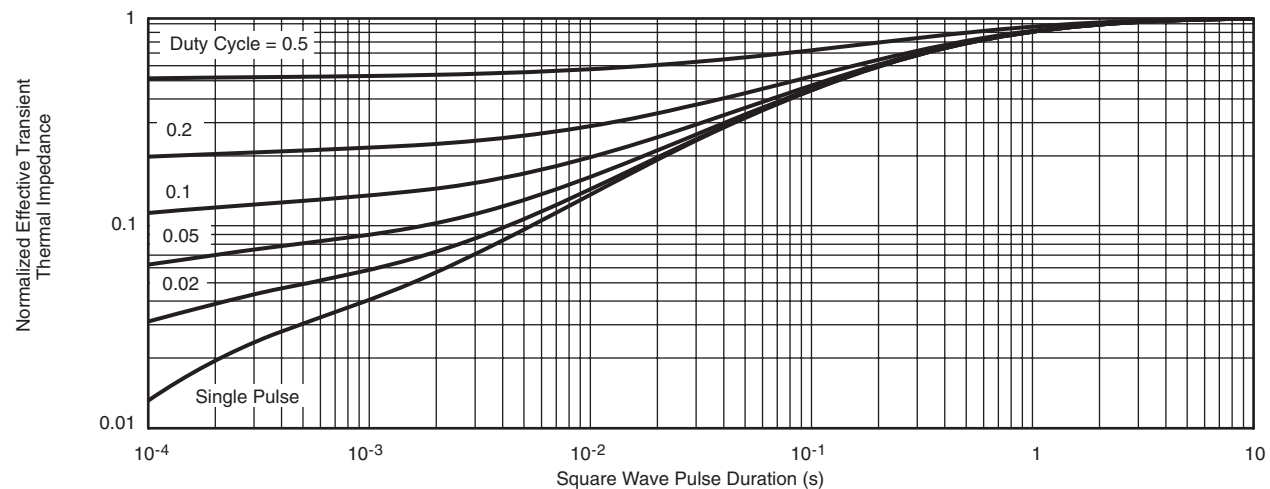


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

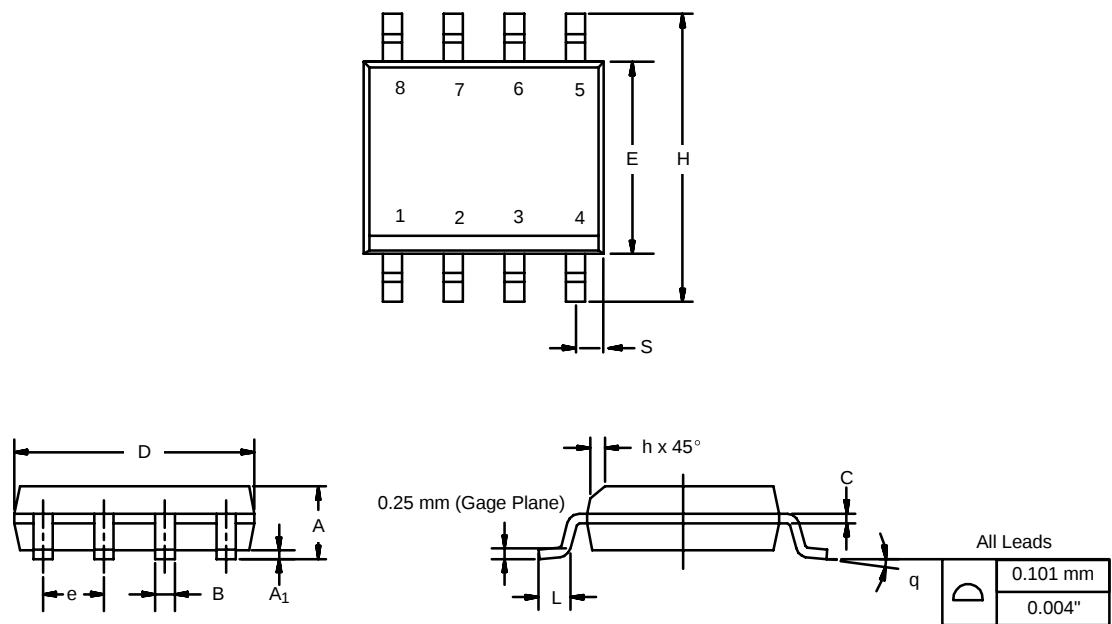


Normalized Thermal Transient Impedance, Junction-to-Ambient



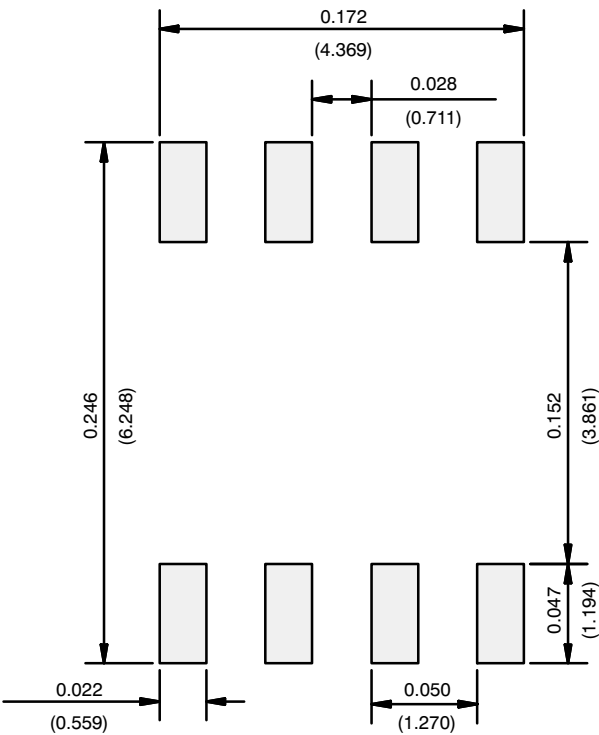
Normalized Thermal Transient Impedance, Junction-to-Foot

SOIC (NARROW): 8-LEAD
JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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