

ELM14411AA-VB Datasheet P-Channel 30-V (D-S) MOSFET

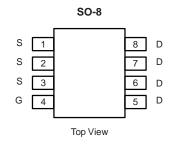
PRODUCT SUMMARY					
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^d	Q _g (Typ.)		
- 30	0.018 at V _{GS} = - 10 V	- 9.0	13 nC		
- 30	0.024 at V _{GS} = - 4.5 V	- 7.8	13110		

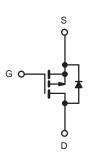
FEATURES

- Halogen-free According to IEC 61249-2-21
 Definition
- Trench Power MOSFET
- 100 % R_g Tested

APPLICATIONS

- Load Switch
- Battery Switch





P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	A = 25 °C, unless othe	erwise noted		
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	- 30	V	
Gate-Source Voltage	V _{GS}	± 20	v	
	T _C = 25 °C		- 9.0	
Continuous Drain Current (T ₁ = 150 °C)	T _C = 70 °C		- 7.2	
Continuous Drain Current $(T_j = 150^{\circ} C)$	T _A = 25 °C		- 7.0 ^{a, b}	
	T _A = 70 °C		- 5.6 ^{a, b}	A
Pulsed Drain Current	I _{DM} -	- 30		
Continuous Course Drain Diada Current	T _C = 25 °C		- 3.5	
Continuous Source-Drain Diode Current	T _A = 25 °C	Is I	- 2.1 ^{a, b}	
	T _C = 25 °C		4.2	
Maximum Davies Disais stics	T _C = 70 °C		2.7	W
Maximum Power Dissipation	T _A = 25 °C	FD FD	2.5 ^{a, b}	VV
	T _A = 70 °C	1	1.6 ^{a, b}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{a, c}	t ≤ 10 s	R _{thJA}	40	50	°C/W	
Maximum Junction-to-Foot	Steady State	R _{thJF}	24	30	0,000	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. t = 10 s.

c. Maximum under Steady State conditions is 95 °C/W.

d. Based on $T_C = 25 \text{ °C}$.

COMPLIANT HALOGEN

Available

SPECIFICATIONS $T_J = 25 \circ C$, unless oth	erwise noted					
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 30			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	1 050 1		- 31		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = - 250 μA		4.5			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \ \mu A$	- 1.0		- 2.5	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
		$V_{DS} = -30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			- 1		
Zero Gate Voltage Drain Current	IDSS	$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 \text{ °C}$			- 5	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \le -5 V, V_{GS} = -10 V$	- 20			Α	
	_ ` `	V _{GS} = - 10 V, I _D = - 7.0 A	0.018			1	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 5.6 A		0.024		Ω	
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 15 V, I _D = - 7.0 A		18		S	
Dynamic ^b	010		I			1	
Input Capacitance	C _{iss}			1455			
Output Capacitance	C _{oss}	V _{DS} = - 15 V, V _{GS} = 0 V, f = 1 MHz		180		pF	
Reverse Transfer Capacitance	C _{rss}			145			
		V _{DS} = - 15 V, V _{GS} = - 10 V, I _D = - 7.0 A		25	38		
Total Gate Charge	Qg			13	20	-	
Gate-Source Charge	Q _{gs}	V _{DS} = - 15 V, V _{GS} = - 4.5 V, I _D = - 7.0 A		3.5	-	nC	
Gate-Drain Charge	Q _{gd}			5.5		-	
Gate Resistance	Rg	f = 1 MHz	0.4	2.0	4.0	Ω	
Turn-On Delay Time	t _{d(on)}			10	20		
Rise Time	t _r	V _{DD} = - 15 V, R _I = 2.7 Ω		13	20		
Turn-Off DelayTime	t _{d(off)}	$I_D \cong -5.6 \text{ A}, \text{ V}_{\text{GEN}} = -10 \text{ V}, \text{ R}_{\text{g}} = 1 \Omega$		23	35		
Fall Time	t _f			9	18		
Turn-On Delay Time	t _{d(on)}			38	57	ns	
Rise Time	t _r	V _{DD} = - 15 V, R _I = 2.7 Ω		89	134		
Turn-Off DelayTime	t _{d(off)}	$I_D \cong -5.6 \text{ A}, \text{ V}_{\text{GEN}} = -4.5 \text{ V}, \text{ R}_a = 1 \Omega$		22	33		
Fall Time	t _f			11	17		
Drain-Source Body Diode Characteris	-		I				
Continous Source-Drain Diode Current	Is	T _C = 25 °C			- 6.5		
Pulse Diode Forward Current	I _{SM}	<u> </u>			- 30	A	
Body Diode Voltage	V _{SD}	I _S = - 5.6 A, V _{GS} = 0 V		- 0.71	- 1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			22	33	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	1		17	26	nC	
, , , ,		I _F = - 5.6 A, dI/dt = 100 A/μs, T _{.1} = 25 °C					
Reverse Recovery Fall Time	t _a			13			

Notes:

a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.

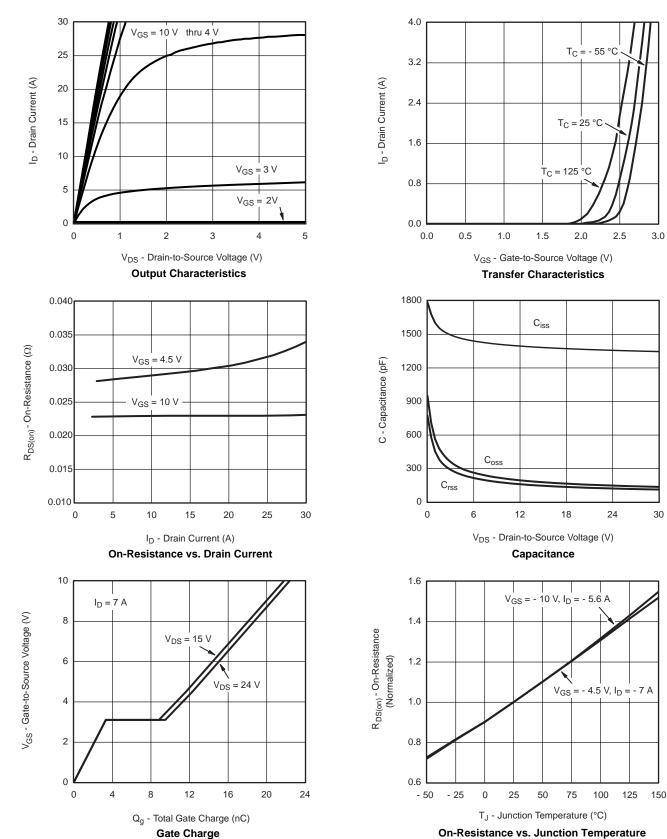
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

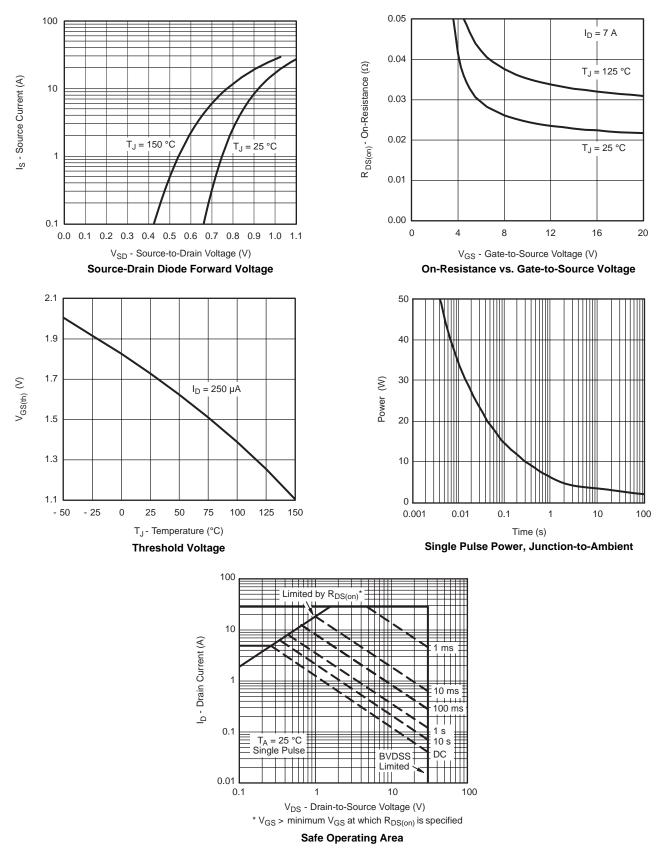
semi

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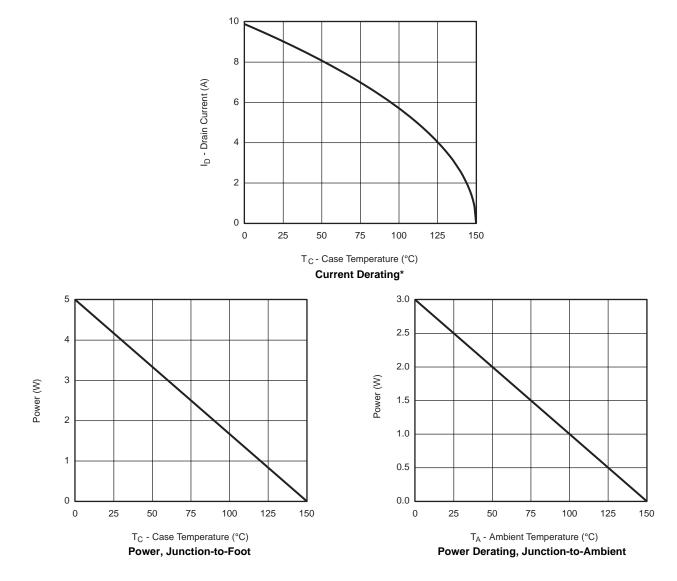






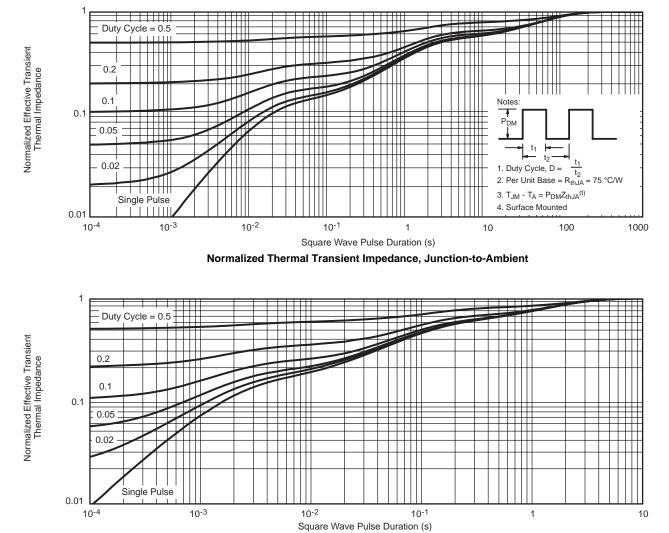






* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Foot



SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012





	MILLIMETERS		INC	HES		
DIM	Min	Мах	Min	Max		
A	1.35	1.75	0.053	0.069		
A ₁	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
E	3.80	4.00	0.150	0.157		
е	1.27 BSC		0.050	0.050 BSC		
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498						



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)



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