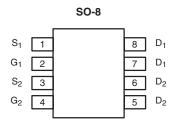


# AUF7304Q-VB Datasheet Dual P-Channel 20V (D-S) MOSFET

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}\left(\Omega\right)$	I <sub>D</sub> (A)			
	0.018 at V <sub>GS</sub> = - 4.5 V	- 8.9			
- 20	0.022 at V <sub>GS</sub> = - 2.5 V	- 8.1			
	0.030 at V <sub>GS</sub> = - 1.8 V	- 3.6			



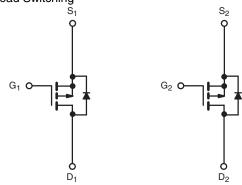
#### **FEATURES**

- Halogen-free According to IEC 61249-2-21 Definition
- Trench Power MOSFET
- Advanced High Cell Density Process
- Compliant to RoHS Directive 2002/95/EC

## ROHS COMPLIANT HALOGEN FREE

#### **APPLICATIONS**

Load Switching



P-Channel MOSFET

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T	<sub>A</sub> = 25 °C, unle	ss otherwise r	noted		
Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V <sub>DS</sub>	- 20		V
Gate-Source Voltage		V <sub>GS</sub>	± 12		
Continuous Dunis Comment /T 450 9008	T <sub>A</sub> = 25 °C	- I <sub>D</sub>	- 8.9	- 6.7	
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup>	T <sub>A</sub> = 70 °C		- 7.1	- 5.4	
Pulsed Drain Current		I <sub>DM</sub>	- 30		Α
Continuous Source Current (Diode Conduction) <sup>a</sup>		I <sub>S</sub>	- 1.7	- 0.9	
W	T <sub>A</sub> = 25 °C	P <sub>D</sub>	2.0	1.1	W
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 70 °C	] ' <sup>*</sup> D	1.3	0.7	VV
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maniana landina ta Antina	t ≤ 10 s	R <sub>thJA</sub>	46	62.5	
Maximum Junction-to-Ambient <sup>a</sup>	Steady State	' 'thJA	80	110	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	$R_{thJF}$	24	32	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.



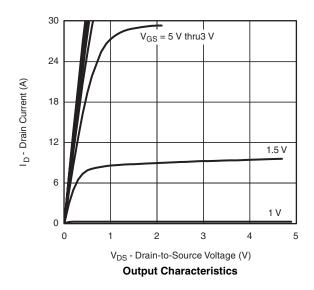
Parameter	Symbol	Test Conditions		Тур.	Max.	Unit
Static				•		
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = -350 \mu A$	- 0.4		- 1.0	V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 8 V			± 100	nA
Zava Cata Valta da Busin Comuna	I <sub>DSS</sub>	V <sub>DS</sub> = - 20 V, V <sub>GS</sub> = 0 V	-1		- 1	μА
Zero Gate Voltage Drain Current		V <sub>DS</sub> = - 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			- 5	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = - 5 V, V <sub>GS</sub> = - 4.5 V	- 30			Α
	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 8.9 A	0.018			
Drain-Source On-State Resistance <sup>a</sup>		V <sub>GS</sub> = - 2.5 V, I <sub>D</sub> = - 8.1 A		0.022		Ω
		V <sub>GS</sub> = - 1.8 V, I <sub>D</sub> = - 3.6 A		0.030		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = - 10 V, I <sub>D</sub> = - 8.9 A		26		S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	I <sub>S</sub> = - 1.7 A, V <sub>GS</sub> = 0 V		- 0.7	- 1.2	V
Dynamic <sup>b</sup>						
Total Gate Charge	$Q_g$			34.5	52	
Gate-Source Charge	$Q_{gs}$	V <sub>DS</sub> = - 10 V, V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 8.9 A		5.1		nC
Gate-Drain Charge	$Q_{gd}$			9.6		
Gate Resistance	$R_g$			9		Ω
Turn-On Delay Time	t <sub>d(on)</sub>			25	40	
Rise Time	t <sub>r</sub>	$V_{DD}$ = - 10 V, $R_L$ = 6 $\Omega$		46	70	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong$ - 1 A, $V_{GEN}$ = - 4.5 V, $R_g$ = 6 $\Omega$		230	345	ns
Fall Time				155	235	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = - 1.7 A, dI/dt = 100 A/μs		128	200	

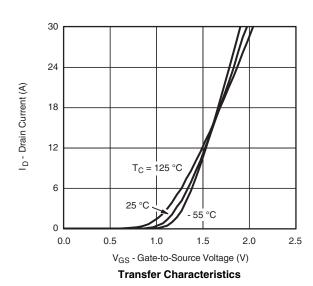
#### Notes:

- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

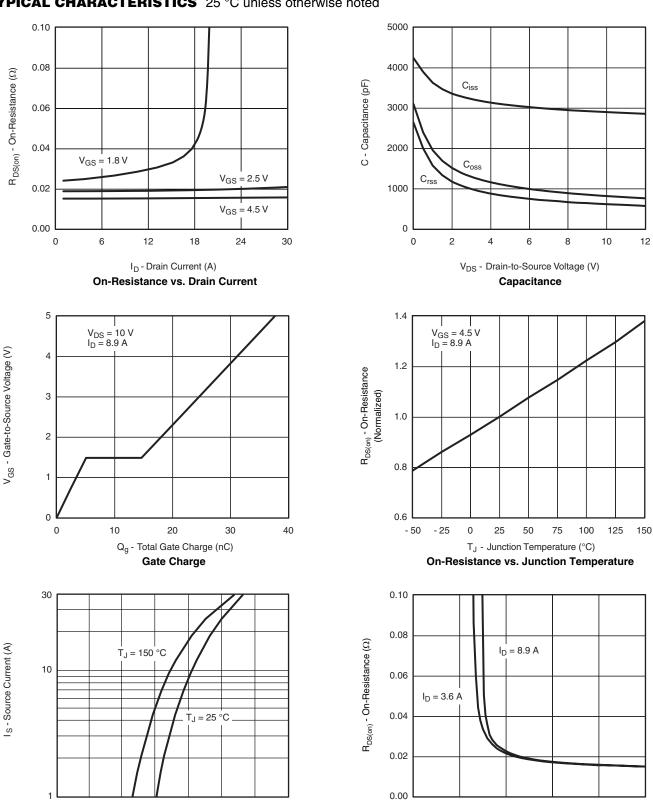
#### TYPICAL CHARACTERISTICS 25 °C unless otherwise noted







#### TYPICAL CHARACTERISTICS 25 °C unless otherwise noted



0

0.0

0.2

0.4

0.6

0.8

V<sub>SD</sub> - Source-to-Drain Voltage (V)

Source-Drain Diode Forward Voltage

1.0

1.2

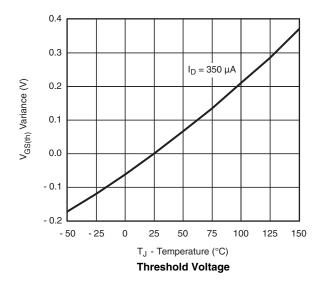
5

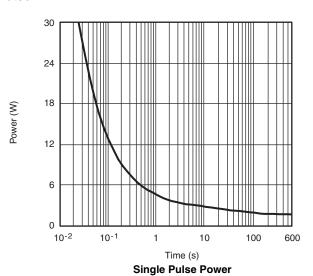
 $V_{GS}$  - Gate-to-Source Voltage (V)

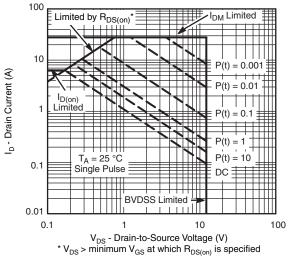
On-Resistance vs. Gate-to-Source Voltage



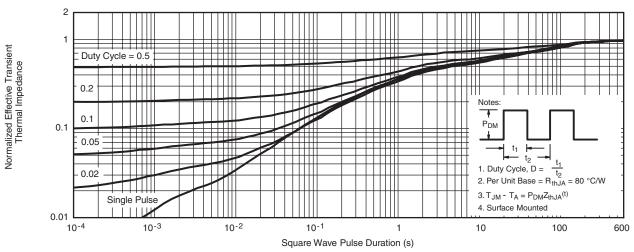
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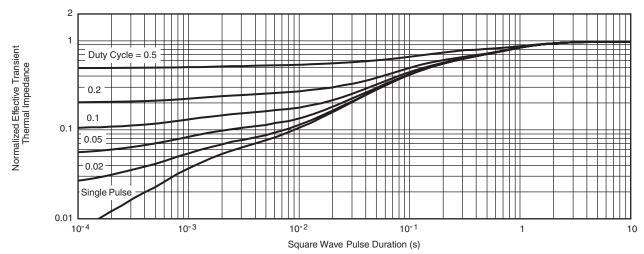




Normalized Thermal Transient Impedance, Junction-to-Ambient



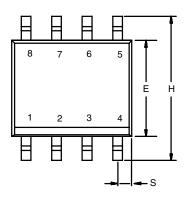
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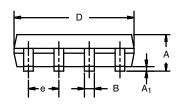


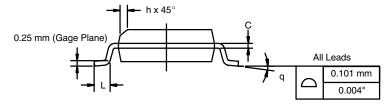
Normalized Thermal Transient Impedance, Junction-to-Foot



SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012





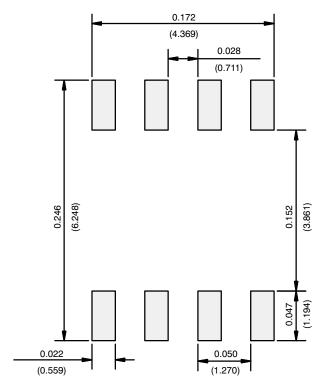


	MILLIM	IETERS	INC	INCHES		
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A <sub>1</sub>	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
E	3.80	4.00	0.150	0.157		
е	1.27	BSC	0.050 BSC			
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C-06527-Rev. J. 11-Sep-06						

DWG: 5498



#### **RECOMMENDED MINIMUM PADS FOR SO-8**



Recommended Minimum Pads Dimensions in Inches/(mm)

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