AP50T10GM-HF-VB Datasheet
N-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[a]	Q_g (Typ.)
100	0.200 at V_{GS} = 10 V	3	7.3 nC

FEATURES

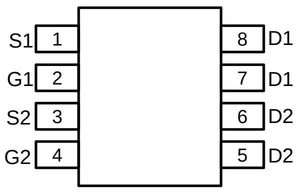
- **Halogen-free According to IEC 61249-2-21 Definition**
- Trench Power MOSFET
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC

Pb-free
RoHS COMPLIANT
HALOGEN FREE Available

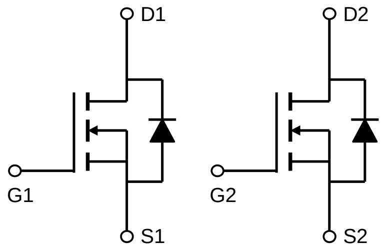
APPLICATIONS

- DC/DC Conversion
  - Notebook System Power

SO-8



Top View



Absolute Maximum Ratings T_A=25℃ unless otherwise noted				
Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_A=25℃	I_D	3.0	A
	T_A=70℃		2.5	
Pulsed Drain Current [C]		I_{DM}	10	
Avalanche Current [C]		I_{AR}	2	A
Repetitive avalanche energy L=0.1mH [C]		E_{AR}	12.8	mJ
Power Dissipation [B]	T_A=25℃	P_D	2	W
	T_A=70℃		1.3	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	℃

Thermal Characteristics					
Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	48	62.5	℃/W
Maximum Junction-to-Ambient [A D]	Steady-State		74	90	℃/W
Maximum Junction-to-Lead	Steady-State	$R_{\theta JL}$	32	40	℃/W

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	100			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=80V, V_{GS}=0V			1	µA
		T_J=55℃			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±30V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1	2	3	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	5			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=2.5A		200		mΩ
		T_J=125℃		253		
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=2.5A		15		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.77	1	V
I_S	Maximum Body-Diode Continuous Current				2.5	A
I_{SM}	Pulsed Body-diode Current[C]				18	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=40V, f=1MHz	510	740	970	pF
C_{oss}	Output Capacitance		28	40	52	pF
C_{rss}	Reverse Transfer Capacitance		12	20	30	pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	0.9	1.8	2.7	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=40V, I_D=2.5A	8	11	13	nC
Q_g(4.5V)	Total Gate Charge		4	5.5	7	
Q_{gs}	Gate Source Charge		4	5	6	nC
Q_{gd}	Gate Drain Charge		0.7	1.2	1.7	nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=40V, R_L=8Ω, R_{GEN}=3Ω		7.2		ns
t_r	Turn-On Rise Time			2.2		ns
$t_{D(off)}$	Turn-Off DelayTime			17		ns
t_f	Turn-Off Fall Time			2		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=2.5A, dI/dt=300A/µs	14	20	26	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=2.5A, dI/dt=300A/µs	35	50	65	nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25℃. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150℃, using ≤ 10s junction-to-ambient thermal resistance.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150℃. Ratings are based on low frequency and duty cycles to keep initialT_J=25℃.
D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on 1in^2 FR-4 board with

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

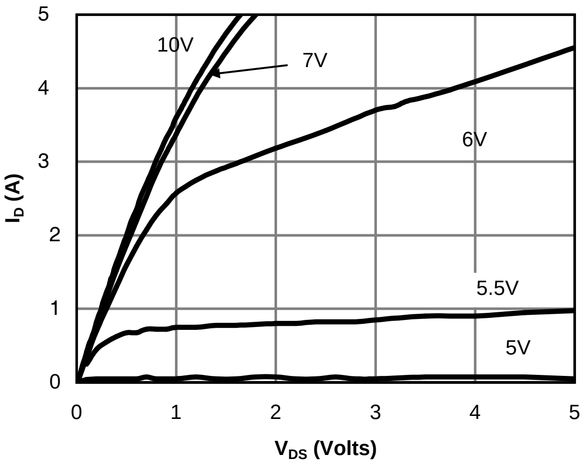


Fig 1: On-Region Characteristics (Note E)

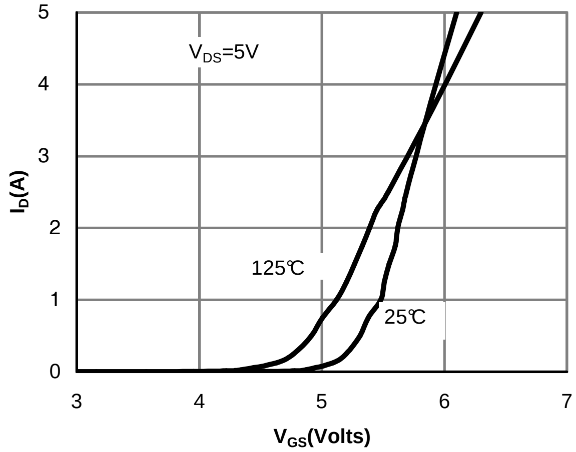


Figure 2: Transfer Characteristics (Note E)

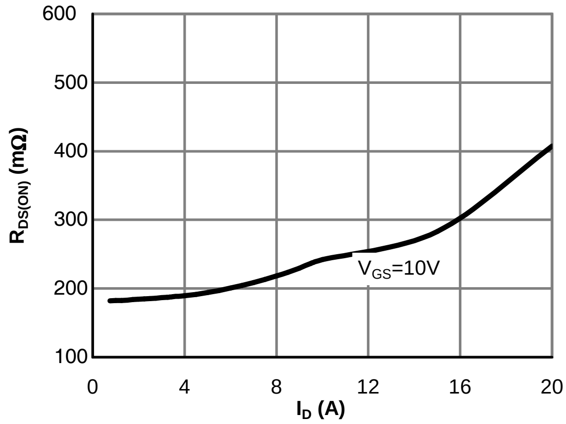


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

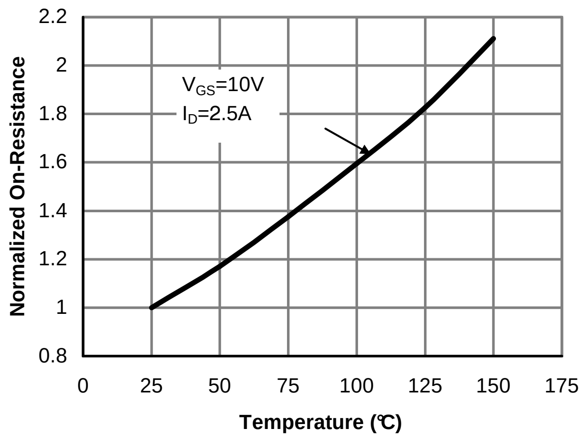


Figure 4: On-Resistance vs. Junction Temperature (Note E)

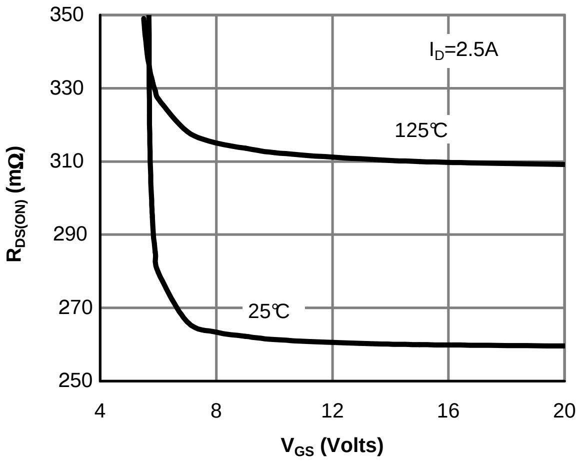


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

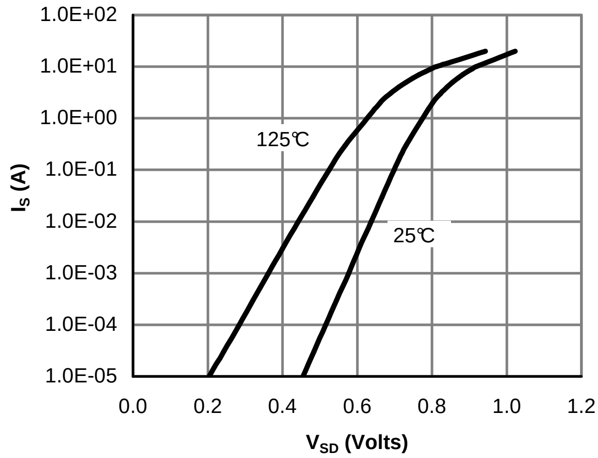


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

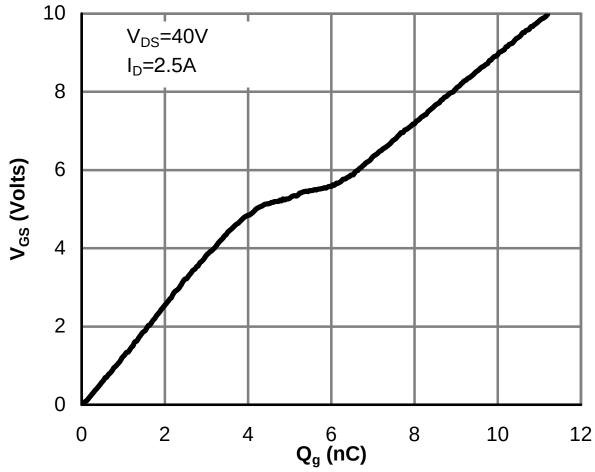


Figure 7: Gate-Charge Characteristics

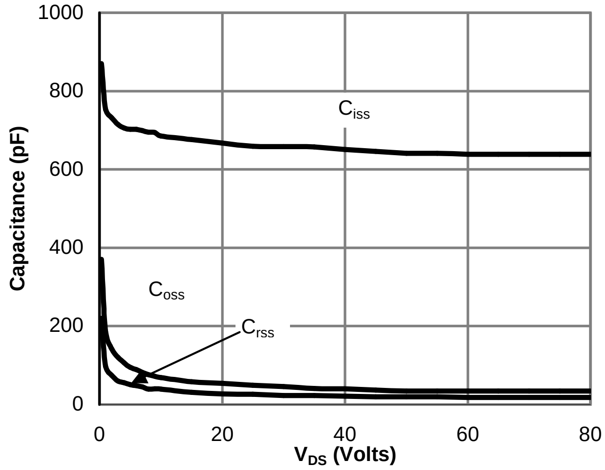


Figure 8: Capacitance Characteristics

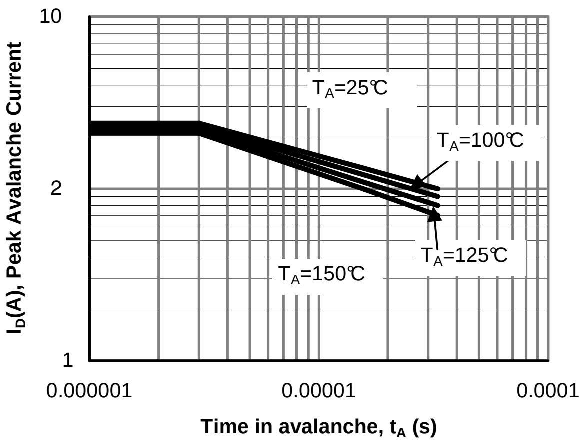


Figure 12: Single Pulse Avalanche capability

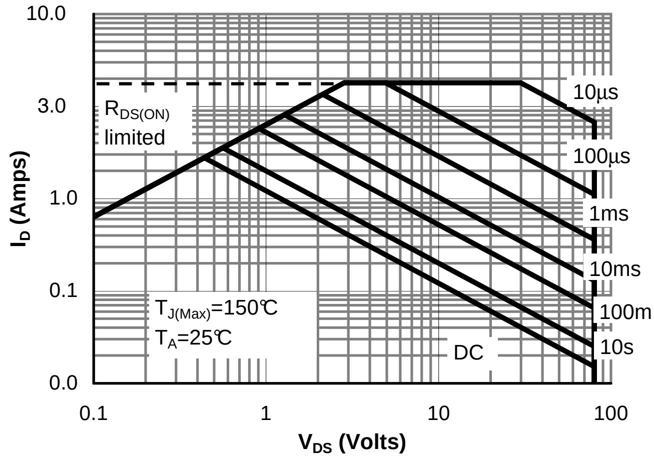


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

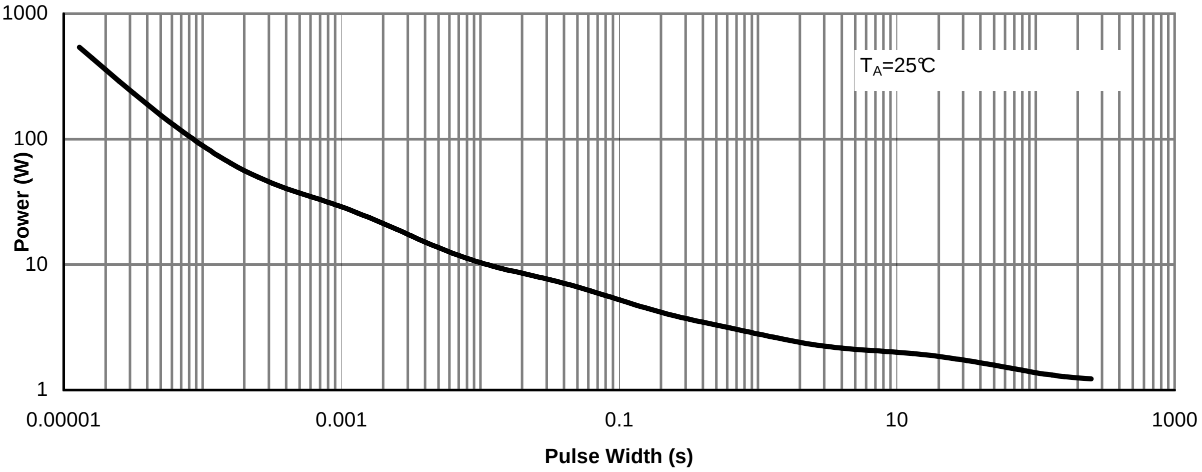


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

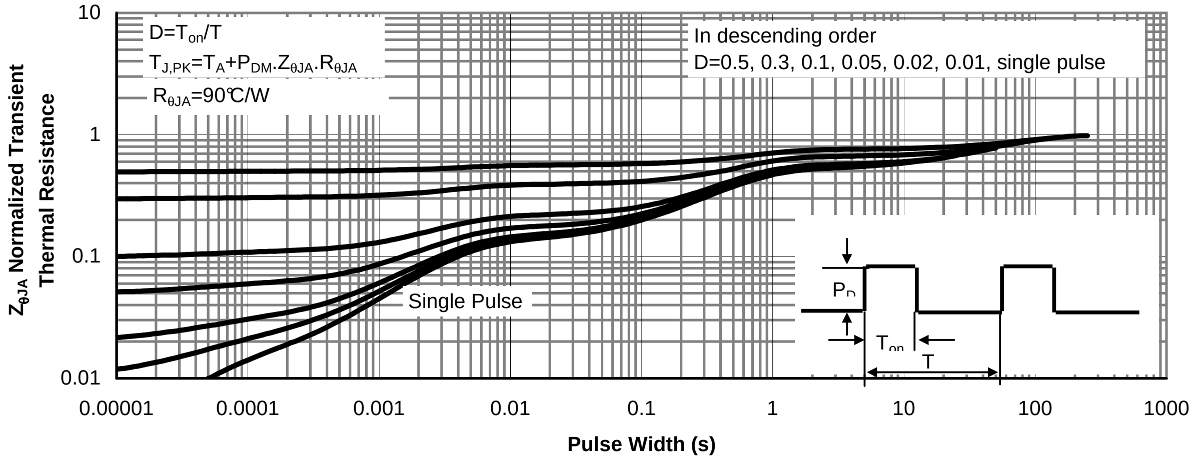
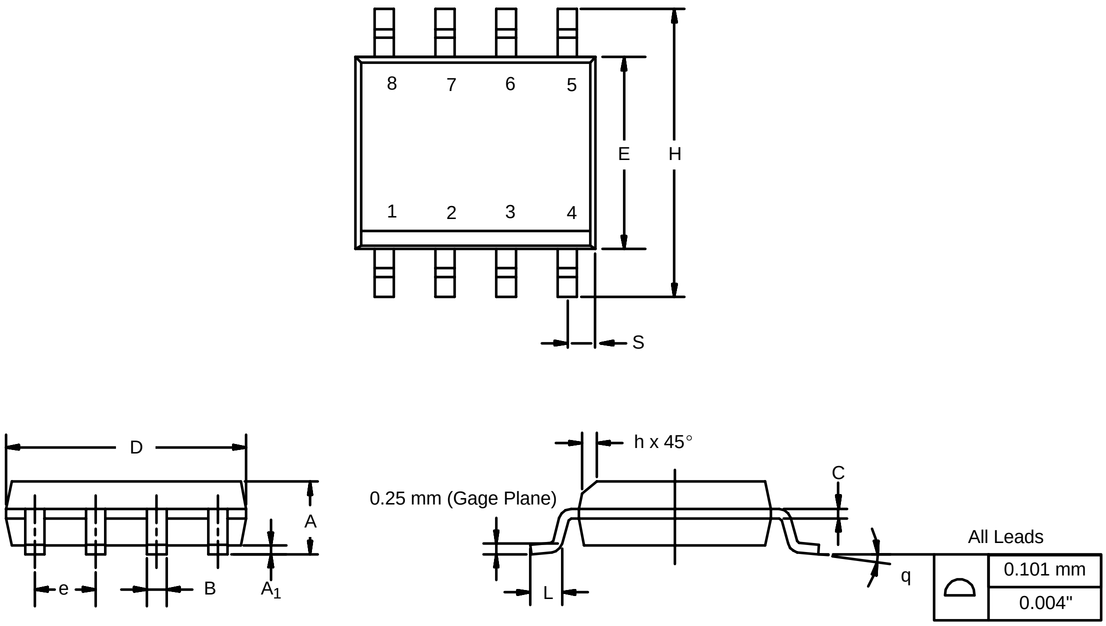


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

SOIC (NARROW): 8-LEAD

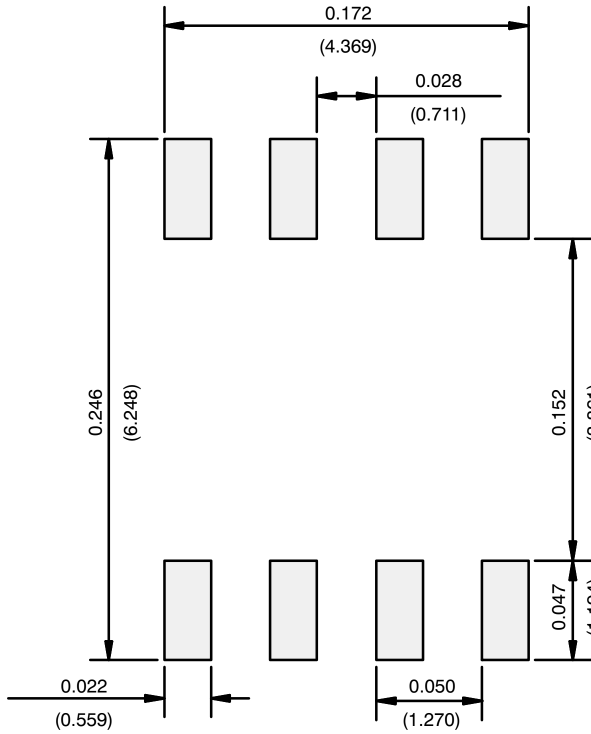
JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026

ECN: C-06527-Rev. I, 11-Sep-06
DWG: 5498

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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