

# AO4435-VB Datasheet P-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY						
V <sub>DS</sub> (V)	$R_{DS(on)}\left(\Omega\right)$	I <sub>D</sub> (A) <sup>d</sup>	Q <sub>g</sub> (Typ.)			
- 30	0.018 at V <sub>GS</sub> = - 10 V	- 9.0	13 nC			
	0.024 at V <sub>GS</sub> = - 4.5 V	- 7.8	13110			

#### **FEATURES**

- Halogen-free According to IEC 61249-2-21 Definition
- Trench Power MOSFET
- 100 % R<sub>g</sub> Tested

# RoHS COMPLIANT HALOGEN

FREE

#### **APPLICATIONS**

- Load Switch
- · Battery Switch



P-Channel MOSFET

	SO-8	
S 1		8 D
S 2		7 D
S 3		6 D
G 4		5 D
L	Top View	J

Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	V <sub>DS</sub>	- 30	V		
Gate-Source Voltage	$V_{GS}$	± 20			
	T <sub>C</sub> = 25 °C		- 9.0		
Continuous Drain Current (T <sub>.1</sub> = 150 °C)	T <sub>C</sub> = 70 °C		- 7.2	A	
Continuous Diain Current (1) = 150 °C)	T <sub>A</sub> = 25 °C	l <sub>D</sub>	- 7.0 <sup>a, b</sup>		
	T <sub>A</sub> = 70 °C		- 5.6 <sup>a, b</sup>		
Pulsed Drain Current	I <sub>DM</sub>	- 30	1		
Continuous Course Danie Biodo Current	T <sub>C</sub> = 25 °C	1	- 3.5		
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	- I <sub>S</sub> -	- 2.1 <sup>a, b</sup>		
	T <sub>C</sub> = 25 °C		4.2		
Mariana Paran Piada di a	T <sub>C</sub> = 70 °C		2.7	1 ,,,	
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	2.5 <sup>a, b</sup>	W	
	T <sub>A</sub> = 70 °C	1	1.6 <sup>a, b</sup>		
Operating Junction and Storage Temperature Rang	T <sub>J</sub> , T <sub>stq</sub>	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>a, c</sup>	t ≤ 10 s	R <sub>thJA</sub>	40	50	°C/W	
Maximum Junction-to-Foot	Steady State	R <sub>thJF</sub>	24	30	C/VV	

#### Notes:

- a. Surface mounted on 1" x 1" FR4 board.
- b. t = 10 s.
- c. Maximum under Steady State conditions is 95 °C/W.
- d. Based on  $T_C = 25$  °C.



Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	- 30			V	
V <sub>DS</sub> Temperature Coefficient	AVps/Ti			- 31		m\//°C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = - 250 μA		4.5		mV/°C	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	- 1.0		- 2.5	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zara Cata Valtaga Drain Current	I	V <sub>DS</sub> = - 30 V, V <sub>GS</sub> = 0 V			- 1		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = - 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			- 5	μA	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \le -5 \text{ V}, V_{GS} = -10 \text{ V}$	- 20			Α	
	D	V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 7.0 A		0.018			
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 5.6 A		0.024		Ω	
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = - 15 V, I <sub>D</sub> = - 7.0 A		18		S	
Dynamic <sup>b</sup>		·					
Input Capacitance	C <sub>iss</sub>			1455		pF	
Output Capacitance	C <sub>oss</sub>	$V_{DS} = -15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		180			
Reverse Transfer Capacitance	C <sub>rss</sub>			145			
	Q <sub>g</sub>	$V_{DS} = -15 \text{ V}, V_{GS} = -10 \text{ V}, I_{D} = -7.0 \text{ A}$		25	38	nC	
Total Gate Charge				13	20		
Gate-Source Charge	$Q_{gs}$	$V_{DS} = -15 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -7.0 \text{ A}$		3.5			
Gate-Drain Charge	Q <sub>qd</sub>			5.5			
Gate Resistance	R <sub>q</sub>	f = 1 MHz	0.4	2.0	4.0	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			10	20		
Rise Time t <sub>r</sub>		$V_{DD} = -15 \text{ V}, R_L = 2.7 \Omega$		13	20	1	
Turn-Off DelayTime	t <sub>d(off)</sub>	$I_D \cong -5.6 \text{ A}, V_{GEN} = -10 \text{ V}, R_g = 1 \Omega$		23	35		
Fall Time	t <sub>f</sub>	1		9	18		
Turn-On Delay Time	t <sub>d(on)</sub>			38	57	ns	
Rise Time	t <sub>r</sub>	$V_{DD} = -15 \text{ V}, R_{L} = 2.7 \Omega$		89	134		
Turn-Off DelayTime	t <sub>d(off)</sub>	$I_D \cong -5.6 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_g = 1 \Omega$		22	33		
Fall Time	t <sub>f</sub>	1		11	17		
Drain-Source Body Diode Characteris	tics					•	
ontinous Source-Drain Diode Current $I_S$ $T_C = 25 ^{\circ}C$		T <sub>C</sub> = 25 °C			- 6.5		
Pulse Diode Forward Current	I <sub>SM</sub>	-			- 30	- A	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = - 5.6 A, V <sub>GS</sub> = 0 V		- 0.71	- 1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			22	33	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			17	26	nC	
Reverse Recovery Fall Time	t <sub>a</sub>	$I_F = -5.6 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$		13		ns	
Reverse Recovery Rise Time	t <sub>b</sub>	1		9			

#### Notes:

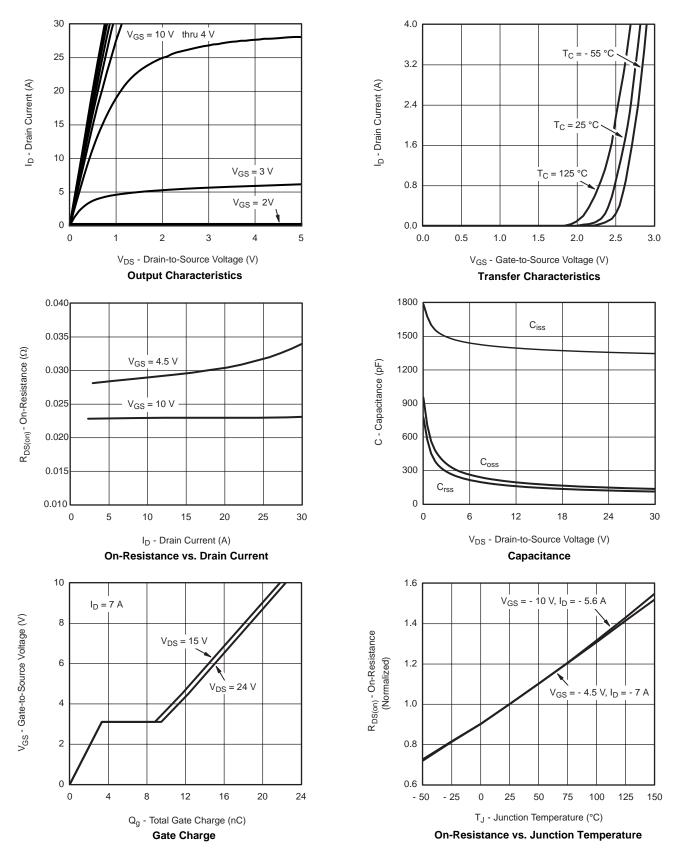
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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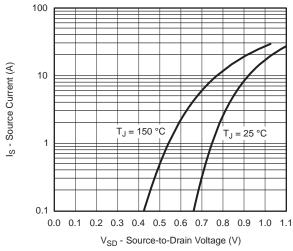
a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$ 

b. Guaranteed by design, not subject to production testing.

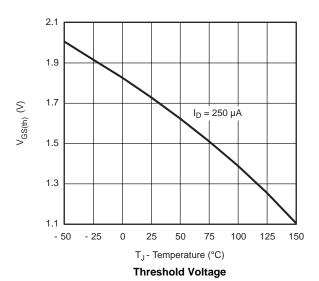








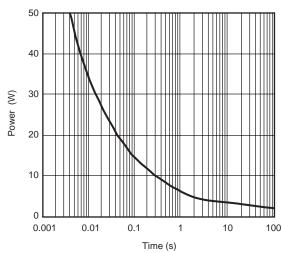
#### Source-Drain Diode Forward Voltage



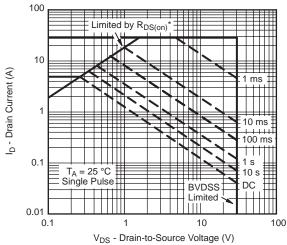
 $C_{O}$   $C_{O$ 

V<sub>GS</sub> - Gate-to-Source Voltage (V)

On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient

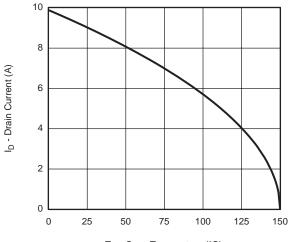


\* V<sub>GS</sub> > minimum V<sub>GS</sub> at which R<sub>DS(on)</sub> is specified

Safe Operating Area

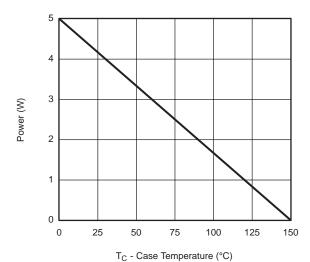
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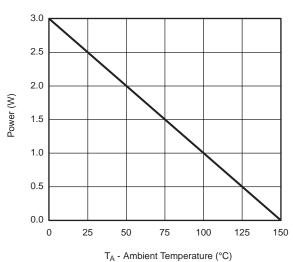


T<sub>C</sub> - Case Temperature (°C)

## Current Derating\*



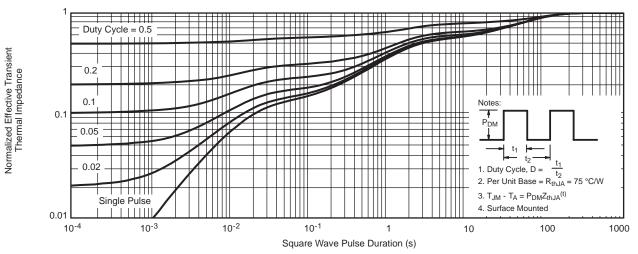
Power, Junction-to-Foot



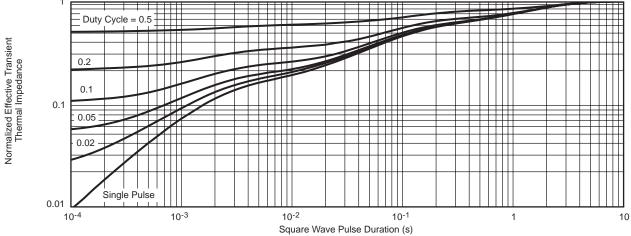
Power Derating, Junction-to-Ambient

<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

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**SOIC (NARROW): 8-LEAD** JEDEC Part Number: MS-012







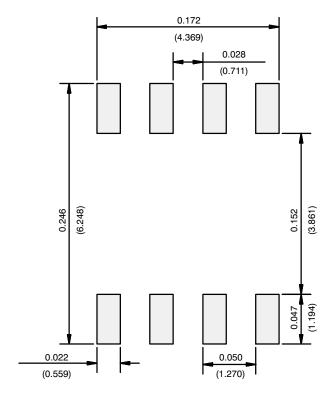
	MILLIMETERS		INCHES		
DIM	Min	Max	Min	Max	
Α	1.35	1.75	0.053	0.069	
A <sub>1</sub>	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
E	3.80	4.00	0.150	0.157	
е	1.27 BSC		0.050 BSC		
Н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
FCN: C-06527-Rev I 11-Sep-06					

ECN: C-06527-Rev. I, 11-Sep-06

DWG: 5498



# **RECOMMENDED MINIMUM PADS FOR SO-8**



Recommended Minimum Pads Dimensions in Inches/(mm)



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