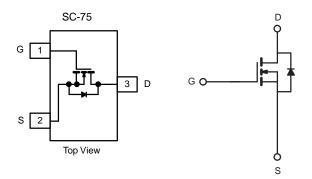


Si1032X-T1-GE3-VB Datasheet N-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^c	Q _g (TYP.)		
20	$0.270 \text{ at V}_{GS} = 4.5 \text{ V}$	0.85			
	0.390 at V _{GS} = 2.5 V	0.70	1.4 nC		



FEATURES

- Trench power MOSFET
- 100 % R_g tested

APPLICATIONS

- Smart phones, tablet PC's
 - DC/DC converters
 - Boost converters
 - Load switch, OVP switch



PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V _{DS}	20	V
Gate-Source Voltage		V _{GS}	± 12	V
	T _C = 25 °C		0.85	
Continuous Prais Current /T 150 °C\	T _C = 70 °C	1 . 🗀	0.65	
Continuous Drain Current (T _J = 150 °C)	T _A = 25 °C	I _D	0.7 ^{a, b}	
	T _A = 70 °C		0.6 ^{a, b}	Α
Pulsed Drain Current (t = 300 μs)		I _{DM}	6	
Continuous Source-Drain Diode Current	T _C = 25 °C		0.4	
Continuous Source-Drain Diode Current	T _A = 25 °C	l _S —	0.3	
	T _C = 25 °C		0.5	
Maximum Davier Dissination	T _C = 70 °C		0.3	w
Maximum Power Dissipation	T _A = 25 °C	P _D	0.4 ^{a, b}	VV
	T _A = 70 °C		0.3 ^{a, b}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C	
Soldering Recommendations (Peak Temperature)		260		

THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient a, d	t ≤ 10 s	R _{thJA}	250	300	°C/W	
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	225	270	C/VV	

Notes

- a. Surface mounted on 1" x 1" FR4 board.
- b. t = 10 s.
- c. Based on T_C = 25 °C.
- d. Maximum under steady state conditions is 360 $^{\circ}\text{C/W}.$



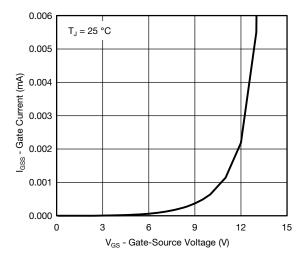
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static					I.	
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	20	-	-	V
V _{DS} Temperature Coefficient	$\frac{\Delta V_{DS}/T_J}{\Delta V_{GS(th)}/T_J}$ $I_D = 250 \ \mu A$		-	32	-	mV/°C
V _{GS(th)} Temperature Coefficient			-	-3	-	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	0.5	-	1.0	V
Cata Carrian Lagliana		V _{DS} = 0 V, V _{GS} = 4.5 V	-	-	0.1	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 12 V	-	-	± 20	
Zana Onto Vallera a Barin O annul	,	V _{DS} = 20 V, V _{GS} = 0 V	-	-	0.1	- μA -
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V, T _J = 55 °C	-	-	10	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	2	-	-	Α
Drain-Source On-State Resistance a	Book)	V _{GS} = 4.5 V, I _D = 1 A	-	0.270	-	
Diam-Source on-State nesistance	R _{DS(on)}	V _{GS} = 2.5 V, I _D = 0.5 A	-	0.390	-	Ω
Forward Transconductance ^a	9 _{fs}	V _{DS} = 10 V, I _D = 1.4 A	-	5	-	S
Dynamic ^b						
Input Capacitance	C _{iss}		-	105	-	pF
Output Capacitance	C _{oss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	23	-	
Reverse Transfer Capacitance	C _{rss}		-	11	-	
Total Cata Chausa	Q_g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 1.4 A	-	2.7	4.1	nC
Total Gate Charge			-	1.4	2.1	
Gate-Source Charge	Q _{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 1.4 \text{ A}$	-	0.3	-	
Gate-Drain Charge	Q_{gd}		-	0.5		
Gate Resistance	R _g	f = 1 MHz	1.4	7	14	Ω
Turn-On Delay Time	t _{d(on)}		-	2	4	1
Rise Time	t _r	$V_{DD} = 15 \text{ V}, R_1 = 13.6 \Omega$	-	9	18	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 1.1 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	8	16	
Fall Time	t _f		-	8	16	
Turn-On Delay Time	t _{d(on)}		-	8	16	ns
Rise Time	t _r	$V_{DD} = 15 \text{ V}, R_L = 13.6 \Omega$		13	20	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 1.1 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$	-	15	23	
Fall Time	t _f		-	6	12	
Drain-Source Body Diode Characterist						
Continuous Source-Drain Diode Current	Is	T _C = 25 °C	-	-	0.4	Λ.
Pulse Diode Forward Current ^a	I _{SM}		-	-	6	Α
Body Diode Voltage	V _{SD}	I _F = 1.1 A	-	0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}		-	8	16	ns
Body Diode Reverse Recovery Charge	Body Diode Reverse Recovery Charge Qr.		-	3	6	nC
Reverse Recovery Fall Time	t _a	$I_F = 1.1 \text{ A, dI/dt} = 100 \text{ A/}\mu\text{s, T}_J = 25 ^{\circ}\text{C}$	-	5	-	
Reverse Recovery Rise Time	t _b		-	3	-	ns

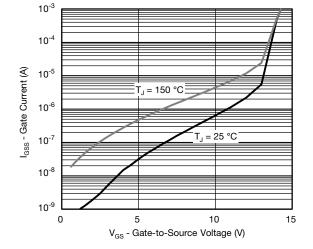
Notes

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

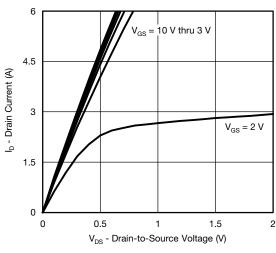


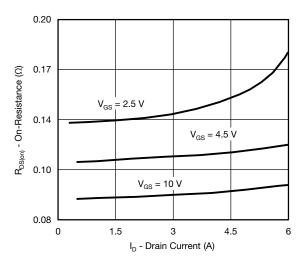




Gate Source Voltage vs. Gate Current

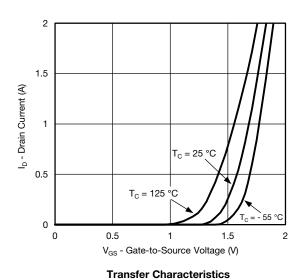
Gate Source Voltage vs. Gate Current

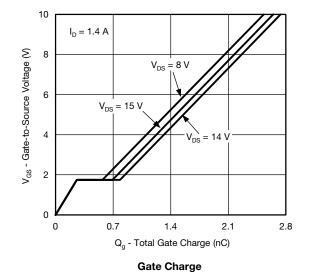




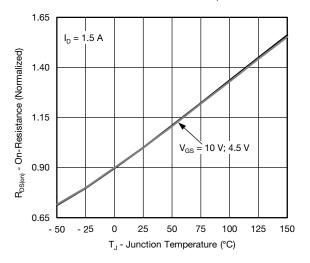
Output Characteristics

On-Resistance vs. Drain Current

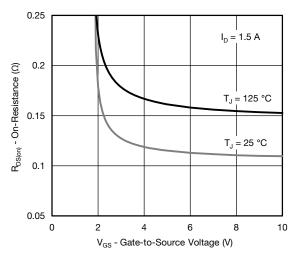




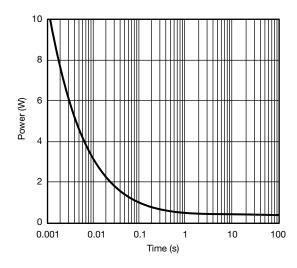




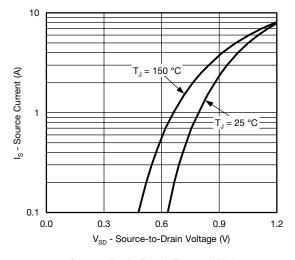
On-Resistance vs. Junction Temperature



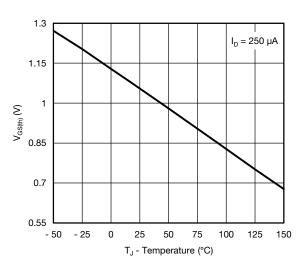
On-Resistance vs. Gate-to-Source Voltage



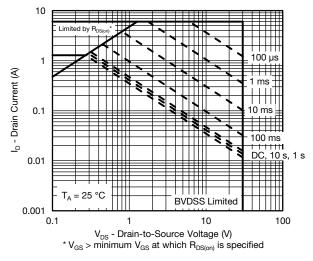
Single Pulse Power, Junction-to-Ambient



Source-Drain Diode Forward Voltage

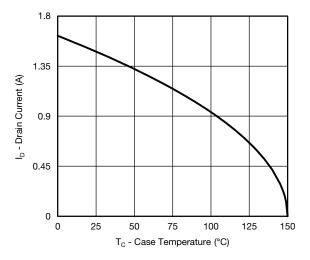


Threshold Voltage

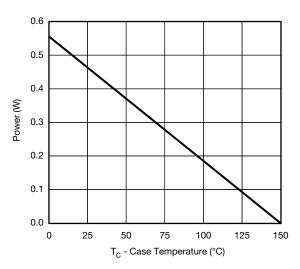


Safe Operating Area, Junction-to-Ambient

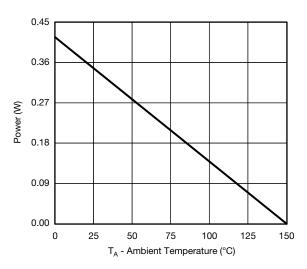




Current Derating*





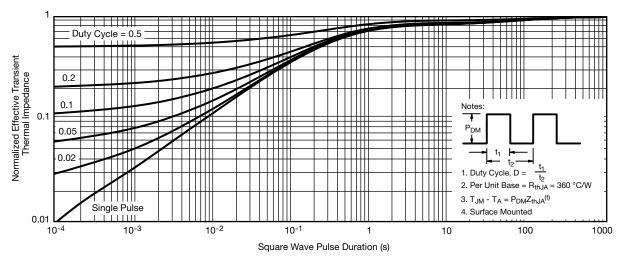


Power, Junction-to-Ambient

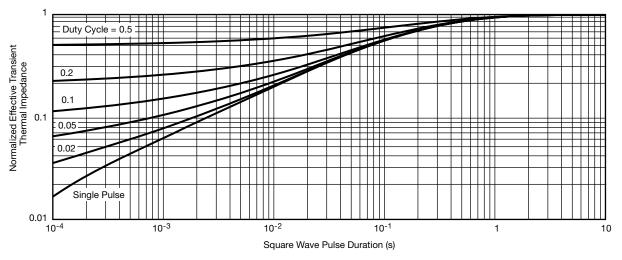
5

^{*} The power dissipation P_D is based on $T_{J \text{ (max.)}} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





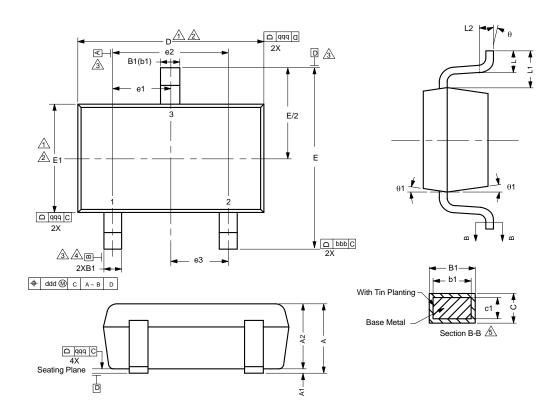
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot



SC-75A: 3 Leads



Notes

Dimensions in millimeters will govern.

Dimension D does not include mold flash, protrusions or gate burrs. Mold flash protrusions or gate burrs shall not exceed 0.10 mm per end. Dimension E1 does not include Interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.10 mm per side.

Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interelead flash, but including any mismatch between the top and bottom of the plastic body.

Datums A, B and D to be determined 0.10 mm from the lead tip.

A Terminal positions are shown for reference only.

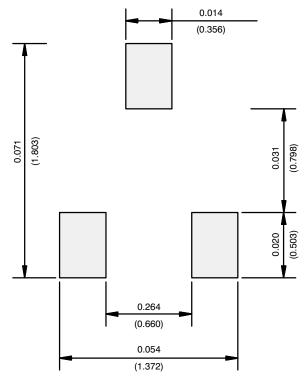
These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

DIMENSIONS	TOLERANCES
aaa	0.10
bbb	0.10
ccc	0.10
ddd	0.10

DIM.	l l			
Dilvi.	MIN.	NOM.	MAX.	NOTE
Α	-	-	0.80	
A ₁	0.00	-	0.10	
A ₂	0.65	0.70	0.80	
B ₁	0.19	-	0.24	5
b ₁	0.17	-	0.21	
С	0.13	-	0.15	5
C ₁	0.10	-	0.12	5
D	1.48	1.575	1.68	1, 2
E	1.50	1.60	1.70	
E ₁	0.66	0.76	0.86	1, 2
e ₁				
e ₂				
e ₃	0.50 BSC			
L	0.15	0.205	0.30	
L ₁	0.40 ref.			
L ₂	0.15 BSC			·
θ	0°	-	8°	·
θ1	4°	=	10°	



RECOMMENDED MINIMUM PADS FOR SC-75A: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)



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