

SSM3K15FS-VB Datasheet

N-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^c	Q_g (TYP.)
20	0.270 at $V_{GS} = 4.5$ V	0.85	1.4 nC
	0.390 at $V_{GS} = 2.5$ V	0.70	

FEATURES

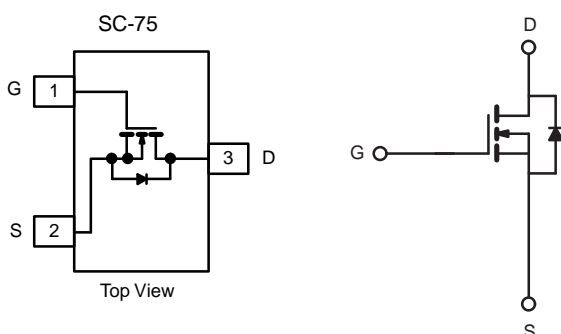
- Trench power MOSFET
- 100 % R_g tested

APPLICATIONS

- Smart phones, tablet PC's
 - DC/DC converters
 - Boost converters
 - Load switch, OVP switch



RoHS
COMPLIANT
HALOGEN
FREE



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	$T_C = 25^\circ\text{C}$	I_D	0.85	A
	$T_C = 70^\circ\text{C}$		0.65	
	$T_A = 25^\circ\text{C}$		0.7 ^{a, b}	
	$T_A = 70^\circ\text{C}$		0.6 ^{a, b}	
Pulsed Drain Current ($t = 300 \mu\text{s}$)		I_{DM}	6	
Continuous Source-Drain Diode Current	$T_C = 25^\circ\text{C}$	I_S	0.4	
	$T_A = 25^\circ\text{C}$		0.3	
Maximum Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	0.5	W
	$T_C = 70^\circ\text{C}$		0.3	
	$T_A = 25^\circ\text{C}$		0.4 ^{a, b}	
	$T_A = 70^\circ\text{C}$		0.3 ^{a, b}	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)			260	

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient ^{a, d}	$t \leq 10$ s	R_{thJA}	250	300	$^\circ\text{C/W}$
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	225	270	

Notes

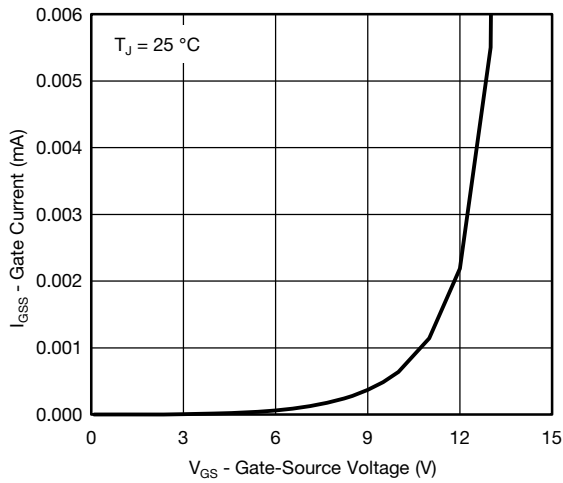
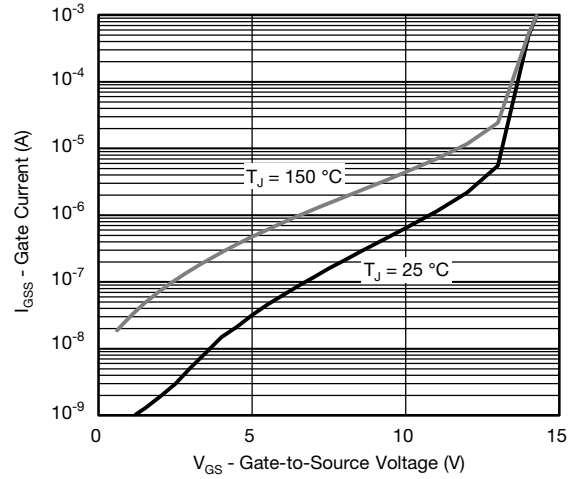
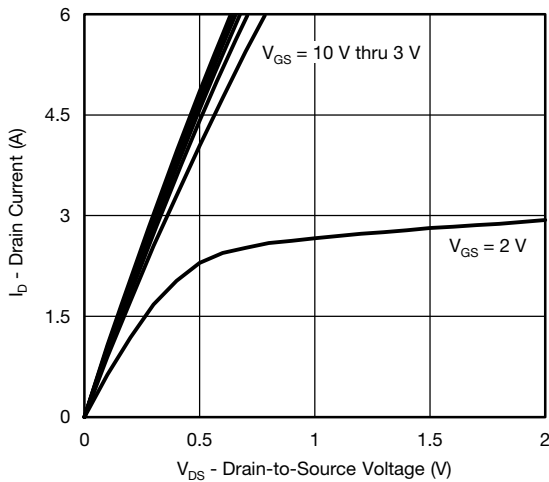
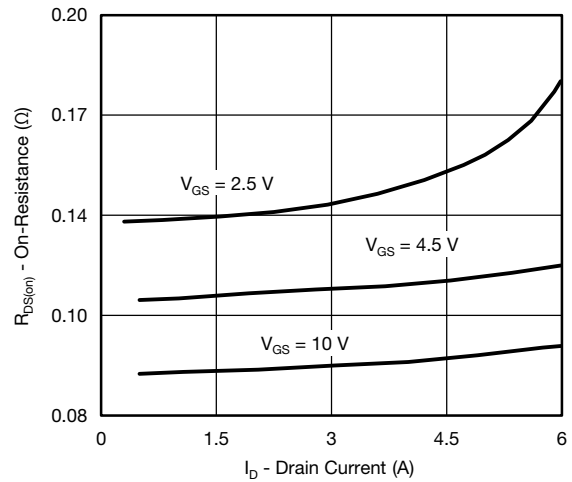
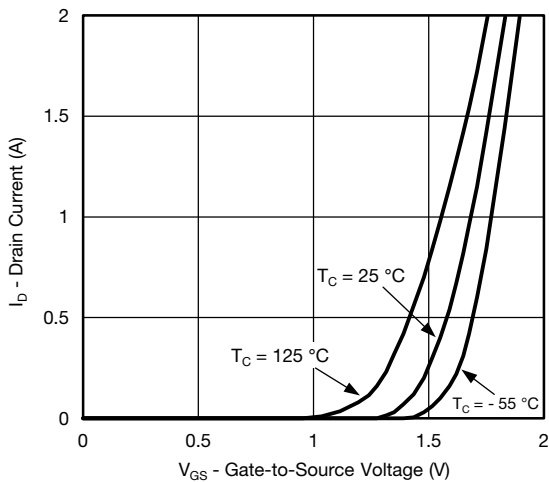
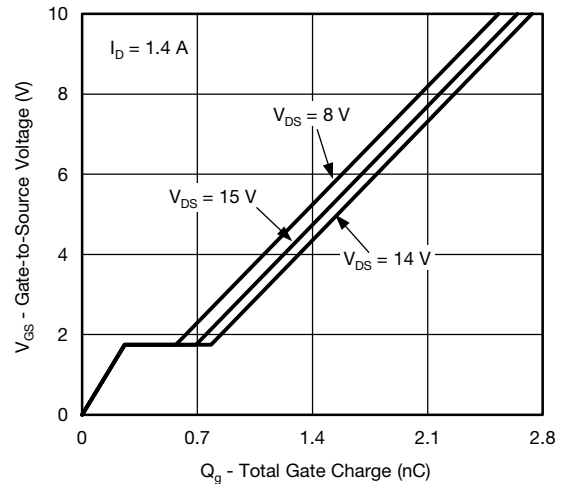
- Surface mounted on 1" x 1" FR4 board.
- $t = 10$ s.
- Based on $T_C = 25^\circ\text{C}$.
- Maximum under steady state conditions is 360°C/W .

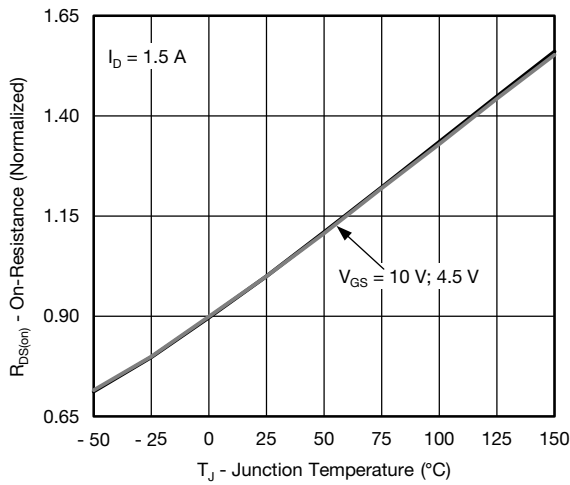
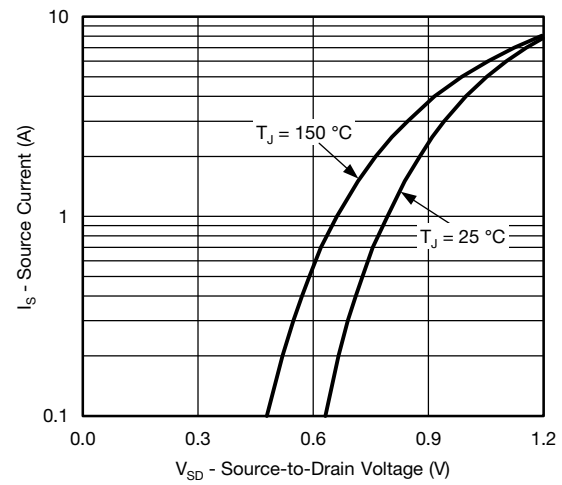
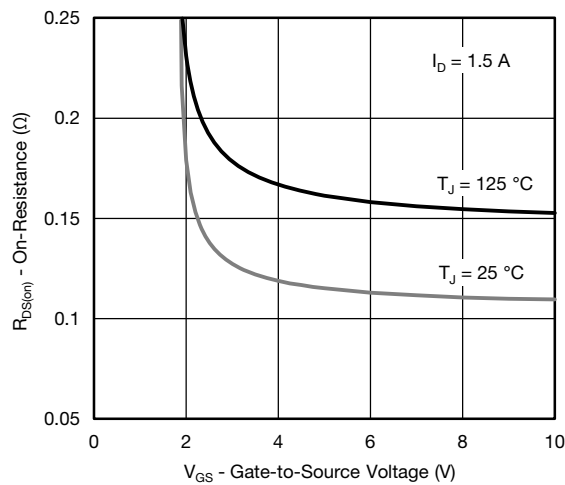
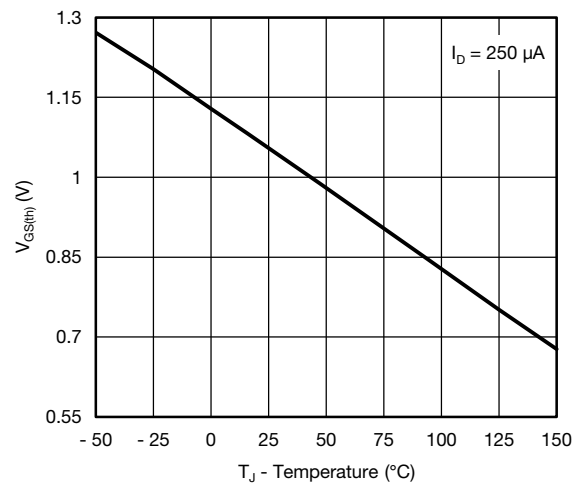
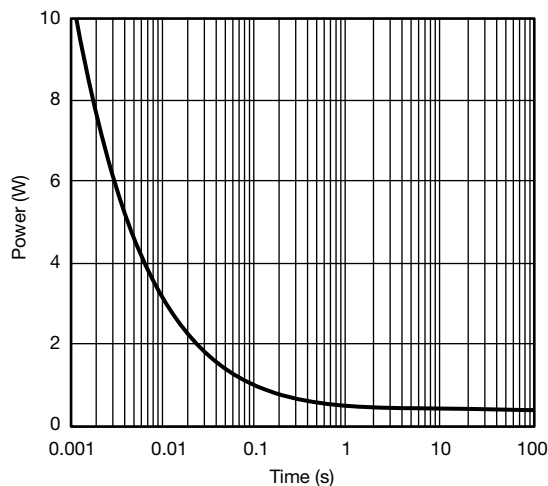
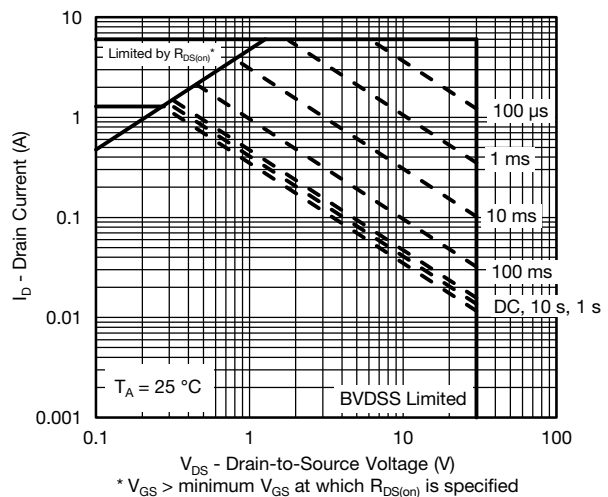
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	20	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA	-	32	-	mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J		-	-3	-	
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.5	-	1.0	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = 4.5 V	-	-	0.1	μA
		V _{DS} = 0 V, V _{GS} = ± 12 V	-	-	± 20	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	-	-	0.1	
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 55 °C	-	-	10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	2	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 1 A	-	0.270	-	Ω
		V _{GS} = 2.5 V, I _D = 0.5 A	-	0.390	-	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 1.4 A	-	5	-	S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	-	105	-	pF
Output Capacitance	C _{oss}		-	23	-	
Reverse Transfer Capacitance	C _{rss}		-	11	-	
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 1.4 A	-	2.7	4.1	nC
		V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 1.4 A	-	1.4	2.1	
Gate-Source Charge	Q _{gs}		-	0.3	-	
Gate-Drain Charge	Q _{gd}		-	0.5	-	
Gate Resistance	R _g	f = 1 MHz	1.4	7	14	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 13.6 Ω I _D ≅ 1.1 A, V _{GEN} = 10 V, R _g = 1 Ω	-	2	4	ns
Rise Time	t _r		-	9	18	
Turn-Off Delay Time	t _{d(off)}		-	8	16	
Fall Time	t _f		-	8	16	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 13.6 Ω I _D ≅ 1.1 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	8	16	
Rise Time	t _r		-	13	20	
Turn-Off Delay Time	t _{d(off)}		-	15	23	
Fall Time	t _f		-	6	12	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	-	-	0.4	A
Pulse Diode Forward Current ^a	I _{SM}		-	-	6	
Body Diode Voltage	V _{SD}	I _F = 1.1 A	-	0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 1.1 A, dI/dt = 100 A/μs, T _J = 25 °C	-	8	16	ns
Body Diode Reverse Recovery Charge	Q _{rr}		-	3	6	nC
Reverse Recovery Fall Time	t _a		-	5	-	ns
Reverse Recovery Rise Time	t _b		-	3	-	

Notes

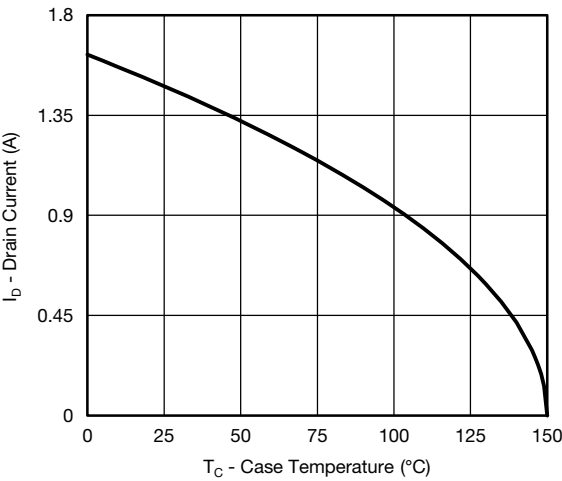
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

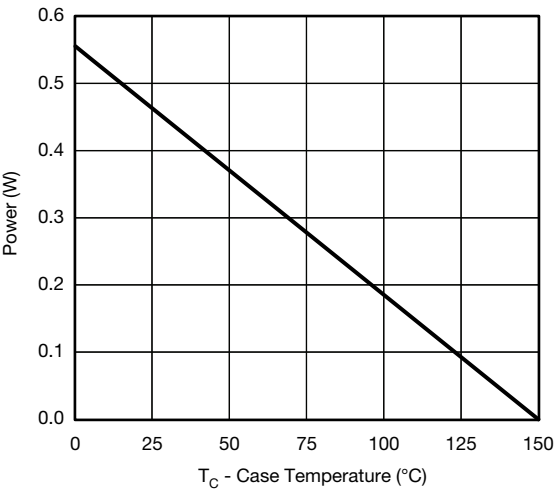
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)**Gate Source Voltage vs. Gate Current****Gate Source Voltage vs. Gate Current****Output Characteristics****On-Resistance vs. Drain Current****Transfer Characteristics****Gate Charge**

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

On-Resistance vs. Junction Temperature

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Single Pulse Power, Junction-to-Ambient

Safe Operating Area, Junction-to-Ambient

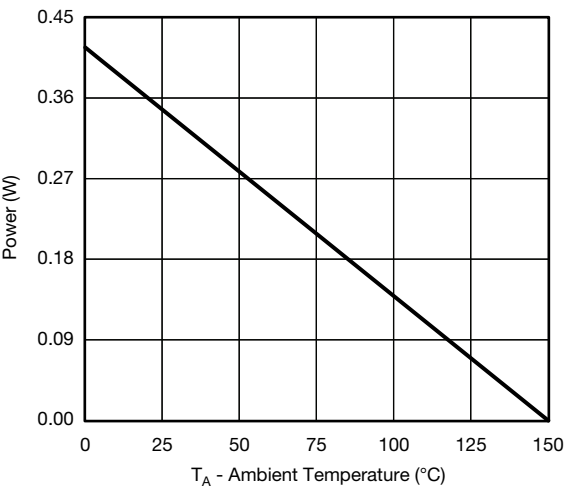
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



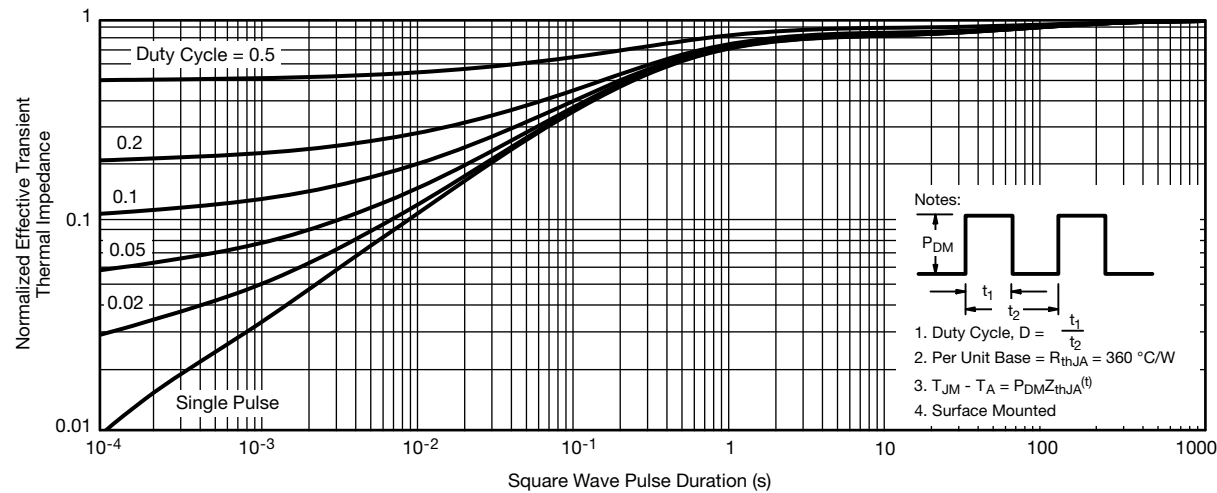
Power, Junction-to-Case



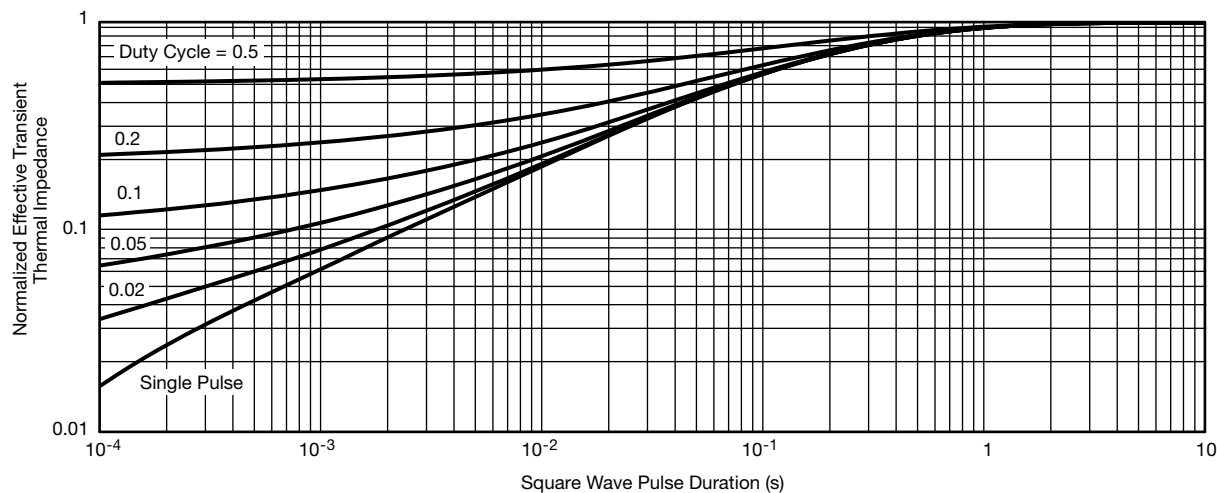
Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max.)} = 150\text{ °C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

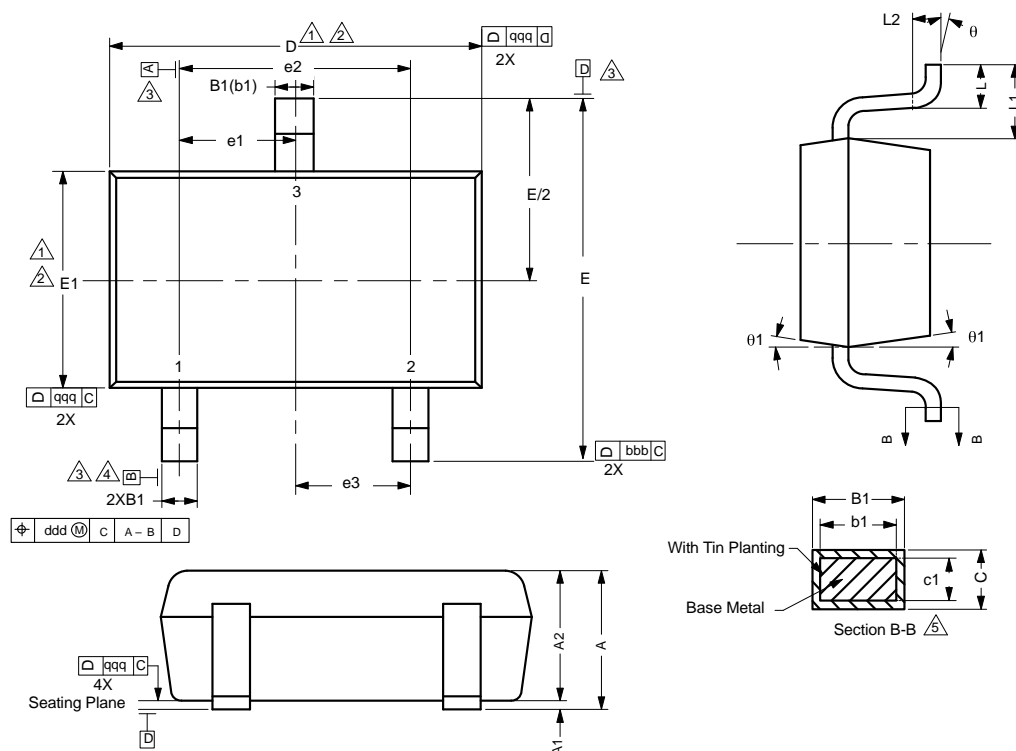


Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

SC-75A: 3 Leads



Notes

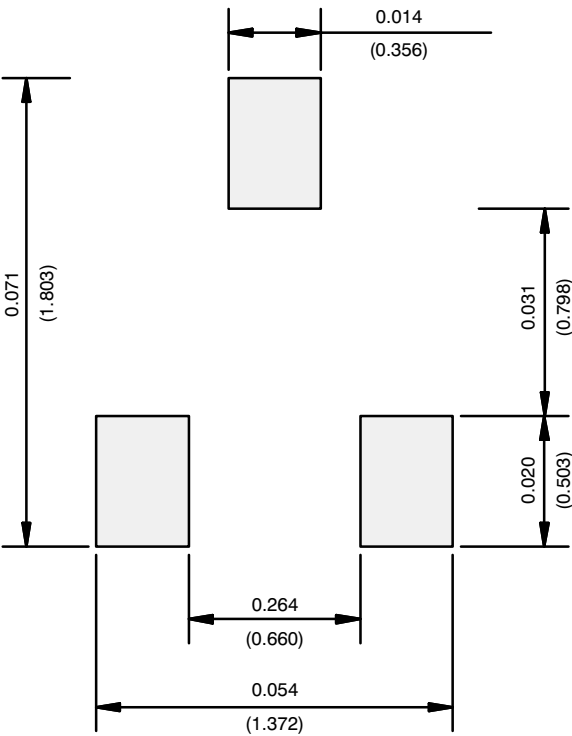
Dimensions in millimeters will govern.

1. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash protrusions or gate burrs shall not exceed 0.10 mm per end. Dimension E1 does not include Interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.10 mm per side.
2. Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
3. Datums A, B and D to be determined 0.10 mm from the lead tip.
4. Terminal positions are shown for reference only.
5. These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

DIMENSIONS	TOLERANCES
aaa	0.10
bbb	0.10
ccc	0.10
ddd	0.10

DIM.	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	-	-	0.80	
A ₁	0.00	-	0.10	
A ₂	0.65	0.70	0.80	
B ₁	0.19	-	0.24	5
b ₁	0.17	-	0.21	
c	0.13	-	0.15	5
c ₁	0.10	-	0.12	5
D	1.48	1.575	1.68	1, 2
E	1.50	1.60	1.70	
E ₁	0.66	0.76	0.86	1, 2
e ₁	0.50 BSC			
e ₂	1.00 BSC			
e ₃	0.50 BSC			
L	0.15	0.205	0.30	
L ₁	0.40 ref.			
L ₂	0.15 BSC			
θ	0°	-	8°	
θ_1	4°	-	10°	

RECOMMENDED MINIMUM PADS FOR SC-75A: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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